

LIN J2602 Transceiver

Features:

- The MCP2003/2003A and MCP2004/2004A are compliant with Local Interconnect Network (LIN) Bus Specifications 1.3, 2.0 and 2.1 and are compliant to SAE J2602
- Support Baud Rates up to 20 kbaud with LIN-Compatible Output Driver
- 43V Load Dump Protected
- Very Low High Electromagnetic Immunity (EMI) meets Stringent Original Equipment Manufacturers (OEM) Requirements
- Very High Electrostatic Discharge (ESD) Immunity:
 - >20 kV on V_{BB} (IEC 61000-4-2)
 - >14 kV on L_{BUS} (IEC 61000-4-2)
- Very High Immunity to RF Disturbances meets Stringent OEM Requirements
- Wide Supply Voltage, 6.0V-27.0V Continuous
- Extended Temperature Range: -40 to +125°C
- Interface to PIC[®] MCU EUSART and Standard USARTs
- LIN Bus Pin:
 - Internal pull-up resistor and diode
 - Protected against battery shorts
 - Protected against loss of ground
 - High current drive
- Automatic Thermal Shutdown
- Low-Power mode:
 - Receiver monitoring bus and transmitter off, ($\cong 5 \mu\text{A}$)



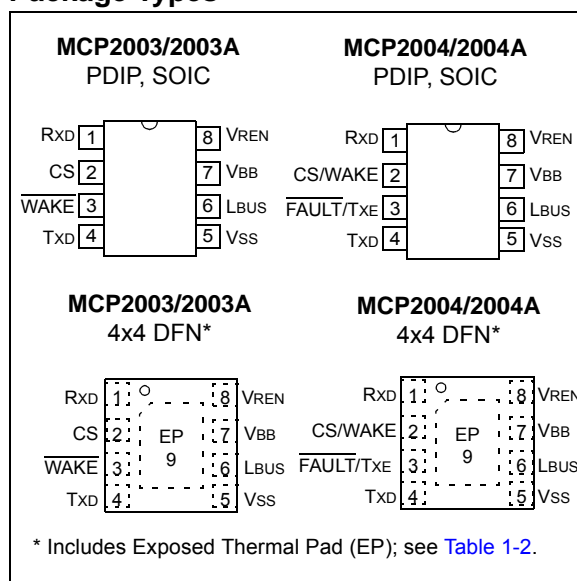
Description:

This device provides a bidirectional, half-duplex communication, physical interface to automotive and industrial LIN systems to meet the LIN Bus Specification Revision 2.1 and SAE J2602. The device is short-circuit and over-temperature protected by internal circuitry. The device has been specifically designed to operate in the automotive operating environment and will survive all specified transient conditions while meeting all of the stringent quiescent current requirements.

MCP200X family members:

- 8-pin PDIP, DFN and SOIC packages:
 - MCP2003, LIN-compatible driver, with WAKE pins, wake-up on falling edge of L_{BUS}
 - MCP2003A, LIN-compatible driver, with WAKE pins, wake-up on rising edge of L_{BUS}
 - MCP2004, LIN-compatible driver, with FAULT/TXE pins, wake-up on falling edge of L_{BUS}
 - MCP2004A, LIN-compatible driver, with FAULT/TXE pins, wake-up on rising edge of L_{BUS}

Package Types



1.0 DEVICE OVERVIEW

The MCP2003/4/3A/4A devices provide a physical interface between a microcontroller and a LIN bus. These devices will translate the CMOS/TTL logic levels to LIN logic level, and vice versa. It is intended for automotive and industrial applications with serial bus speeds up to 20 kbaud.

LIN Bus Specification Revision 2.1 requires that the transceiver of all nodes in the system is connected via the LIN pin, referenced to ground and with a maximum external termination resistance load of 510Ω from LIN bus to battery supply. The 510Ω corresponds to 1 master and 15 slave nodes.

The VREN pin can be used to drive the logic input of an external voltage regulator. This pin is high in all modes except for Power-Down mode.

1.1 External Protection

1.1.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see [Example 1-1](#)).

1.1.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between VBB and ground, with a 50Ω transient protection resistor (RTP) in series with the battery supply and the VBB pin serve to protect the device from power transients (see [Example 1-1](#)) and ESD events. While this protection is optional, it is considered good engineering practice.

1.2 Internal Protection

1.2.1 ESD PROTECTION

For component-level ESD ratings, please refer to the maximum operation specifications.

1.2.2 GROUND LOSS PROTECTION

The LIN Bus specification states that the LIN pin must transition to the recessive state when ground is disconnected. Therefore, a loss of ground effectively forces the LIN line to a high-impedance level.

1.2.3 THERMAL PROTECTION

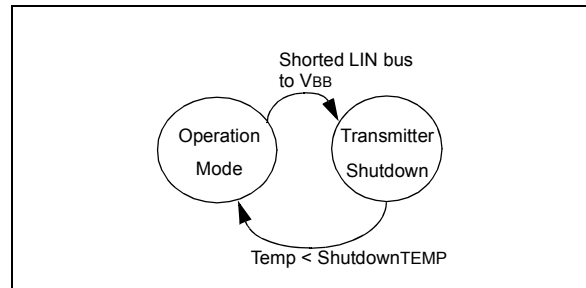
The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter.

There are two causes for a thermal overload. A thermal shutdown can be triggered by either, or both, of the following thermal overload conditions.

- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

Driving the TXD and checking the RXD pin makes it possible to determine whether there is a bus contention (Rx = low, Tx = high) or a thermal overload condition (Rx = high, Tx = low). After a thermal overload event, the device will automatically recover once the die temperature has fallen below the recovery temperature threshold (see [Figure 1-1](#)).

FIGURE 1-1: THERMAL SHUTDOWN STATE DIAGRAM



MCP2003/4/3A/4A

1.3 Modes of Operation

For an overview of all operational modes, refer to Table 1-1.

1.3.1 POWER-DOWN MODE

In Power-Down mode, everything is off except the wake-up section. This is the lowest power mode. The receiver is off, thus its output is open-drain.

On CS going to a high level or a falling edge on $\overline{\text{WAKE}}$ (MCP2003/MCP2003A only), the device will enter Ready mode as soon as internal voltage stabilizes. Refer to Section 2.4 “AC Specifications” for further information. In addition, LIN bus activity will change the device from Power-down mode to Ready mode; MCP2003/4 wakes-up on a falling edge on L_{BUS}, followed by a low level lasting at least 20 μs . MCP2003A/4A wakes-up on a rising edge on L_{BUS}, followed by a high level lasting 70 μs typically. See Figures 1-2 to 1-5 about remote wake-up. If CS is held high as the device transitions from Power-Down to Ready mode, the device will transition to either Operation or Transmitter Off mode, depending on TXD input, as soon as internal voltages stabilize.

1.3.2 READY MODE

Upon entering the Ready mode, V_{REN} is enabled and the receiver detect circuit is powered up. The transmitter remains disabled and the device is ready to receive data but not to transmit.

Upon V_{BB} supply pin power-on, the device will remain in Ready mode as long as CS is low. When CS transitions high, the device will either enter Operation mode, if TXD pin is held high, or the device will enter Transmitter Off mode, if TXD pin is held low.

1.3.3 OPERATION MODE

In this mode, all internal modules are operational.

The device will go into Power-Down mode on the falling edge of CS. For the MCP2003/4 device, a specific process should be followed to put all nodes into Power-Down mode. Refer to Section 1.6 “MCP2003/4 and MCP2003A/4A Difference Details” and Figure 1-6. The device will enter Transmitter Off mode in the event of a Fault condition, such as: thermal overload, bus contention and TXD timer expiration.

The MCP2004/2004A device can also enter Transmitter Off mode if the $\overline{\text{FAULT/TXE}}$ pin is pulled low. The V_{BB} to L_{BUS} pull-up resistor is connected only in Operation mode.

1.3.4 TRANSMITTER OFF MODE

Transmitter Off mode is reached whenever the transmitter is disabled either due to a Fault condition or pulling the $\overline{\text{FAULT/TXE}}$ pin low on the MCP2004/2004A. The Fault conditions include: thermal overload, bus contention, RxD monitoring or TXD timer expiration.

The device will go into Power-Down mode on the falling edge of CS, or return to Operation mode if all faults are resolved and the $\overline{\text{FAULT/TXE}}$ pin on the MCP2004/2004A is high.

FIGURE 1-2: OPERATIONAL MODES STATE DIAGRAM – MCP2003

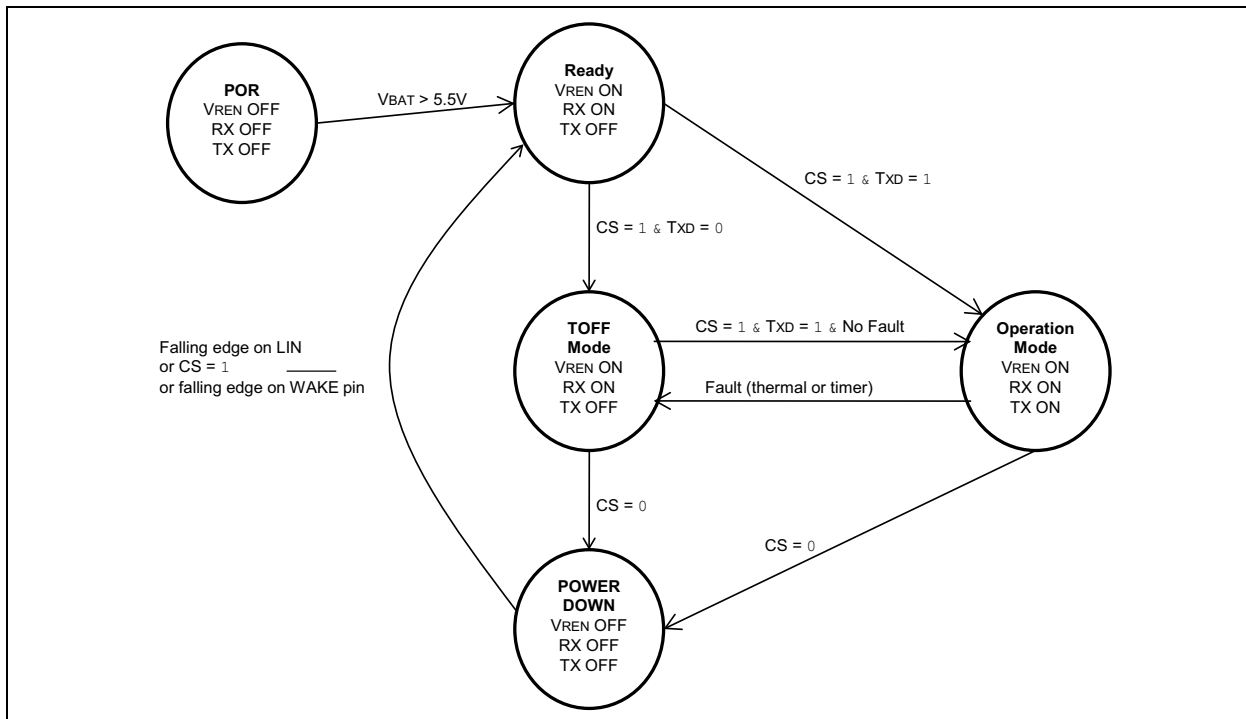


FIGURE 1-3: OPERATIONAL MODES STATE DIAGRAM – MCP2003A

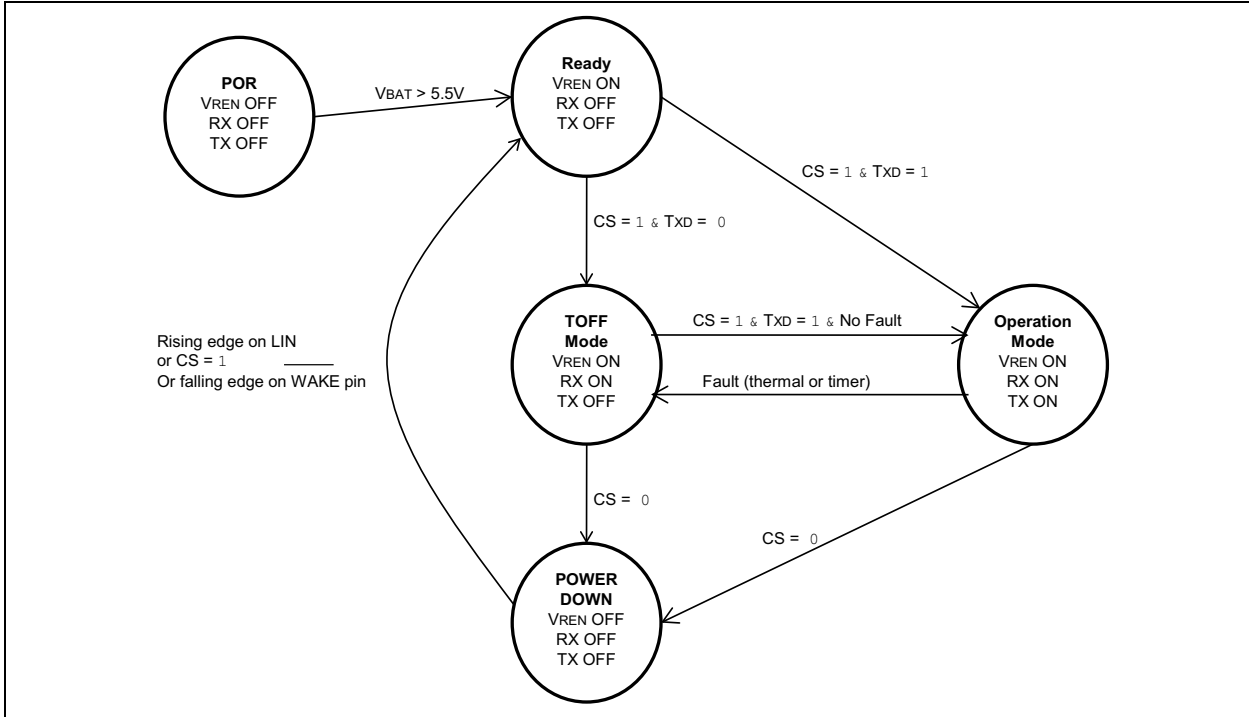
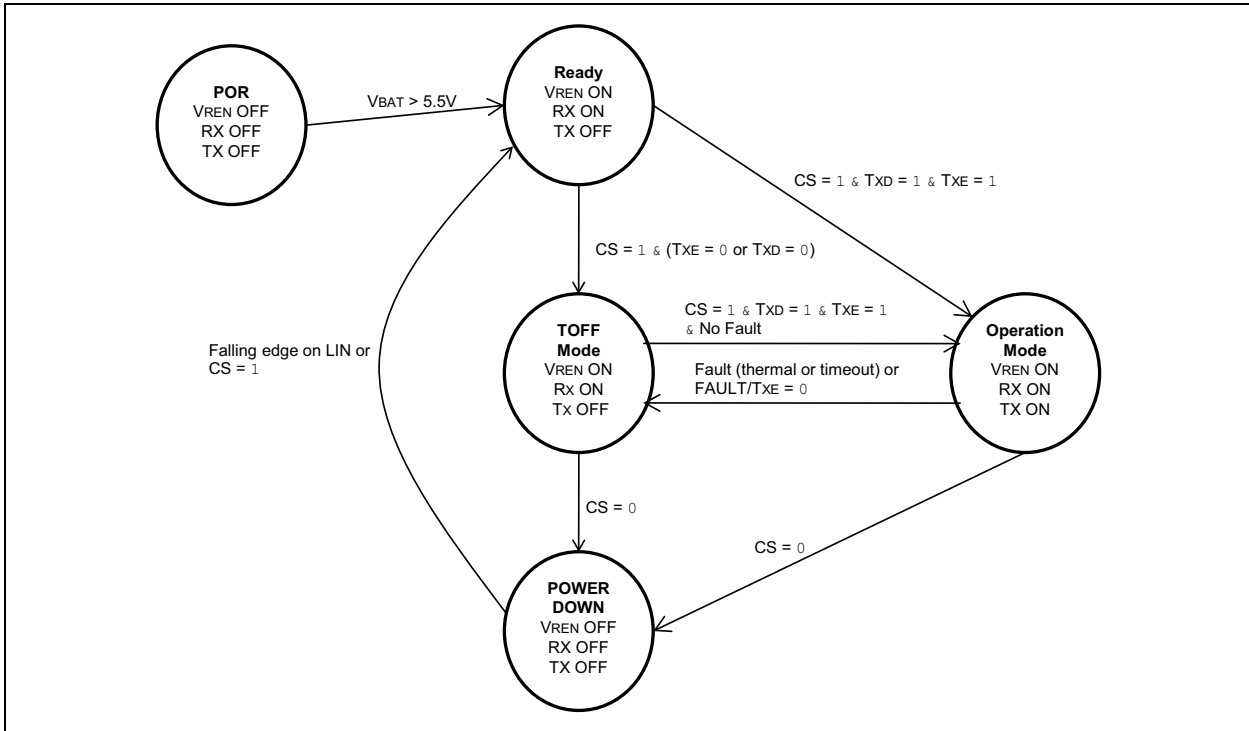


FIGURE 1-4: OPERATIONAL MODES STATE DIAGRAM – MCP2004



MCP2003/4/3A/4A

FIGURE 1-5: OPERATIONAL MODES STATE DIAGRAM – MCP2004A

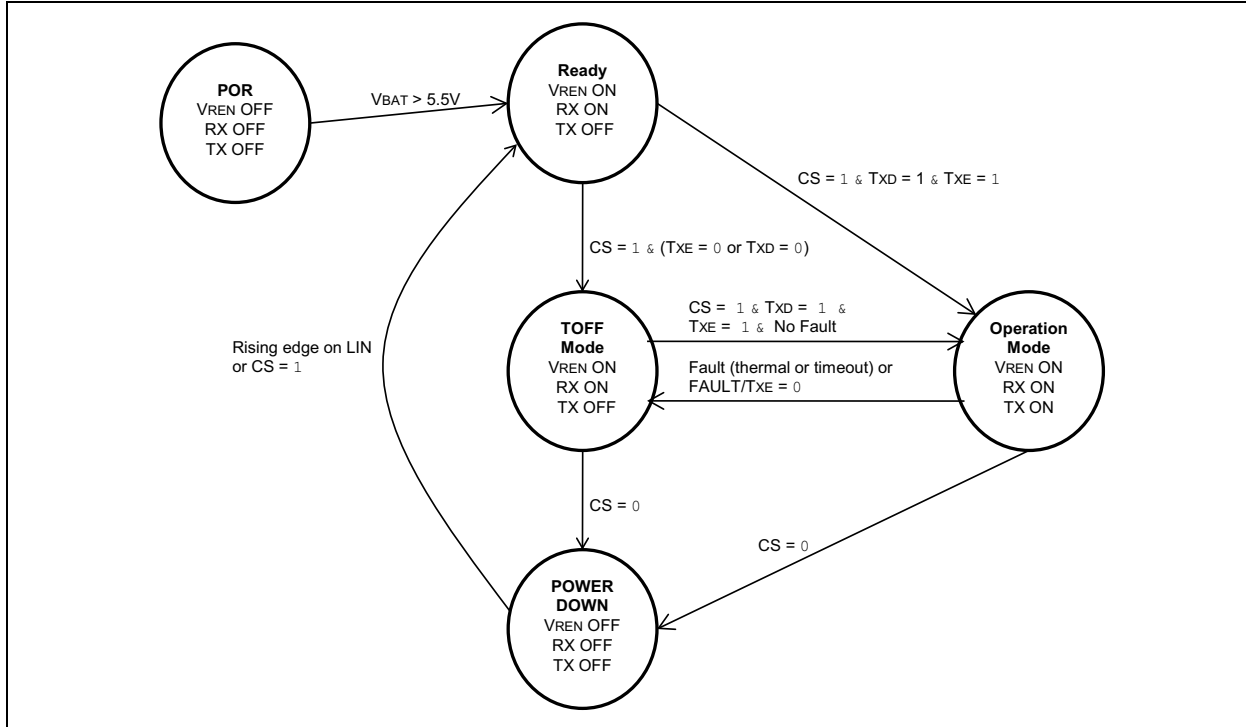
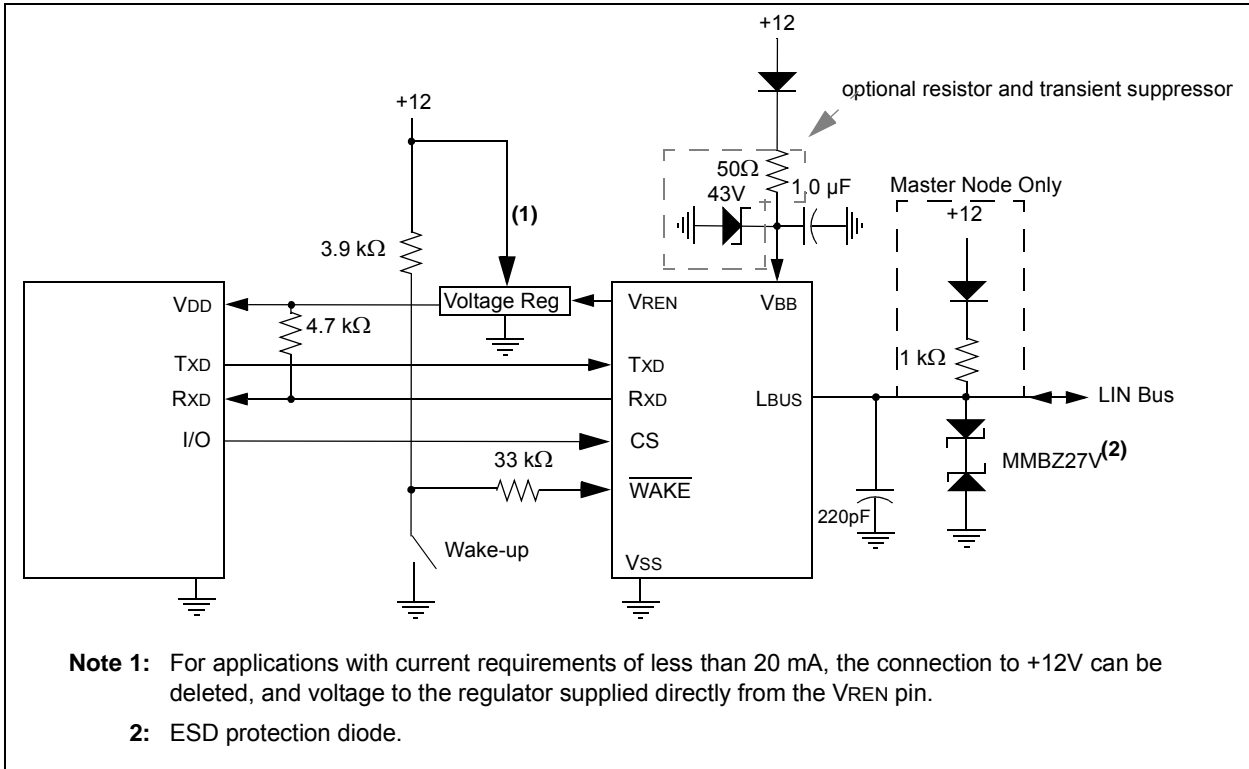


TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

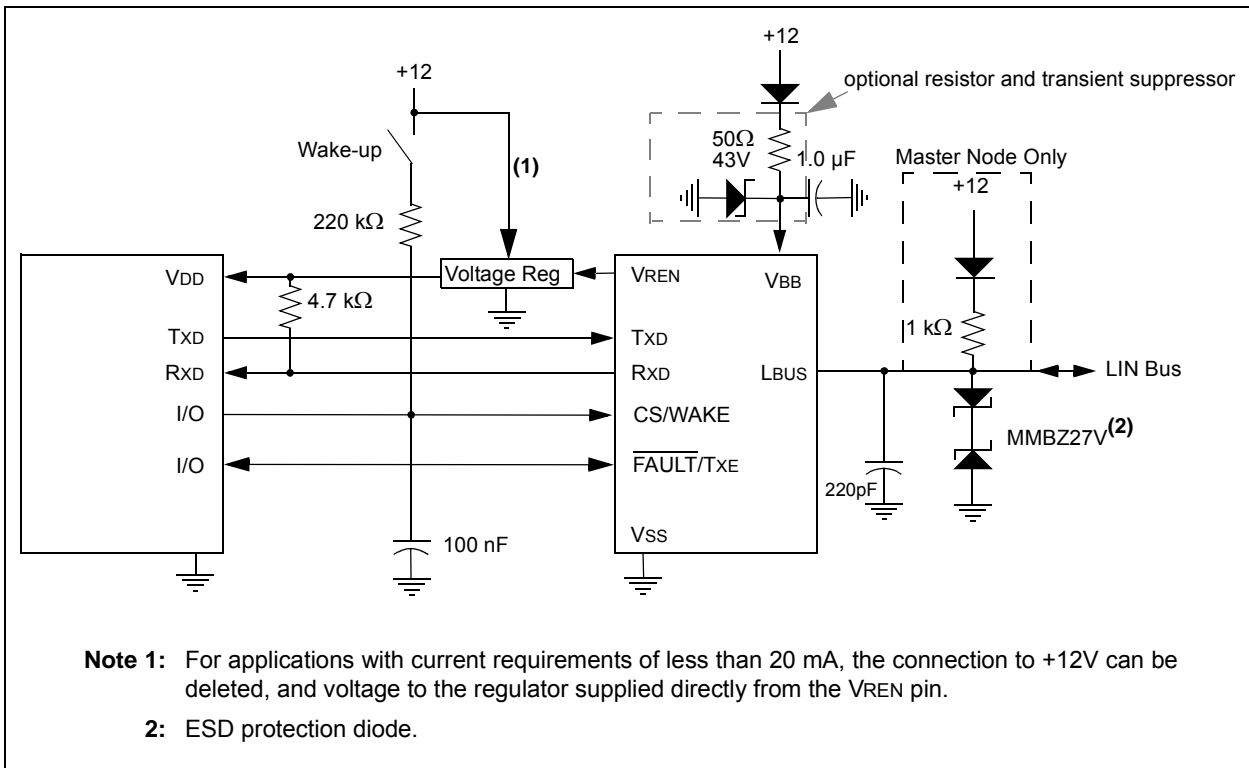
State	Transmitter	Receiver	VREN	Operation	Comments
POR	OFF	OFF	OFF	Check CS, if low then proceed to Ready mode; If high, transitions to either TOFF or Operation mode, depending on TXD (2003/A), or TXD and $\overline{\text{FAULT}}/\text{TXE}$ (2004/A).	$V_{\text{BB}} > V_{\text{BB(MIN)}}$ and Internal Supply stable
Ready	OFF	ON	ON	If CS is high level, then proceed to Operation or TXOFF mode.	Bus Off state
Operation	ON	ON	ON	If CS is low level, then proceed to Power-Down; If $\overline{\text{FAULT}}/\text{TXE}$ low level, then proceed to Transmitter Off mode.	Normal Operation mode
Power-Down	OFF	Activity Detect	OFF	On CS high level, proceed to Ready mode then proceed to either Operation mode or TXOFF. MCP2003/2003A: Falling edge on WAKE will put the device into Ready mode. MCP2003/MCP2004: falling edge on LIN bus will put the device into Ready mode. MCP2003A/MCP2004A: rising edge on LIN bus will put the device into Ready mode.	Low-Power mode
Transmitter Off	OFF	ON	ON	If CS is low level, then proceed to Power-Down mode; If $\overline{\text{FAULT}}/\text{TXE}$ and TXD high, then proceed to Operation mode	$\overline{\text{FAULT}}/\text{TXE}$ only available on MCP2004/2004A

1.4 Typical Applications

EXAMPLE 1-1: TYPICAL MCP2003/2003A APPLICATION

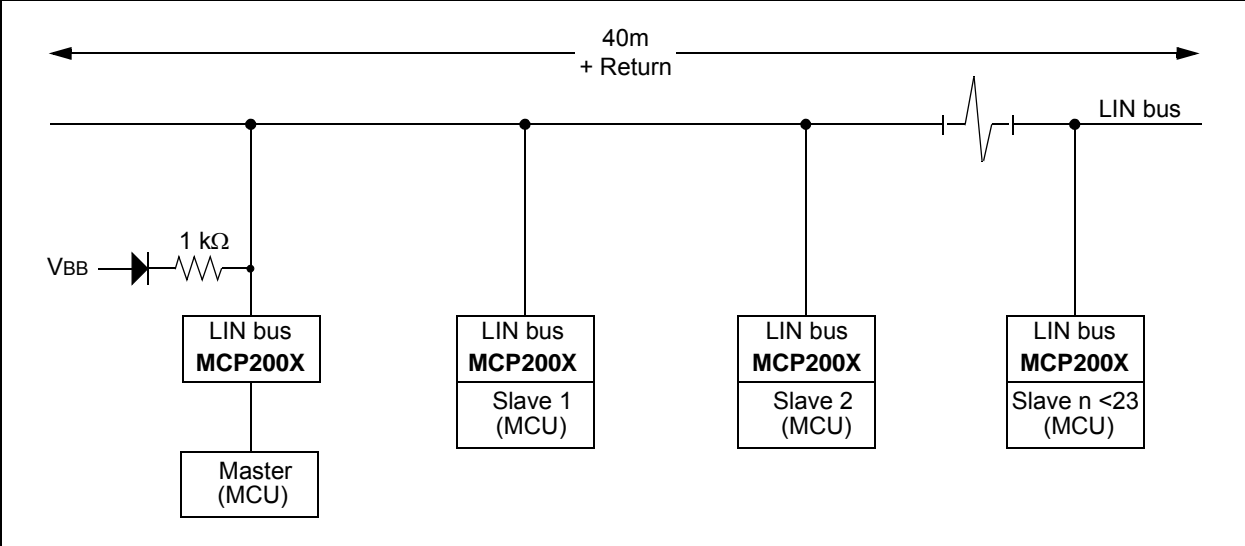


EXAMPLE 1-2: TYPICAL MCP2004/2004A APPLICATION



MCP2003/4/3A/4A

EXAMPLE 1-3: TYPICAL LIN NETWORK CONFIGURATION



1.5 Pin Descriptions

TABLE 1-2: PINOUT DESCRIPTIONS

Pin Name	8-Lead PDIP, SOIC	4x4 DFN	MCP2003/2003A	MCP2004/2004A
			Normal Operation	Normal Operation
RxD	1	1	Receive Data Output (OD), HV tolerant	Receive Data Output (OD), HV tolerant
CS	2	2	Chip Select (TTL), HV tolerant	Chip Select/Local WAKE (TTL), HV tolerant
WAKE (MCP2003/2003A only)	3	3	Wake-up, HV tolerant	Fault Detect Output (OD) Transmitter Enable (TTL) HV tolerant
FAULT/TxE (MCP2004/2004A only)				
TxD	4	4	Transmit Data Input (TTL), HV tolerant	Transmit Data Input (TTL), HV tolerant
Vss	5	5	Ground	Ground
LBUS	6	6	LIN Bus (bidirectional)	LIN Bus (bidirectional)
VBB	7	7	Battery Positive	Battery Positive
VREN	8	8	Voltage Regulator Enable Output	Voltage Regulator Enable Output
EP	—	9	Exposed Thermal Pad. Do not electrically connect or connect to Vss	Exposed Thermal Pad. Do not electrically connect or connect to Vss

Legend: TTL = TTL Input Buffer; OD = Open-Drain Output

1.5.1 RECEIVE DATA OUTPUT (RxD)

The Receive Data Output pin is an open drain (OD) output and follows the state of the LIN pin, except in Power Down mode.

1.5.1.1 RxD Monitoring

The RxD pin is internally monitored. It has to be at a high level (> 2.5V typical) while LBUS is recessive. Otherwise, an internal fault will be created and the device will transition to Transmitter Off mode. On the MCP2004/2004A, the FAULT/TxE pin will be driven low to indicate the Transmitter Off state.

1.5.2 CHIP SELECT (CS)

This is the Chip Select Input pin. An internal pull-down resistor will keep the CS pin low. This is done to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-on Reset and an I/O initialization sequence. The pin must detect a high level to activate the transmitter. An internal Low-Pass filter, with a typical time constant of 10 μ s, prevents unwanted wake-up (or transition to Power Down mode) on glitches.

If CS = 0 when the VBB supply is turned on, the device goes to Ready mode as soon as internal voltages stabilize, and stays there as long as the CS pin is held low (0). In Ready mode, the receiver is on, and the LIN transmitter driver is off.

If CS = 1 when the VBB supply is turned on, the device will proceed to Operation mode, or TXOFF (refer to Figures 1-2 to 1-5), as soon as internal voltages stabilize.

This pin may also be used as a local wake-up input (refer to Example 1-1). In this implementation, the microcontroller I/O controlling the CS should be converted to a high-impedance input allowing the internal pull-down resistor to keep CS low. An external switch, or other source, can then wake-up both the transceiver and the microcontroller (if powered). Refer to Section 1.3 “Modes of Operation”, for detailed operation of CS.

Note: It is not recommended to tie CS high as this can result in the device entering Operation mode before the microcontroller is initialized and may result in unintentional LIN traffic.

1.5.3 WAKE-UP INPUT ($\overline{\text{WAKE}}$)

This pin is only available on the MCP2003/2003A.

The $\overline{\text{WAKE}}$ pin has an internal 800 k Ω pull-up to VBB. A falling edge on the $\overline{\text{WAKE}}$ pin causes the device to wake from Power-Down mode. Upon waking, the MCP2003/3A will enter Ready mode.

MCP2003/4/3A/4A

1.5.4 $\overline{\text{FAULT/TXE}}$

This pin is only available on the MCP2004/2004A. This pin is bidirectional and allows disabling of the transmitter, as well as fault reporting related to disabling the transmitter. This pin is an open-drain output, with states as defined in [Table 1-3](#). The transmitter is disabled whenever this pin is low ('0'), either from an internal Fault condition or by an external

drive. While the transmitter is disabled, the internal 30 k Ω pull-up resistor on the LBUS pin is also disconnected to reduce current.

Note: The $\overline{\text{FAULT/TXE}}$ pin is true ('0') whenever the internal circuits have detected a short or thermal excursion and have disabled the LBUS output driver.

TABLE 1-3: $\overline{\text{FAULT/TXE}}$ TRUTH TABLE

TxD In	RxD Out	LINBUS I/O	Thermal Override	$\overline{\text{FAULT/TXE}}$		Definition
				External Input	Driven Output	
L	H	VBB	OFF	H	L	FAULT , TxD driven low, LBUS shorted to VBB (Note 1)
H	H	VBB	OFF	H	H	OK
L	L	GND	OFF	H	H	OK
H	L	GND	OFF	H	H	OK , data is being received from LBUS
x	x	VBB	ON	H	L	FAULT , Transceiver in thermal shutdown
x	x	VBB	x	L	x	NO FAULT , the CPU is commanding the transceiver to turn off the transmitter driver

Legend: x = don't care.

Note 1: The $\overline{\text{FAULT/TXE}}$ is valid after approximately 25 μs after TXD falling edge. This is to eliminate false fault reporting during bus propagation delays.

1.5.5 TRANSMIT DATA INPUT (TXD)

The Transmit Data Input pin has an internal pull-up. The LIN pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

For extra bus security, TXD is internally forced to '1' whenever the transmitter is disabled regardless of external TXD voltage.

1.5.5.1 TXD Dominant Timeout

If TXD is driven low for longer than approximately 25 ms, the LBUS pin is switched to Recessive mode and the part enters TOFF Mode. This is to prevent the LIN node from permanently driving the LIN Bus dominant. The transmitter is reenabled on TXD rising edge.

1.5.6 GROUND (Vss)

This is the Ground pin.

1.5.7 LIN BUS (LBUS)

The bidirectional LIN Bus pin (LBUS) is controlled by the TXD input. LBUS has a current limited open collector output. To reduce EMI, the edges during the signal changes are slope controlled and include corner rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus, and matches the output signal RXD to follow the state of the LBUS pin.

1.5.7.1 Bus Dominant Timer

The Bus Dominant Timer is an internal timer that deactivates the LBUS transmitter after approximately 25 ms of dominant state on the LBUS pin. The timer is reset on any recessive LBUS state.

The LIN bus transmitter will be reenabled after a recessive state on the LBUS pin as long as CS is high. Disabling can be caused by the LIN bus being externally held dominant, or by TXD being driven low. Additionally, on the MCP2004/2004A, the $\overline{\text{FAULT}}$ pin will be driven low to indicate the Transmitter Off state.

1.5.8 BATTERY (VBB)

This is the Battery Positive Supply Voltage pin.

1.5.9 VOLTAGE REGULATOR ENABLE OUTPUT (VREN)

This is the External Voltage Regulator Enable pin. Open source output is pulled high to VBB in all modes, except Power-Down.

1.5.10 EXPOSED THERMAL PAD (EP)

Do not electrically connect, or connect to Vss.

1.6 MCP2003/4 and MCP2003A/4A Difference Details

The differences between the MCP2003/4 and the MCP2003/4A devices are isolated to the wake-up functionality. The changes were implemented to make the device more robust to LIN bus conditions, outside of the normal operating conditions. The MCP2003/4 will wake-up from Power-Down mode during any LIN falling edge held low longer than 20 μs .

In the case where a LIN system is designed to minimize stand-by current by disconnecting all bus pull-ups resistors (including the external master pull-up resistor to V_{BB}), the original MCP2003/4 could wake-up, if the floating bus drifted to a valid low level. The MCP2003/4A revisions were modified to require a rising edge after a valid low level. This will prevent an undesired system wake-up in this scenario, while maintaining functional capability with the original version.

It should be noted that the original MCP2003/4 meets all LIN transceiver specification requirements and modules can be designed to pass all LIN system requirements. However, when all bus pull-up resistors are disconnected, the MCP2003/4 requires the module designer to write firmware to monitor the LIN Bus after any wake-up event to prevent the transceiver from automatically transitioning from Ready mode to Operational mode.

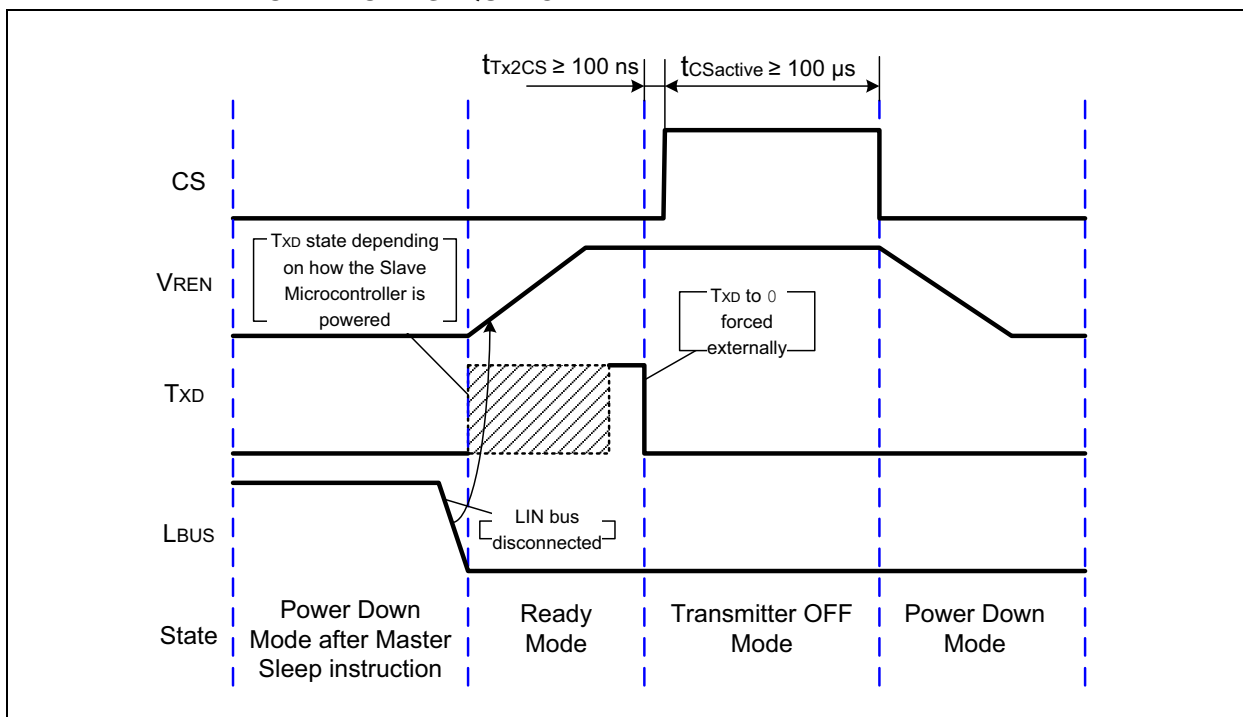
If the MCP2003/4 is placed into Operational mode, V_{BB} to L_{BUS} pull-up resistor is automatically connected, which will raise the LIN bus to a recessive level; then putting the device to Power-Down mode may cause L_{BUS} to be floating, and thus wake-up all bus nodes. To prevent this, the designer should ensure T_{XD} (MCP2003) or T_{XE} (MCP2004) is held low until valid bus activity is verified (see Figure 1-6). This will ensure the transceiver transitions from Ready mode to Transmitter Off mode, until bus activity can be verified.

In the case of valid bus activity, the transceiver can shift to Operation mode, while if there is no bus activity, the device can be again placed into Power Down. The design practices needed to accomplish this are fully detailed in Tech Brief TB3067 – “MCP2003 Power-Down Mode and Wake-Up Handling in Case of LIN Bus Loss” (DS93067).

The revised MCP2003/4A devices now eliminate the need for firmware to prevent system wide wake-up. The revised devices now require a longer valid bus low (see updated t_{BDB} value in Section 2.3 “DC Specifications” and Figure 2-7), which enables a rising edge detect circuit. The device will now only wake-up after a rising edge, following a low longer than t_{BDB}. While the module designer can still hold T_{XD} (MCP2003) or T_{XE} (MCP2004) low during wake-up, to enter Transmitter Off mode from Ready mode, it is not required to prevent an advertent system wake-up.

In addition to the longer t_{BDB} value, the time from wake-up detect to V_{REN} enable is shortened as documented in Section 2.3 “DC Specifications”.

FIGURE 1-6: MCP2003/2004 SWITCHING TIMING DIAGRAM FOR THE FORCED POWER-DOWN MODE SEQUENCE



MCP2003/4/3A/4A

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V _{IN} DC Voltage on RXD, TXD, $\overline{\text{FAULT}}/\text{TXE}$, CS	-0.3 to +43V
V _{IN} DC Voltage on $\overline{\text{WAKE}}$ and V _{REN}	-0.3 to +V _{BB}
V _{BB} Battery Voltage, continuous, non-operating (Note 1)	-0.3 to +40V
V _{BB} Battery Voltage, non-operating (LIN bus recessive) (Note 2)	-0.3 to +43V
V _{BB} Battery Voltage, transient ISO 7637 Test 1	-200V
V _{BB} Battery Voltage, transient ISO 7637 Test 2a	+150V
V _{BB} Battery Voltage, transient ISO 7637 Test 3a	-300V
V _{BB} Battery Voltage, transient ISO 7637 Test 3b	+200V
V _{LBUS} Bus Voltage, continuous	-18 to +40V
V _{LBUS} Bus Voltage, transient (Note 3)	-27 to +43V
I _{LBUS} Bus Short Circuit Current Limit	200 mA
ESD protection on LIN, V _{BB} , $\overline{\text{WAKE}}$ (IEC 61000-4-2) (Note 4)	±8 KV
ESD protection on LIN, V _{BB} (Human Body Model) (Note 5)	±8 KV
ESD protection on all other pins (Human Body Model) (Note 5)	±4 KV
ESD protection on all pins (Charge Device Model) (Note 6)	±2 KV
ESD protection on all pins (Machine Model) (Note 7)	±200V
Maximum Junction Temperature	150°C
Storage Temperature	-65 to +150°C

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device, at those or any other conditions above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: LIN 2.x compliant specification.

2: SAE J2602 compliant specification.

3: ISO 7637/1 load dump compliant (t < 500 ms).

4: According to IEC 61000-4-2, 330 ohm, 150 pF and Transceiver EMC Test Specifications [2] to [4]. For $\overline{\text{WAKE}}$ pin to meet the specification, series resistor must be in place (refer to [Example 1-2](#)).

5: According to AEC-Q100-002/JESD22-A114.

6: According to AEC-Q100-011B.

7: According to AEC-Q100-003/JESD22-A115.

2.2 Nomenclature Used in This Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

LIN 2.1 Name	Term used in the following tables	Definition
VBAT	<i>not used</i>	ECU operating voltage
VSUP	V _{BB}	Supply voltage at device pin
IBUS_LIM	ISC	Current Limit of driver
VBUSREC	V _{IH} (LBUS)	Recessive state
VBUSDOM	V _{IL} (LBUS)	Dominant state

2.3 DC Specifications

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $30.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$					
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power						
V _{BB} Quiescent Operating Current	IBBQ	—	90	150	μA	Operating Mode, bus recessive (Note 1)
V _{BB} Transmitter-off Current	IBBTO	—	75	120	μA	Transmitter off, bus recessive (Note 1)
V _{BB} Power-Down Current	IBBPD	—	5	15	μA	
V _{BB} Current with V _{SS} Floating	IBBNOGND	-1	—	1	mA	V _{BB} = 12V, GND to V _{BB} , V _{LIN} = 0-27V
Microcontroller Interface						
High-Level Input Voltage (TXD, FAULT/TXE)	V _{IH}	2.0	—	30	V	
Low-Level Input Voltage (TXD, FAULT/TXE)	V _{IL}	-0.3	—	0.8	V	
High-Level Input Current (TXD, FAULT/TXE)	I _{IH}	-2.5	—	—	μA	Input voltage = 4.0V
Low-Level Input Current (TXD, FAULT/TXE)	I _{IL}	-10	—	—	μA	Input voltage = 0.5V
High-Level Voltage (VREN)	V _{HVREN}	-0.3	—	V _{BB} +0.3	V	
High-Level Output Current (VREN)	I _{HVREN}	-40	—	-10	mA	Output voltage = V _{BB} -0.5V
		-125	—	-35		Output voltage = V _{BB} -2.0V
High-Level Input Voltage (CS)	V _{IH}	2.0	—	30	V	Through a current limiting resistor
Low-Level Input Voltage (CS)	V _{IL}	-0.3	—	0.8	V	
High-Level Input Current (CS)	I _{IH}	—	—	10.0	μA	Input voltage = 4.0V
Low-Level Input Current (CS)	I _{IL}	—	—	5.0	μA	Input voltage = 0.5V
Low-Level Input Voltage (WAKE)	V _{IL}	V _{BB} - 4.0V	—	—	V	
Low-Level Output Voltage (RXD)	V _{OL}	—	—	0.4	V	I _{IN} = 2 mA
High-Level Output Current (RXD)	I _{OH}	-1	—	-1	μA	V _{LIN} = V _{BB} , V _{RXD} = 5.5V

Note 1: Internal current limited. 2.0 ms maximum recovery time ($R_{L_{BUS}} = 0\Omega$, $T_X = 0.4 V_{REG}$, $V_{L_{BUS}} = V_{BB}$).

2: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

MCP2003/4/3A/4A

2.3 DC Specifications (Continued)

DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $30.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$				
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Bus Interface						
High-Level Input Voltage	$V_{IH}(L_{BUS})$	$0.6 V_{BB}$	—	—	V	Recessive state
Low-Level Input Voltage	$V_{IL}(L_{BUS})$	-8	—	$0.4 V_{BB}$	V	Dominant state
Input Hysteresis	V_{HYS}	—	—	$0.175 V_{BB}$	V	$V_{IH}(L_{BUS}) - V_{IL}(L_{BUS})$
Low-Level Output Current	$I_{OL}(L_{BUS})$	40	—	200	mA	Output voltage = $0.1 V_{BB}$, $V_{BB} = 12V$
High-Level Output Current	$I_{OH}(L_{BUS})$	—	—	20	μA	
Pull-up Current on Input	$I_{PU}(L_{BUS})$	5	—	180	μA	~30 k Ω internal pull-up @ $V_{IH}(L_{BUS}) = 0.7 V_{BB}$
Short Circuit Current Limit	I_{SC}	50	—	200	mA	(Note 1)
High-Level Output Voltage	$V_{OH}(L_{BUS})$	$0.9 V_{BB}$	—	V_{BB}	V	
Driver Dominant Voltage	$V_{_LOSUP}$	—	—	1.2	V	$V_{BB} = 7V$, $R_{LOAD} = 500\Omega$
Driver Dominant Voltage	$V_{_HISUP}$	—	—	2.0	V	$V_{BB} = 18V$, $R_{LOAD} = 500\Omega$
Driver Dominant Voltage	$V_{_LOSUP} - 1K$	0.6	—	—	V	$V_{BB} = 7V$, $R_{LOAD} = 1 k\Omega$
Driver Dominant Voltage	$V_{_HISUP} - 1K$	0.8	—	—	V	$V_{BB} = 18V$, $R_{LOAD} = 1 k\Omega$
Input Leakage Current (at the receiver during dominant bus level)	$I_{BUS_PAS_DOM}$	-1	-0.4	—	mA	Driver off, $V_{BUS} = 0V$, $V_{BB} = 12V$
Input Leakage Current (at the receiver during recessive bus level)	$I_{BUS_PAS_REC}$	—	12	20	μA	Driver off, $8V < V_{BB} < 18V$ $8V < V_{BUS} < 18V$ $V_{BUS} \geq V_{BB}$
Leakage Current (disconnected from ground)	$I_{BUS_NO_GND}$	-10	1.0	+10	μA	$GND_{DEVICE} = V_{BB}$, $0V < V_{BUS} < 18V$, $V_{BB} = 12V$
Leakage Current (disconnected from V_{BB})	$I_{BUS_NO_V_{BB}}$	—	—	10	μA	$V_{BB} = GND$, $0 < V_{BUS} < 18V$, (Note 2)
Receiver Center Voltage	V_{BUS_CNT}	$0.475 V_{BB}$	$0.5 V_{BB}$	$0.525 V_{BB}$	V	$V_{BUS_CNT} = (V_{IL}(L_{BUS}) + V_{IH}(L_{BUS}))/2$
Slave Termination	R_{SLAVE}	20	30	47	k Ω	
Capacitance of Slave Node	C_{SLAVE}	—	—	50	pF	

Note 1: Internal current limited. 2.0 ms maximum recovery time ($R_{L_{BUS}} = 0\Omega$, $T_X = 0.4 V_{REG}$, $V_{L_{BUS}} = V_{BB}$).

2: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.4 AC Specifications

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, all limits are specified for V _{BB} = 6.0V to 27.0V; T _A = -40°C to +125°C				
Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Bus Interface – Constant Slope Time Parameters						
Slope Rising and Falling Edges	t _{SLOPE}	3.5	—	22.5	μs	7.3V ≤ V _{BB} ≤ 18V
Propagation Delay of Transmitter	t _{TRANSPD}	—	—	4.0	μs	t _{TRANSPD} = max (t _{TRANSPDR} or t _{TRANSPDF})
Propagation Delay of Receiver	t _{TRECPD}	—	—	6.0	μs	t _{TRECPD} = max (t _{TRECPDR} or t _{TRECPDF})
Symmetry of Propagation Delay of Receiver Rising Edge w.r.t. Falling Edge	t _{TRECSYM}	-2.0	—	2.0	μs	t _{TRECSYM} = max (t _{TRECPDF} – t _{TRECPDR}) R _{RXD} 2.4Ω to V _{CC} , C _{RXD} 20 pF
Symmetry of Propagation Delay of Transmitter Rising Edge w.r.t. Falling Edge	t _{TRANSSYM}	-2.0	—	2.0	μs	t _{TRANSSYM} = max (t _{TRANSPDF} - t _{TRANSPDR})
Time to Sample of $\overline{\text{FAULT}}/\text{TXE}$ for Bus Conflict Reporting	t _{FAULT}	—	—	32.5	μs	t _{FAULT} = max (t _{TRANSPD} + t _{SLOPE} + t _{TRECPD})
Duty Cycle 1 @20.0 kbit/sec		0.396	—	—	—	CBUS; RBUS conditions: 1 nF; 1 kΩ 6.8 nF; 660Ω 10 nF; 500Ω T _{HREC} (MAX) = 0.744 x V _{BB} , T _{HDOM} (MAX) = 0.581 x V _{BB} , V _{BB} = 7.0V – 18V; t _{BIT} = 50 μs D1 = t _{BUS_REC} (MIN)/2 x t _{BIT})
Duty Cycle 2 @20.0 kbit/sec		—	—	0.581	—	CBUS; RBUS conditions: 1 nF; 1 kΩ 6.8 nF; 660Ω 10 nF; 500Ω T _{HREC} (MAX) = 0.284 x V _{BB} , T _{HDOM} (MAX) = 0.422 x V _{BB} , V _{BB} = 7.6V – 18V; t _{BIT} = 50 μs D2 = t _{BUS_REC} (MAX)/2 x t _{BIT})
Duty Cycle 3 @10.4 kbit/sec		0.417	—	—	—	CBUS; RBUS conditions: 1 nF; 1 kΩ 6.8 nF; 660Ω 10 nF; 500Ω T _{HREC} (MAX) = 0.778 x V _{BB} , T _{HDOM} (MAX) = 0.616 x V _{BB} , V _{BB} = 7.0V – 18V; t _{BIT} = 96 μs D3 = t _{BUS_REC} (MIN)/2 x t _{BIT})
Duty Cycle 4 @10.4 kbit/sec		—	—	0.590	—	CBUS; RBUS conditions: 1 nF; 1 kΩ 6.8 nF; 660Ω 10 nF; 500Ω T _{HREC} (max) = 0.251 x V _{BB} , T _{HDOM} (MAX) = 0.389 x V _{BB} , V _{BB} = 7.6V – 18V; t _{BIT} = 96 μs D4 = t _{BUS_REC} (MAX)/2 x t _{BIT})
Wake-up Timing						
Bus Activity Debounce time	t _{BDB}	5	—	20	μs	MCP2003/2004
		30	70	125	μs	MCP2003A/2004A
Bus Activity to V _{REN} on	t _{BACTVE}	35	—	150	μs	MCP2003/2004
		10	30	90	μs	MCP2003A/2004A
WAKE to V _{REN} on	t _{WAKE}	—	—	150	μs	
Chip Select to V _{REN} on	t _{CSOR}	—	—	150	μs	V _{REN} floating
Chip Select to V _{REN} off	t _{CSPD}	—	—	80	μs	V _{REN} floating

MCP2003/4/3A/4A

2.5 Thermal Specifications

Parameter	Symbol	Typ.	Max.	Units	Test Conditions
Recovery Temperature	$\theta_{RECOVERY}$	+140	—	°C	
Shutdown Temperature	$\theta_{SHUTDOWN}$	+150	—	°C	
Short Circuit Recovery Time	t_{THERM}	1.5	5.0	ms	
Thermal Package Resistances					
Thermal Resistance, 8L-DFN	θ_{JA}	35.7	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	149.5	—	°C/W	

Note 1: The maximum power dissipation is a function of T_{JMAX} , θ_{JA} and ambient temperature T_A . The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A) \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the device will go into thermal shutdown.

2.6 Typical Performance Curves

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{BB} = 6.0V$ to $18.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$.

FIGURE 2-1: TYPICAL IBBQ

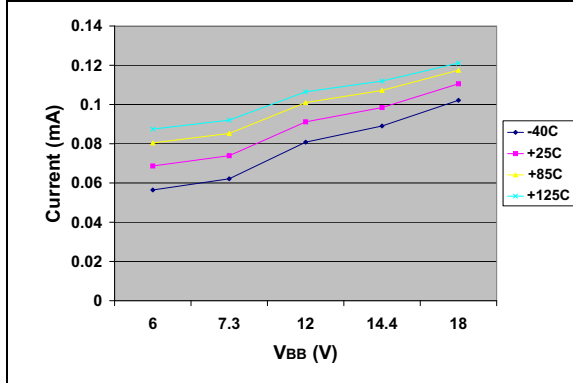


FIGURE 2-3: TYPICAL IBBTO

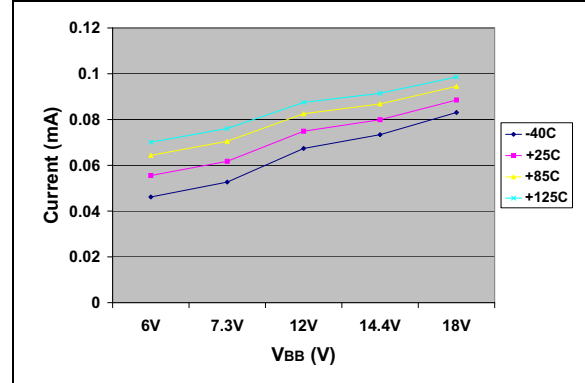
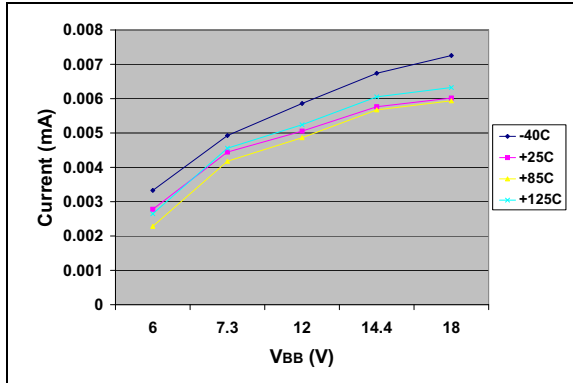


FIGURE 2-2: TYPICAL IBBPD



MCP2003/4/3A/4A

2.7 Timing Diagrams and Specifications

FIGURE 2-4: BUS TIMING DIAGRAM

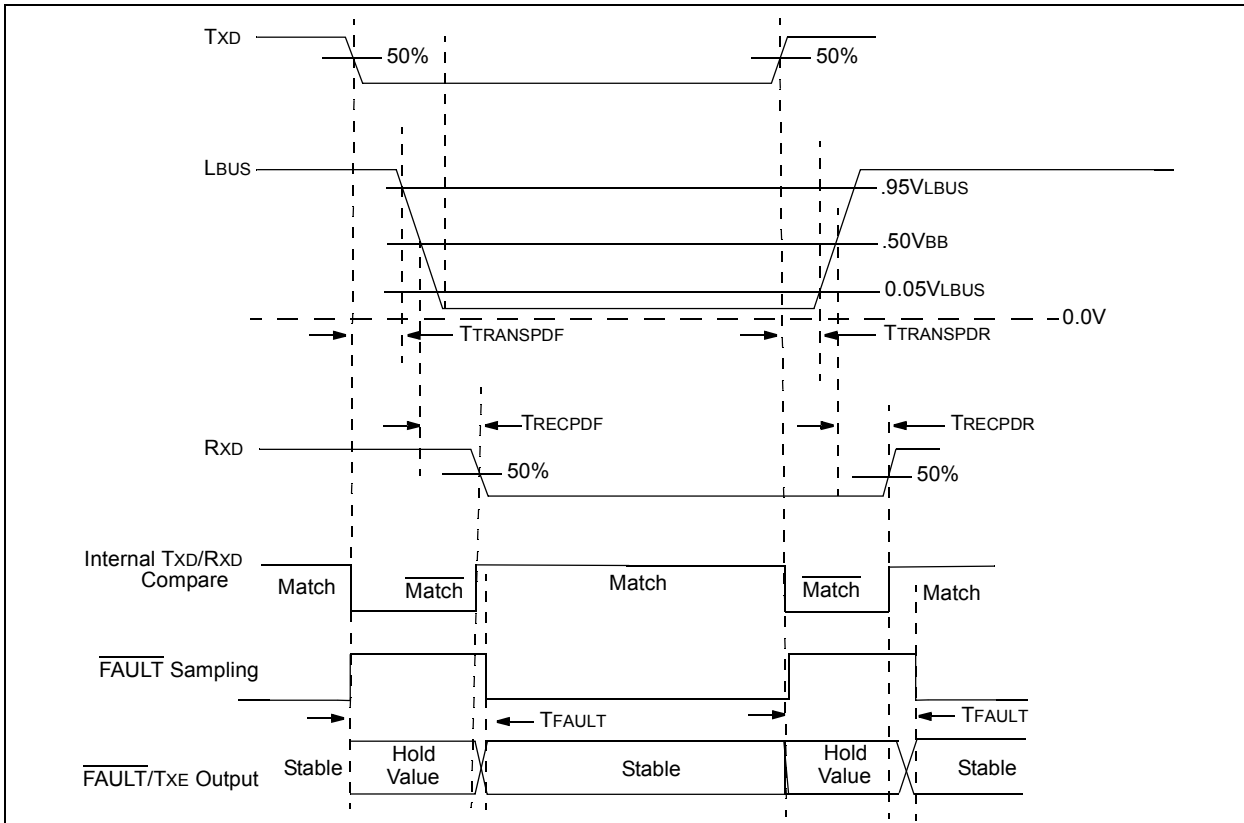


FIGURE 2-5: CS TO VREN TIMING DIAGRAM

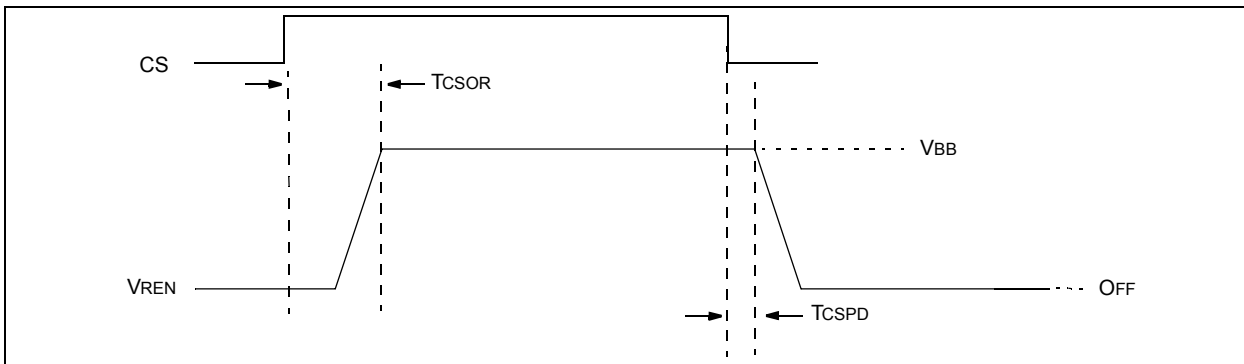


FIGURE 2-6: MCP2003/4 REMOTE WAKE-UP

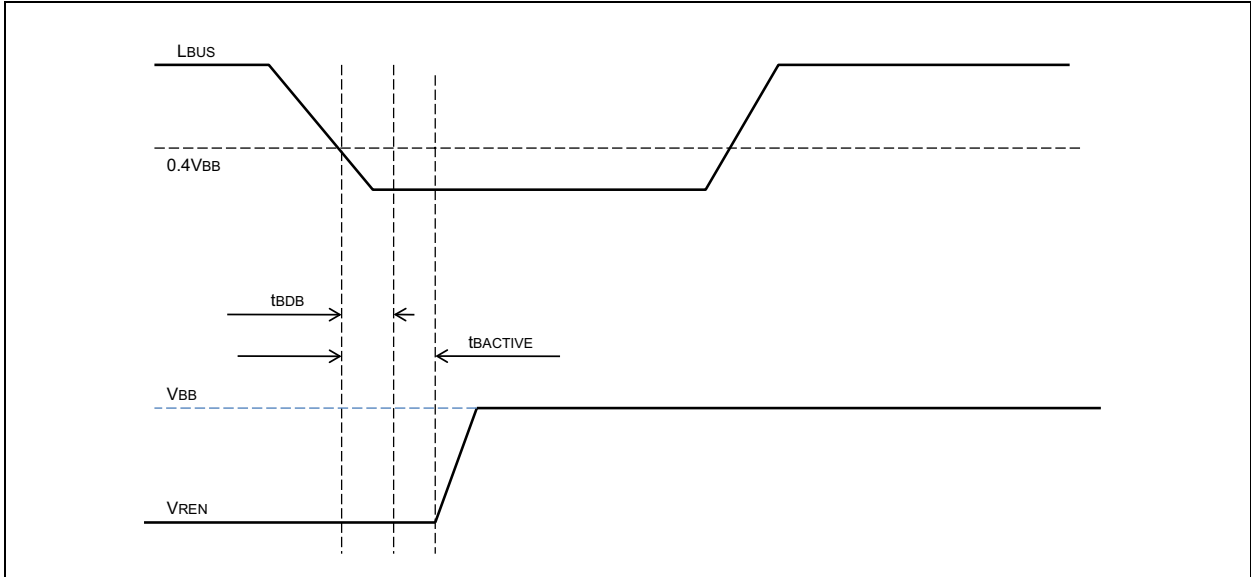
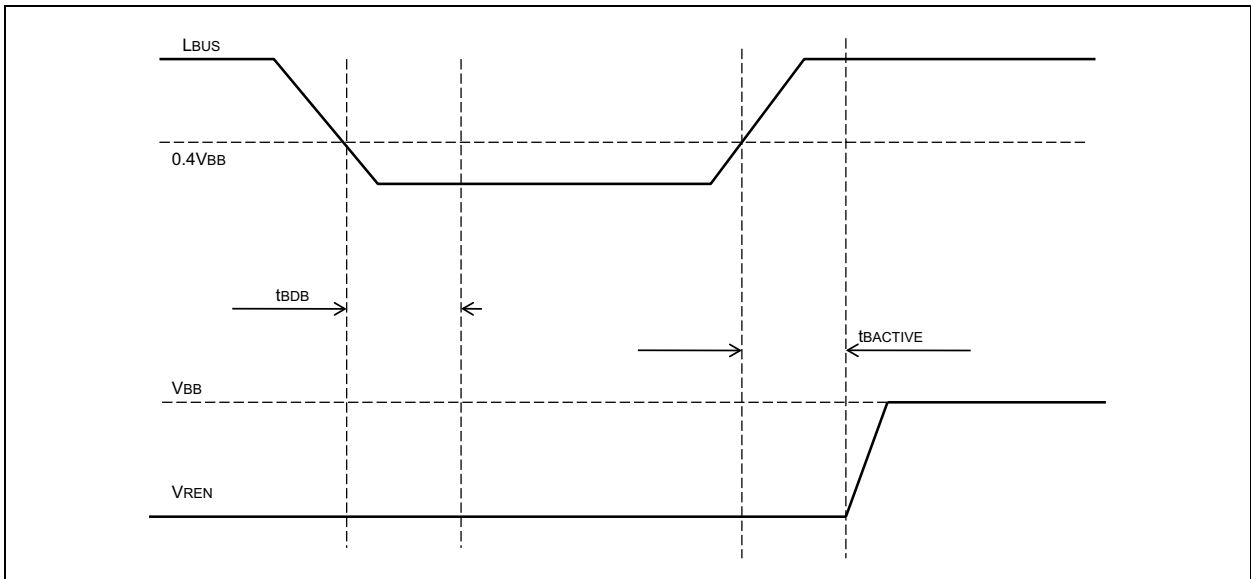


FIGURE 2-7: MCP2003A/4A REMOTE WAKE-UP

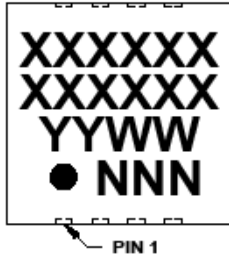


MCP2003/4/3A/4A

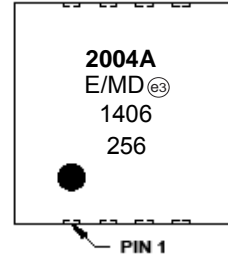
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

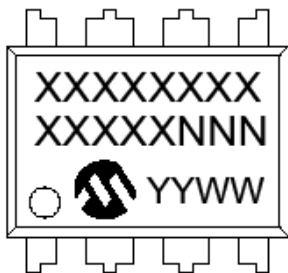
8-Lead DFN (4x4)



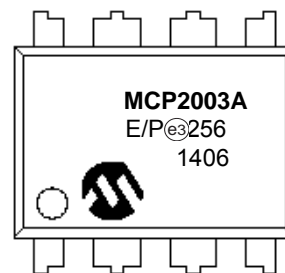
Examples:



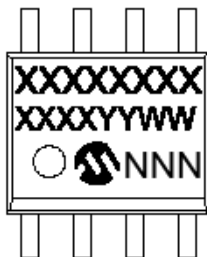
8-Lead PDIP (300 mil)



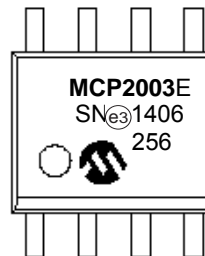
Examples:



8-Lead SOIC (150 mil)



Examples:

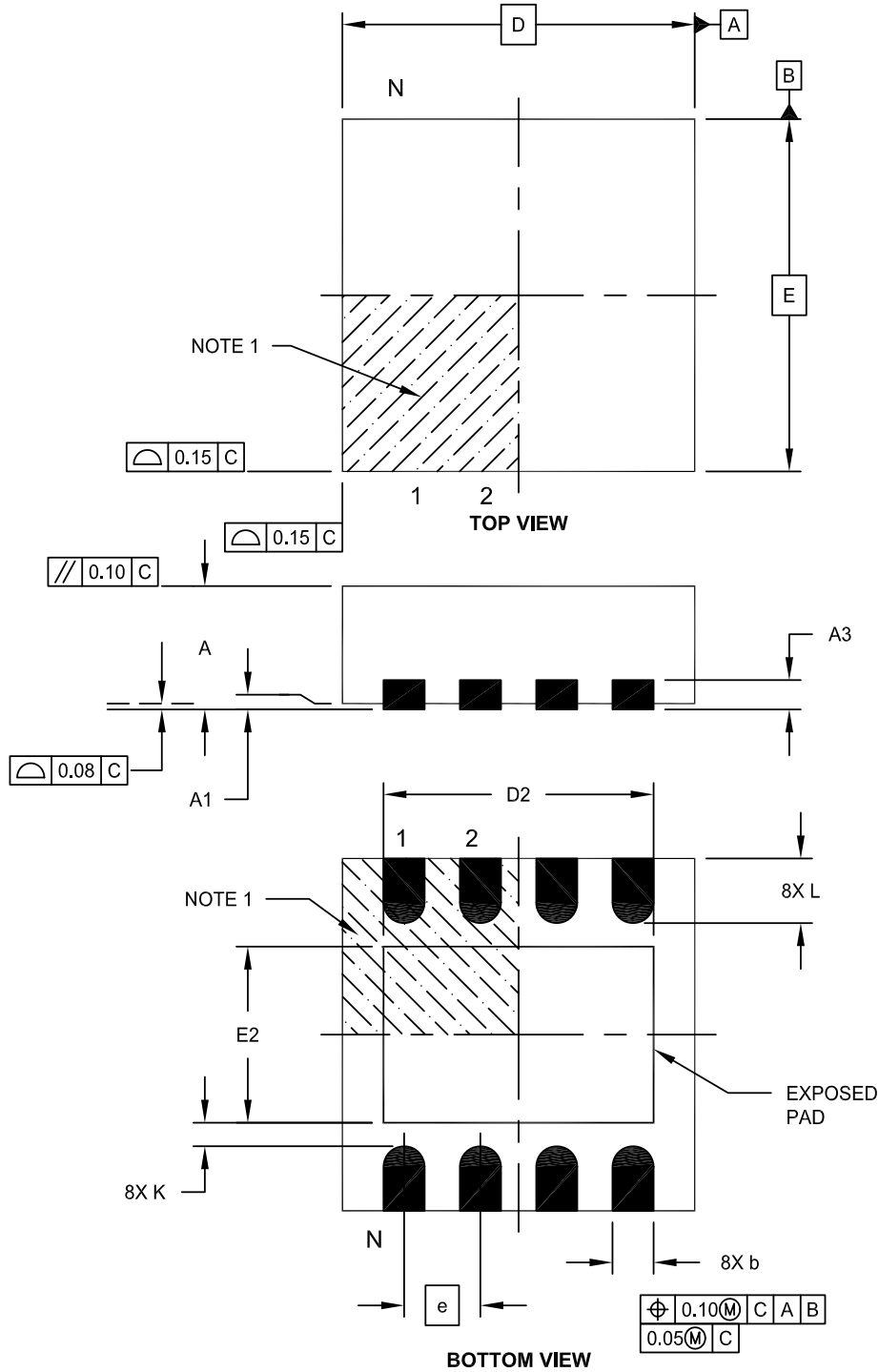


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

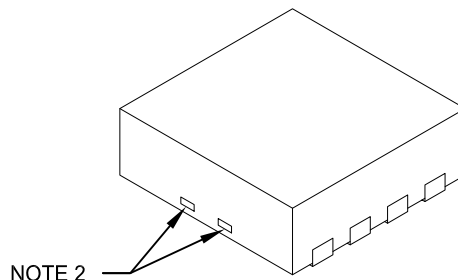


Microchip Technology Drawing C04-131E Sheet 1 of 2

MCP2003/4/3A/4A

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.80 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Width	E	4.00 BSC		
Exposed Pad Length	D2	3.40	3.50	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

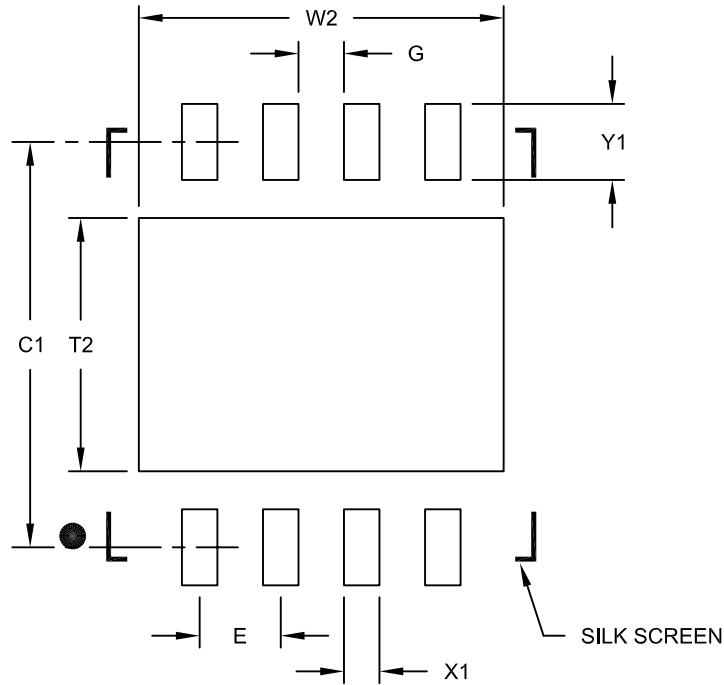
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

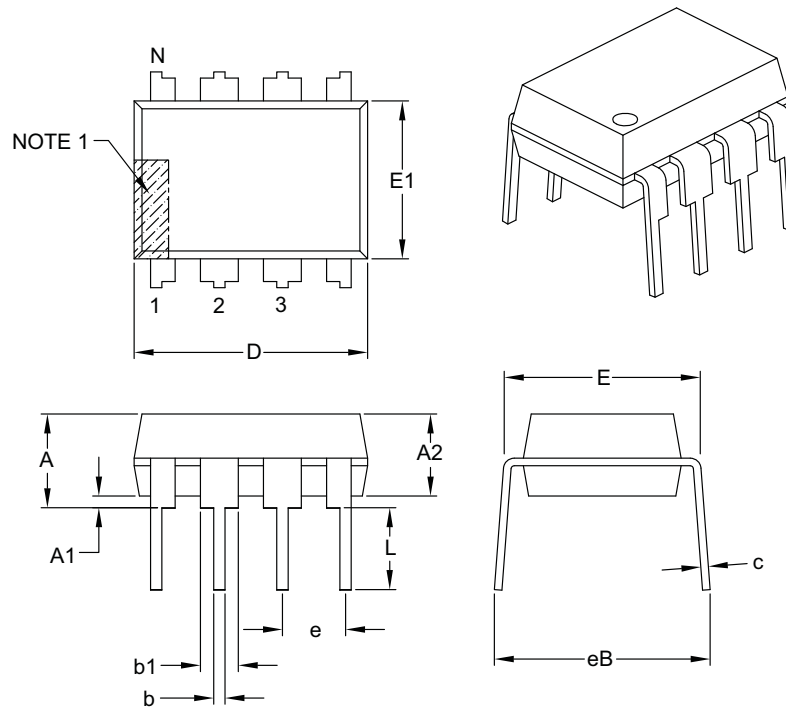
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

MCP2003/4/3A/4A

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

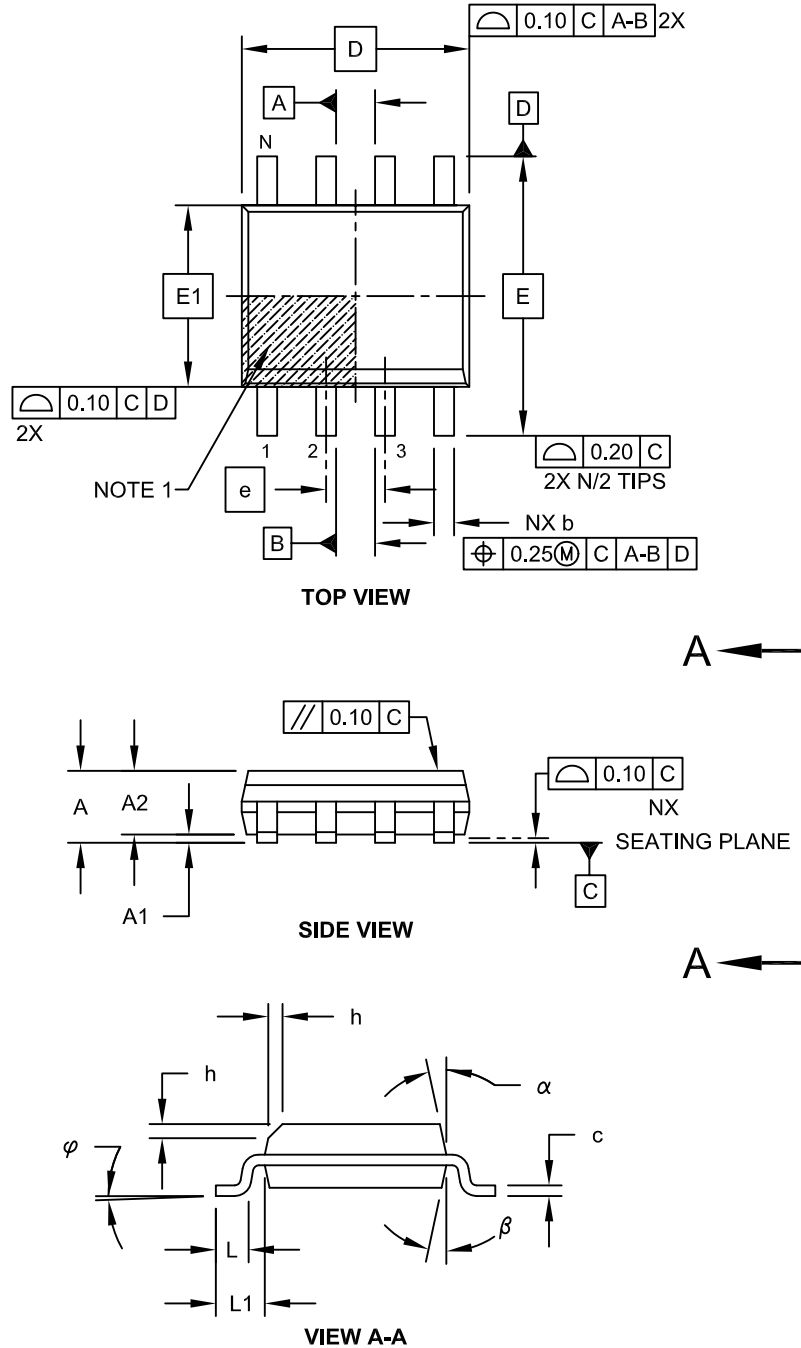
- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

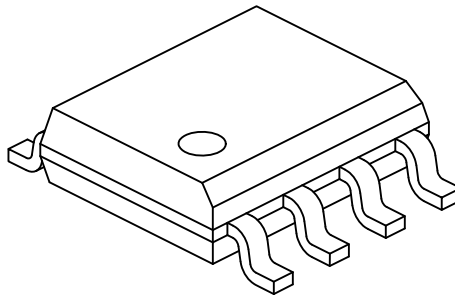


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

MCP2003/4/3A/4A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		1.27 BSC		
Overall Height	A		-	-	1.75
Molded Package Thickness	A2		1.25	-	-
Standoff §	A1		0.10	-	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		4.90 BSC		
Chamfer (Optional)	h		0.25	-	0.50
Foot Length	L		0.40	-	1.27
Footprint	L1		1.04 REF		
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.17	-	0.25
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

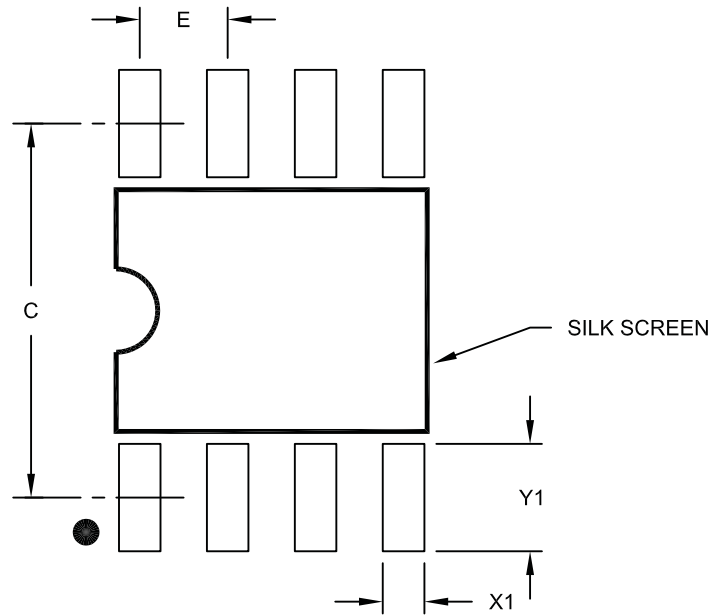
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

MCP2003/4/3A/4A

NOTES:

APPENDIX A: REVISION HISTORY

Revision F (November 2014)

The following is the list of modifications:

1. Updated typical application circuits with values used during ESD tests.

Revision E (October 2013)

The following is the list of modifications:

2. Added additional specification for IHVREN in [Section 2.3 “DC Specifications”](#).
3. Clarified wake-up on LBUS functionality.
4. Added RXD monitoring description.

Revision D (December 2011)

The following is the list of modifications:

5. Added the MCP2003A and MCP2004A devices and related information throughout the document.
6. Updated Figures 1.2, 1.3, 1.4, 1.5, 2.6, 2.7.

Revision C (August 2010)

The following is the list of modifications:

1. Updated all references of Sleep mode to Power-Down mode, and updated the Max. parameter for Duty Cycle 2 in [Section 2.4 “AC Specifications”](#).

Revision B (July 2010)

The following is the list of modifications:

1. Added [Section 2.2 “Nomenclature Used in This Document”](#), and added the “Capacitance of Slave Node” parameter to [Section 2.3 “DC Specifications”](#).

Revision A (March 2010)

- Original Release of this Document.

MCP2003/4/3A/4A

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	Examples:
Device	Temperature Range	Package	
<p>Device:</p> <p>MCP2003: LIN Transceiver, with $\overline{\text{WAKE}}$ pins, wake-up on falling edge of L_{BUS}</p> <p>MCP2003T: LIN Transceiver, with $\overline{\text{WAKE}}$ pins, wake-up on falling edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)</p> <p>MCP2003A: LIN Transceiver, with $\overline{\text{WAKE}}$ pins, wake-up on rising edge of L_{BUS}</p> <p>MCP2003AT: LIN Transceiver, with $\overline{\text{WAKE}}$ pins, wake-up on rising edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)</p> <p>MCP2004: LIN Transceiver with $\overline{\text{FAULT/TxE}}$ pins, wake-up on falling edge of L_{BUS}</p> <p>MCP2004T: LIN Transceiver with $\overline{\text{FAULT/TxE}}$ pins, wake-up on falling edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)</p> <p>MCP2004A: LIN Transceiver with $\overline{\text{FAULT/TxE}}$ pins, wake-up on rising edge of L_{BUS}</p> <p>MCP2004AT: LIN Transceiver with $\overline{\text{FAULT/TxE}}$ pins, wake-up on rising edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)</p>			<p>a) MCP2003A-E/MD: Extended Temperature, 8L-DFN package</p> <p>b) MCP2003A-E/P: Extended Temperature, 8L-PDIP package</p> <p>c) MCP2003A-E/SN: Extended Temperature, 8L-SOIC package</p> <p>d) MCP2003AT-E/MD: Tape and Reel, Extended Temperature, 8L-DFN package</p> <p>e) MCP2003AT-E/SN: Tape and Reel, Extended Temperature, 8L-SOIC package</p>
<p>Temperature Range: E = -40°C to +125°C</p>			<p>a) MCP2004-E/MD: Extended Temperature, 8L-DFN package</p> <p>b) MCP2004-E/P: Extended Temperature, 8L-PDIP package</p> <p>c) MCP2004A-E/SN: Extended Temperature, 8L-SOIC package</p> <p>d) MCP2004AT-E/MD: Tape and Reel, Extended Temperature, 8L-DFN package</p> <p>e) MCP2004AT-E/SN: Tape and Reel, Extended Temperature, 8L-SOIC package</p>
<p>Package:</p> <p>MD = Plastic Dual Flat, No Lead Package - 4x4x0.9mm Body, 8-lead</p> <p>P = Plastic Dual In-Line - 300 mil Body, 8-lead</p> <p>SN = Plastic Small Outline - Narrow 3.90mm Body, 8-lead</p>			

MCP2003/4/3A/4A

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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