Low Harmonic Distortion, 32-Channel, High Voltage Analog Switch Relay Replacement IC

Features

- 32-channel high voltage analog switch
- 2:1 multiplexer/demultiplexer
- Enable control for all-OFF state
- 3.3 or 5.0V CMOS input logic level
- HVCMOS technology for high performance
- Very low quiescent power dissipation, 10µA
- Low parasitic capacitance
- DC to 50MHz analog signal frequency
- -60dB typical OFF-isolation at 5.0MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Flexible operating supply voltages
- 56-Lead 8x8 QFN package

Applications

- Electromechanical relay replacement in medical ultrasound probes.

General Description

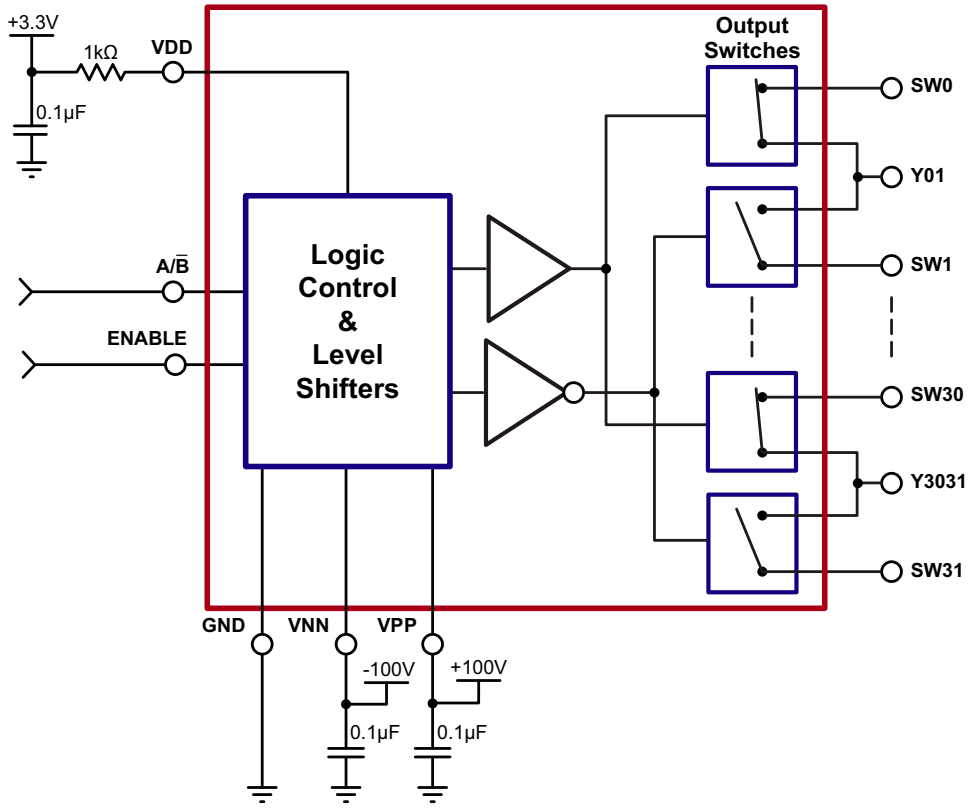
The Supertex HV2809 is a low harmonic distortion, 32-channel, high voltage analog switch integrated circuit (IC), designed for use in medical ultrasound imaging systems as a probe selection relay replacement. It serves as a 16PDT (16-pole, double throw) high voltage analog switch array. The enable function allows the parts to be configured as either a 2:1 or 4:1 multiplexer/demultiplexer. The HV2809 is a very fast transducer multiplexer that consumes minimal power and emits no audible noise.

Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN}: +40V/-160V, +100V/-100V, and +160V/-40V.

The HV2809 comes in an 8.0mm x 8.0mm x 1.0mm, 56-Lead QFN package. Compared to an electromechanical relay, it not only saves considerable PCB area, but also saves on the PCB assembled height.

Block Diagram



Ordering Information

Part Number	Package Options	Packing
HV2809K6-G	56-Lead (8x8) QFN	250/Tray
HV2809K6-G M937	56-Lead (8x8) QFN	2000/Reel

- G indicates package is RoHS compliant ('Green')

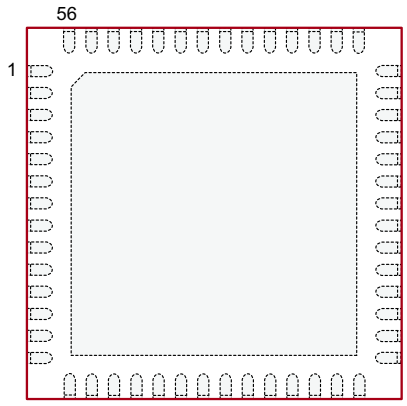
ESD Sensitive Device

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic supply	-0.5V to +6.5V
V_{PP}-V_{NN} differential supply	220V
V_{PP} positive supply	-0.5V to V_{NN} +200V
V_{NN} negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C

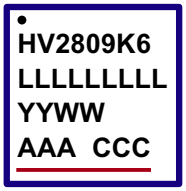
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



56-Lead QFN
(top view)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or

56-Lead QFN

Typical Thermal Resistance

Package	θ_{ja}
56-Lead QFN	21°C/W

Recommended Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	3.0 to 5.5V
V_{PP}	Positive high voltage supply	+40 to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40 to -160V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0 to 0.1V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0 to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1.0msec.*

DC Electrical Characteristics *(Over recommended operating conditions unless otherwise specified)*

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I_{SIG} = 5.0mA	V_{PP} = +40V, V_{NN} = -160V
		-	25	-	22	27	-	32		I_{SIG} = 200mA	
		-	25	-	22	27	-	30		I_{SIG} = 5.0mA	V_{PP} = +100V, V_{NN} = -100V
		-	18	-	18	24	-	27		I_{SIG} = 200mA	
		-	23	-	20	25	-	30		I_{SIG} = 5.0mA	V_{PP} = +160V, V_{NN} = -40V
		-	22	-	16	25	-	27		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +100V, V_{NN} = -100V	
R_{ONL}	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V_{SIG} = V_{PP} -10V, I_{SIG} = 1A	
I_{SOL}	Switch OFF-leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V, V_{NN} +10V	
V_{OS}	DC offset switch OFF	-	300	-	100	300	-	300	mV	100kΩ load	
	DC offset switch ON	-	500	-	100	500	-	500			
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches OFF	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-			
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches ON, I_{SW} = 5.0mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-			
I_{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%	
f_{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	13	-	-	14	-	16	mA	V_{PP}= +40V, V_{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	8.0	-	-	10	-	11		V_{PP}= +100V, V_{NN} = -100V	
		-	8.0	-	-	10	-	11		V_{PP}= +160V, V_{NN} = -40V	
I_{NN}	Average V_{NN} supply current	-	13	-	-	14	-	16	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	8.0	-	-	10	-	11		V_{PP}= +100V, V_{NN} = -100V	
		-	8.0	-	-	10	-	11		V_{PP}= +160V, V_{NN} = -40V	
I_{DD}	V_{DD} supply current	-	0.1	-	-	0.1	-	0.1	mA	V_{DD} = 5.0V@ 50kHz CW	
I_{DDQ}	Quiescent V_{DD} supply current	-	10	-	-	10	-	10	µA	All logic inputs are static	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

** See Test Circuits on page 5*

AC Electrical Characteristics *(Over recommended operating conditions unless otherwise specified)*

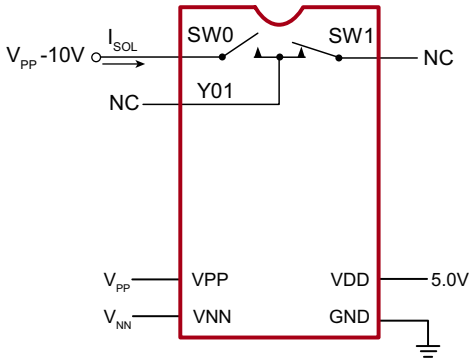
Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{ON}	Turn ON time	-	30	-	15	30	-	30	µs	V_{SIG} = V_{PP} -10V, V_{PP} = +100V, R_{LOAD} = 10kΩ, V_{NN} = -100V
t_{OFF}	Turn OFF time	-	30	-	15	30	-	30		
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	V_{PP} = +40V, V_{NN} = -160V
		-	20	-	-	20	-	20		V_{PP} = +100V, V_{NN} = -100V
		-	20	-	-	20	-	20		V_{PP} = +160V, V_{NN} = -40V
K_O	OFF isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz,1.0kΩ//15pF load
		-58	-	-58	-	-	-58	-		f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	OFF capacitance SW to GND	-	14	-	9.0	14	-	14	pF	V_{SIG} = 0V, f = 1.0MHz, both SW OFF
	OFF capacitance Y to GND	-	28	-	18	28	-	28		
$C_{SG(ON)}$	ON capacitance SW to GND	-	33	-	23	33	-	33	pF	V_{SIG} = 0V, f = 1.0MHz, one SW ON, one SW OFF
	ON capacitance Y to GND	-	33	-	23	33	-	33		
$+V_{SPK}$	Output voltage spike SW	-	250	-	-	250	-	250	mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	250	-	-	250	-	250		
$+V_{SPK}$		-	250	-	-	250	-	250		V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	250	-	-	250	-	250		
$+V_{SPK}$		-	250	-	-	250	-	250		V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	250	-	-	250	-	250		
$+V_{SPK}$	Output voltage spike Y	-	250	-	-	250	-	250	mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	250	-	-	250	-	250		
$+V_{SPK}$		-	250	-	-	250	-	250		V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	250	-	-	250	-	250		
$+V_{SPK}$		-	250	-	-	250	-	250		V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	250	-	-	250	-	250		
QC	Charge injection	-	-	-	1020	-	-	-	pC	V_{PP} = +40V, V_{NN} = -160V
		-	-	-	700	-	-	-		V_{PP} = +100V, V_{NN} = -100V
		-	-	-	370	-	-	-		V_{PP} = +160V, V_{NN} = -40V

** See Test Circuits on page 5*

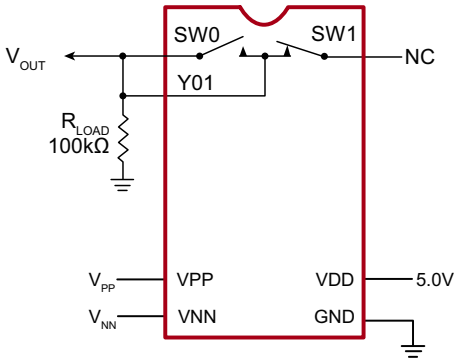
Truth Table

Logic Inputs		Switch Status
EN	A/B	
H	H	SW0, 2, 4...30 ON, SW1, 3, 5...31 OFF
H	L	SW0, 2, 4...30 OFF, SW1, 3, 5...31 ON
L	X	All switches OFF

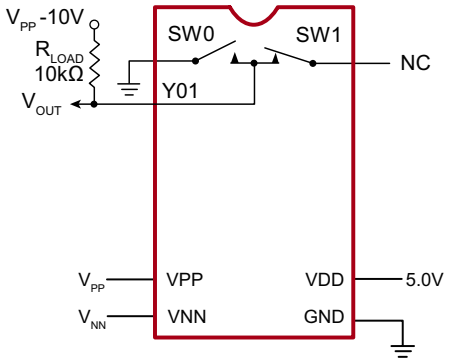
Test Circuits



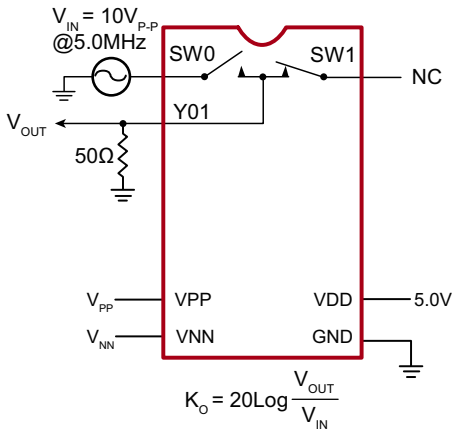
Switch OFF Leakage



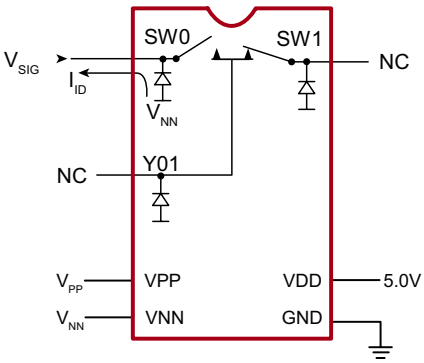
DC Offset ON/OFF



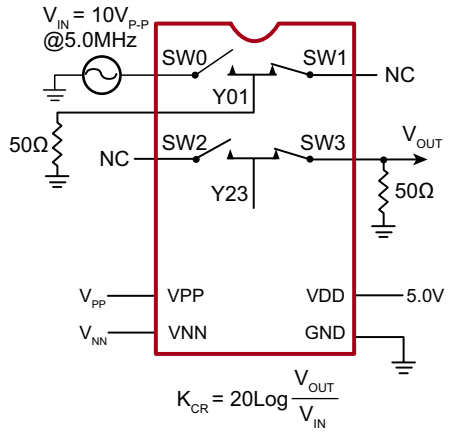
T_{ON}/T_{OFF} Test Circuit



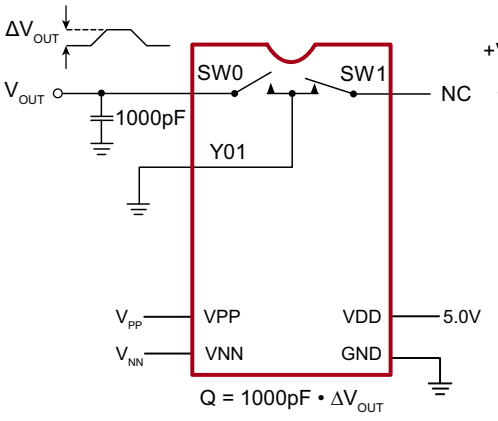
OFF Isolation



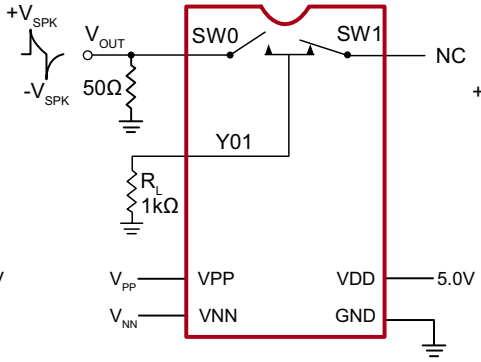
Isolation Diode Current



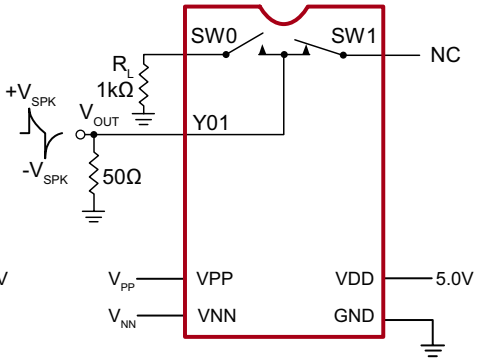
Crosstalk



Charge Injection



Output Voltage Spike SW



Output Voltage Spike Y

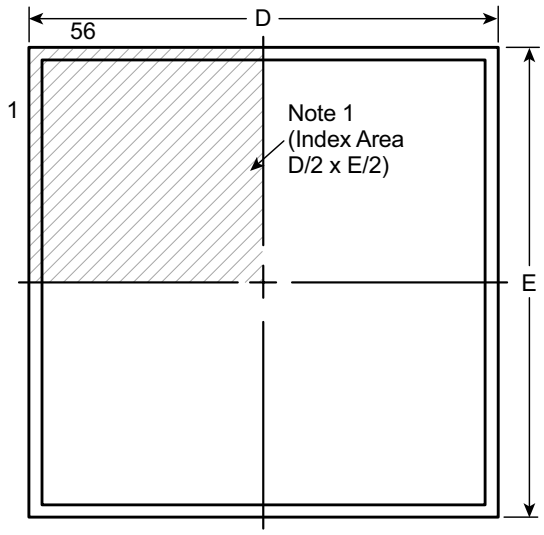
Pin Function

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Y2829	15	SW3	29	Y1213	43	SW19
2	SW29	16	SW4	30	SW13	44	SW20
3	SW30	17	Y45	31	VNN	45	Y2021
4	Y3031	18	SW5	32	SW14	46	SW21
5	SW31	19	SW6	33	Y1415	47	SW22
6	ENABLE	20	Y67	34	SW15	48	Y2223
7	VDD	21	SW7	35	VPP	49	SW23
8	A/$\overline{B}$	22	SW8	36	VPP	50	SW24
9	GND	23	Y89	37	SW16	51	Y2425
10	SW0	24	SW9	38	Y1617	52	SW25
11	Y01	25	SW10	39	SW17	53	SW26
12	SW1	26	Y1011	40	VNN	54	Y2627
13	SW2	27	SW11	41	SW18	55	SW27
14	Y23	28	SW12	42	Y1819	56	SW28

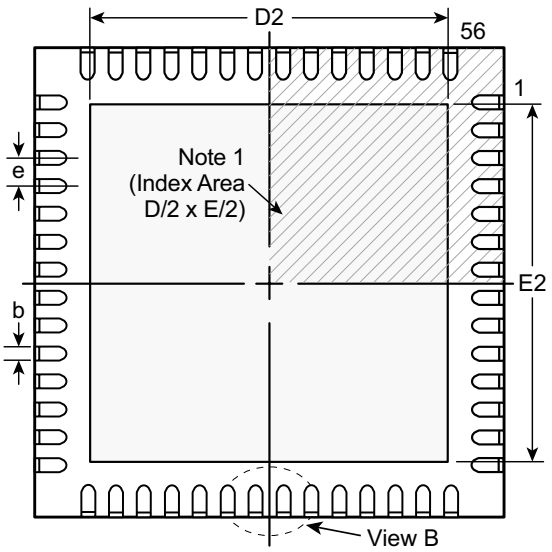
VSUB (Thermal Pad)	The central thermal pad on the bottom of package must be connected to VNN externally

56-Lead QFN Package Outline (K6)

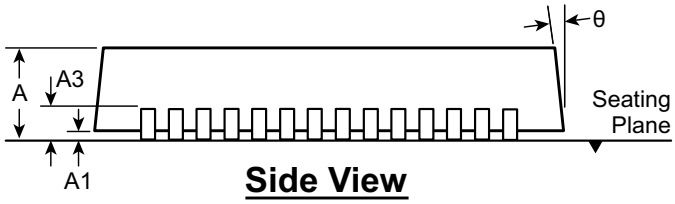
8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



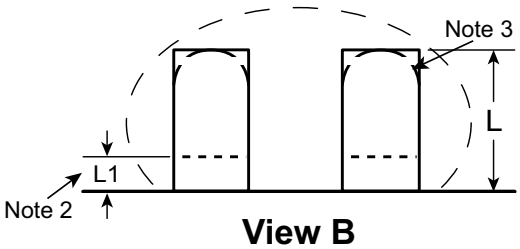
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	7.85*	2.75	7.85*	2.75	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	8.00	5.70	8.00	5.70		0.40	-	-
	MAX	1.00	0.05		0.30	8.15*	6.70†	8.15*	6.70†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.
Supertex Doc.#: *DSPD-56QFNK68X8P050, Version A031010.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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