19-3460; Rev 0; 10/04

EVALUATION KIT AVAILABLE

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

MAX1430

General Description

The MAX1430 is a 5V, high-speed, high-performance analog-to-digital converter (ADC) featuring a fully differential wideband track-and-hold (T/H) and a 15-bit converter core. The MAX1430 is optimized for multichannel, multimode receivers, which require the ADC to meet very stringent dynamic performance requirements. With a noise floor of -76.8dBFS, the MAX1430 allows for the design of receivers with superior sensitivity.

The MAX1430 achieves two-tone, spurious-free dynamic range (SFDR) of -92dBc for input tones of 69MHz and 71MHz. Its excellent signal-to-noise ratio (SNR) of 72.8dB and single-tone SFDR performance (SFDR1/SFDR2) of 86dBc/83dBc at f_{IN} = 70MHz and a sampling rate of 100Msps make this part ideal for high-performance digital receivers.

The MAX1430 operates from an analog 5V and a digital 3V supply, features a $2.2V_{P-P}$ full-scale input range, and allows for a sampling speed of up to 100Msps. The input T/H operates with a -1dB full-power bandwidth of 350MHz.

The MAX1430 features parallel, CMOS-compatible outputs in two's-complement format. To enable the interface with a wide range of logic devices, this ADC provides a separate output driver power-supply range of 2.3V to 3.5V. The MAX1430 is manufactured in an 8mm x 8mm, 56-pin thin QFN package with exposed paddle (EP) for low thermal resistance, and is specified for the extended industrial (-40°C to +85°C) temperature range.

Note that IF parts MAX1418, MAX1428, and MAX1430 (see *Pin-Compatible Higher/Lower Speed Versions Selection* table) are recommended for applications that require high dynamic performance for input frequencies greater than $f_{CLK}/3$. Unlike its baseband counterpart MAX1429, the MAX1430 is optimized for input frequencies greater than $f_{CLK}/3$.

Applications

Cellular Base-Station Transceiver Systems (BTS)

Wireless Local Loop (WLL)

Single- and Multicarrier Receivers

Multistandard Receivers

E911 Location Receivers

Power Amplifier Linearity Correction

Antenna Array Processing

Features

- **100Msps Minimum Sampling Rate**
- **-76.8dBFS Noise Floor**
- **Excellent Dynamic Performance**
  72.8dB SNR at f_{IN} = 70MHz and A_{IN} = -2dBFS
  86dBc/83dBc Single-Tone SFDR1/SFDR2 at f_{IN} = 70MHz and A_{IN} = -2dBFS
  -92dB Multitone SFDR at f_{IN1} = 69MHz and f_{IN2} = 71MHz
- **Less than 0.25ps Sampling Jitter**
- **Fully Differential Analog Input Voltage Range of $2.2V_{P-P}$**
- **CMOS-Compatible Two's-Complement Data Output**
- **Separate Data Valid Clock and Overrange Outputs**
- **Flexible-Input Clock Buffer**
- **EV Kit Available for MAX1430 (Order MAX1427EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1430ETN	-40°C to +85°C	56 Thin QFN-EP*

**EP = Exposed paddle.*

Pin-Compatible Higher/Lower Speed Versions Selection

PART	SPEED GRADE (Msps)	TARGET APPLICATION
MAX1418	65	IF
MAX1419	65	Baseband
MAX1427	80	Baseband
MAX1428	80	IF
MAX1429	100	Baseband
MAX1430	100	IF

Pin Configuration appears at end of data sheet.

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

ABSOLUTE MAXIMUM RATINGS

AV_{CC}, DV_{CC}, DRV_{CC} to GND..... -0.3V to +6V
INP, INN, CLKP, CLKN, CM to GND.....-0.3V to (AV_{CC} + 0.3V)
D0–D14, DAV, DOR to GND.....-0.3V to (DRV_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN (derate 47.6mW/°C above +70°C) ..3809.5mW
Operating Temperature Range .....-40°C to +85°C
Thermal Resistance θ_{JA}.....21°C/W
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{CC} = 5V, DV_{CC} = DRV_{CC} = 2.5V, GND = 0, INP and INN driven differentially with -2dBFS, CLKP and CLKN driven differentially with a $2V_{P-P}$ sinusoidal input signal, C_L = 5pF at digital outputs, f_{CLK} = 100MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			15			Bits
Integral Nonlinearity	INL	f_{IN} = 15MHz		±1.5		LSB
Differential Nonlinearity	DNL	f_{IN} = 70MHz, no missing codes guaranteed		±0.4		LSB
Offset Error			-12		+12	mV
Gain Error			-4		+4	%FS
ANALOG INPUT (INP, INN)						
Differential Input Voltage Range	V_{DIFF}	Fully differential inputs drive, V_{DIFF}=V_{INP} - V_{INN}		2.20		V_{P-P}
Common-Mode Input Voltage	V_{CM}	Self-biased		4.158		V
Differential Input Resistance	R_{IN}			1 ±15%		kΩ
Differential Input Capacitance	C_{IN}			1		pF
Full-Power Analog Bandwidth	$FPBW_{-1dB}$	-1dB rolloff for a full-scale input		350		MHz
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		100			MHz
Minimum Clock Frequency	f_{CLK}			20		MHz
Aperture Jitter	t_{AJ}			0.21		ps_{RMS}
CLOCK INPUT (CLKP, CLKN)						
Full-Scale Differential Input Voltage	$V_{DIFFCLK}$	Fully differential input drive, V_{CLKP} - V_{CLKN}		0.5 to 3.0		V
Common-Mode Input Voltage	V_{CM}	Self-biased		2.4		V
Differential Input Resistance	R_{INCLK}			2 ±15%		kΩ
Differential Input Capacitance	C_{INCLK}			1		pF
DYNAMIC CHARACTERISTICS						
Thermal + Quantization Noise Floor	NF	Analog input <-35dBFS		-76.8		dBFS

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = 5V, DV_{CC} = DRV_{CC} = 2.5V, GND = 0, INP and INN driven differentially with -2dBFS, CLKP and CLKN driven differentially with a $2V_{P-P}$ sinusoidal input signal, C_L = 5pF at digital outputs, f_{CLK} = 100MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio (Note 1)	SNR	f_{IN} = 5MHz at -2dBFS		73.5		dB
		f_{IN} = 15MHz at -2dBFS		73.6		
		f_{IN} = 35MHz at -2dBFS		73.3		
		f_{IN} = 70MHz at -2dBFS		72.8		
		f_{IN} = 170MHz at -6dBFS		67.8		
Signal-to-Noise and Distortion (Note 1)	SINAD	f_{IN} = 5MHz at -2dBFS		73.3		dB
		f_{IN} = 15MHz at -2dBFS		73.4		
		f_{IN} = 35MHz at -2dBFS		72.6		
		f_{IN} = 70MHz at -2dBFS		72.1		
		f_{IN} = 170MHz at -6dBFS		66.5		
Spurious-Free Dynamic Range (HD2 and HD3) (Note 1)	SFDR1	f_{IN} = 5MHz at -2dBFS		93.0		dBc
		f_{IN} = 15MHz at -2dBFS		93.0		
		f_{IN} = 35MHz at -2dBFS		84.0		
		f_{IN} = 70MHz at -2dBFS	76.1	86.0		
		f_{IN} = 170MHz at -6dBFS		73.0		
Spurious-Free Dynamic Range (HD4 and higher) (Note 1)	SFDR2	f_{IN} = 5MHz at -2dBFS		95.0		dBc
		f_{IN} = 15MHz at -2dBFS		95.0		
		f_{IN} = 35MHz at -2dBFS		92.0		
		f_{IN} = 70MHz at -2dBFS	80.2	83.0		
		f_{IN} = 170MHz at -6dBFS		79.0		
Two-Tone Intermodulation Distortion	TTIMD	f_{IN1} = 69MHz at -8dBFS, f_{IN2} = 71MHz at -8dBFS		-78		dBc
Two-Tone Spurious-Free Dynamic Range	$SFDR_{TT}$	f_{IN1} = 69MHz at -12dBFS < f_{IN1} < 100dBFS, f_{IN2} = 71MHz at -12dBFS < f_{IN2} < -100dBFS		-92		dBFS
DIGITAL OUTPUTS (D0–D14, DAV, DOR)						
Digital Output-Voltage Low	V_{OL}				0.5	V
Digital Output-Voltage High	V_{OH}		DRV_{CC} - 0.5			V
TIMING CHARACTERISTICS (DV_{CC} = DRV_{CC} = 2.5V)						
CLKP/CLKN Duty Cycle	Duty Cycle			50 ±5		%
Effective Aperture Delay	t_{AD}			230		ps
Output Data Delay	t_{DAT}	(Note 3)	3.0	4.5	7.5	ns
Data Valid Delay	t_{DAV}	(Note 3)	5.3	6.5	8.7	ns
Pipeline Latency	$t_{LATENCY}$			3		Clock cycles

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = 5V, DV_{CC} = DRV_{CC} = 2.5V, GND = 0, INP and INN driven differentially with -2dBFS, CLKP and CLKN driven differentially with a $2V_{P-P}$ sinusoidal input signal, C_L = 5pF at digital outputs, f_{CLK} = 100MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLKP Rising Edge to DATA Not Valid	t_{DNV}	(Note 3)	2.6	3.8	5.7	ns
CLKP Rising Edge to DATA Valid (Guaranteed)	t_{DGV}	(Note 3)	3.4	5.2	8.6	ns
DATA Setup Time (Before DAV Rising Edge)	t_{SETUP}	(Note 3)	t_{CLKP} - 0.5	t_{CLKP} + 1.3	t_{CLKP} + 2.4	ns
DATA Hold Time (After DAV Rising Edge)	t_{HOLD}	(Note 3)	t_{CLKN} - 3.6	t_{CLKN} - 2.8	t_{CLKN} - 2.0	ns
TIMING CHARACTERISTICS (DV_{CC} = DRV_{CC} = 3.3V)						
CLKP/CLKN Duty Cycle	Duty Cycle			50 ±5		%
Effective Aperture Delay	t_{AD}			230		ps
Output Data Delay	t_{DAT}	(Note 3)	2.8	4.1	6.5	ns
Data Valid Delay	t_{DAV}	(Note 3)	5.3	6.3	8.6	ns
Pipeline Latency	$t_{LATENCY}$			3		Clock cycles
CLKP Rising Edge to DATA Not Valid	t_{DNV}	(Note 3)	2.5	3.4	5.2	ns
CLKP Rising Edge to DATA Valid (Guaranteed)	t_{DGV}	(Note 3)	3.2	4.4	7.4	ns
DATA Setup Time (Before DAV Rising Edge)	t_{SETUP}	(Note 3)	t_{CLKP} + 0.2	t_{CLKP} + 1.7	t_{CLKP} + 2.8	ns
DATA Hold Time (After DAV Rising Edge)	t_{HOLD}	(Note 3)	t_{CLKN} - 3.5	t_{CLKN} - 2.7	t_{CLKN} - 2.0	ns
POWER REQUIREMENTS						
Analog-Supply Voltage Range	AV_{CC}			5 ±3%		V
Digital-Supply Voltage Range	DV_{CC}	(Note 2)		2.3 to 3.5		V
Output-Supply Voltage Range	DRV_{CC}	(Note 2)		2.3 to 3.5		V
Analog Supply Current	I_{AVCC}			400	450	mA
Digital + Output Supply Current	I_{DVCC} + I_{DRVCC}	f_{CLK} = 100MHz, C_L = 5pF		38	44	mA
Total Power Dissipation	PDISS			2095		mW

Note 1: Dynamic performance is based on a 32,768-point data record with a sampling frequency of f_{SAMPLE} = 100.007936MHz, an input frequency of f_{IN} = f_{SAMPLE} x (22937/32768) = 70.003724MHz, and a frequency bin size of 3052Hz. Close-in (f_{IN} ± 36.6kHz) and low-frequency (DC to 73.2kHz) bins are excluded from the spectrum analysis.

Note 2: Apply the same voltage levels to DV_{CC} and DRV_{CC}

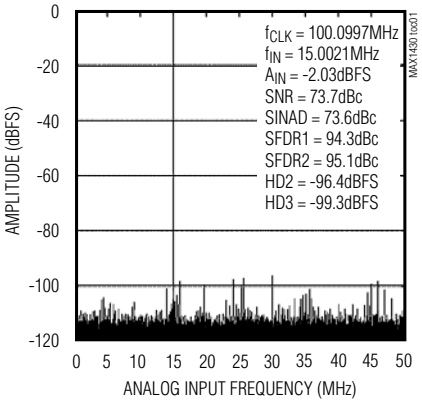
Note 3: Guaranteed by design and characterization.

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

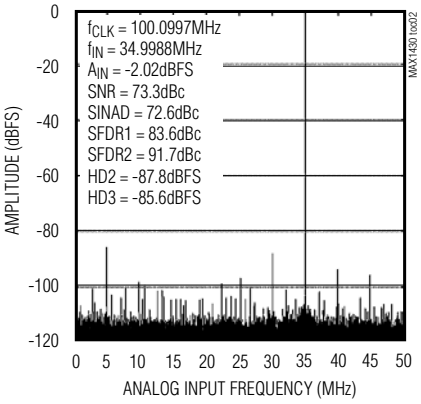
Typical Operating Characteristics

(AV_{CC} = 5V, DV_{CC} = DRV_{CC} = 2.5V, INP and INN driven differentially with a -2dBFS amplitude, CLKP and CLKN driven differentially with a $2V_{P-P}$ sinusoidal input signal, C_L = 5pF at digital outputs, f_{CLK} = 100MHz, T_A = 25°C. All AC data is based on a 32k-point FFT record and under coherent sampling conditions.)

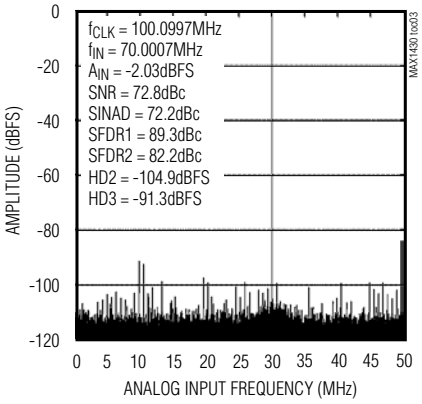
FFT PLOT (32,768-POINT DATA RECORD, COHERENT SAMPLING)



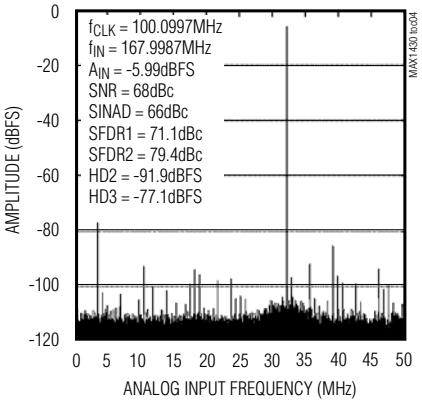
FFT PLOT (32,768-POINT DATA RECORD, COHERENT SAMPLING)



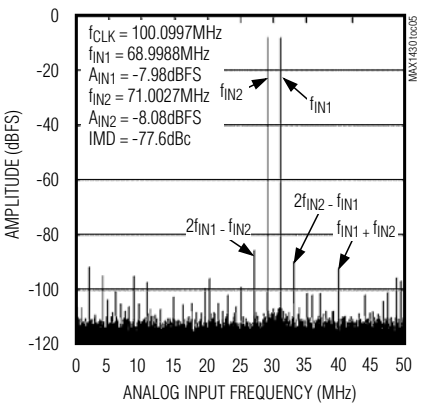
FFT PLOT (16,384-POINT DATA RECORD, COHERENT SAMPLING)



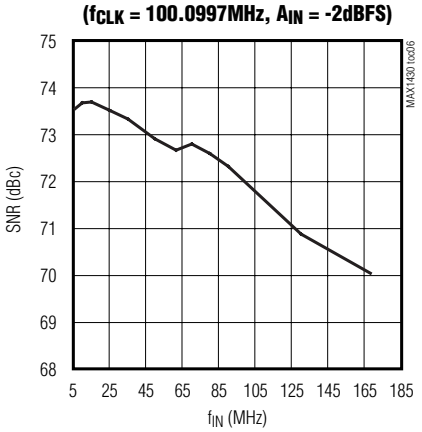
FFT PLOT (32,768-POINT DATA RECORD, COHERENT SAMPLING)



TWO-TONE IMD PLOT (32,768-POINT DATA RECORD, COHERENT SAMPLING)



SNR vs. ANALOG INPUT FREQUENCY (f_{CLK} = 100.0997MHz, A_{IN} = -2dBFS)

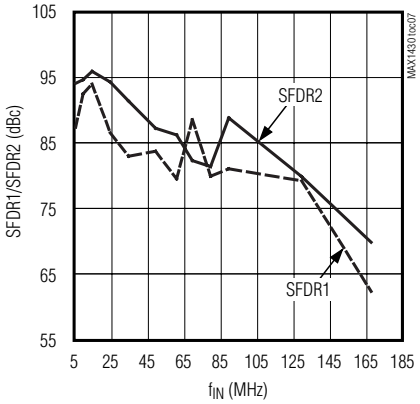


15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

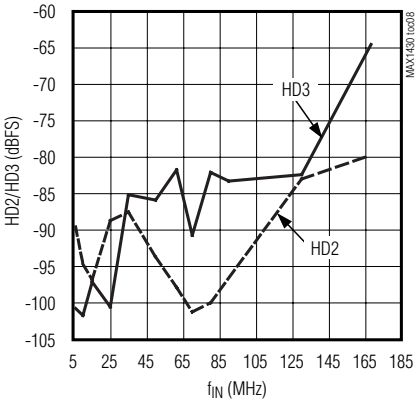
Typical Operating Characteristics (continued)

(AV_{CC} = 5V, DV_{CC} = DRV_{CC} = 2.5V, INP and INN driven differentially with a -2dBFS amplitude, CLKP and CLKN driven differentially with a $2V_{P-P}$ sinusoidal input signal, C_L = 5pF at digital outputs, f_{CLK} = 100MHz, T_A = 25°C. All AC data is based on a 32k-point FFT record and under coherent sampling conditions.)

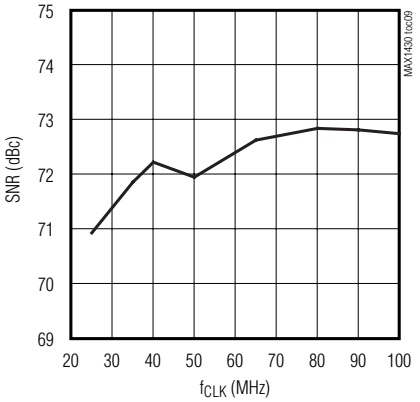
SFDR1/SFDR2 vs. ANALOG INPUT FREQUENCY (f_{CLK} = 100.0997MHz, A_{IN} = -2dBFS)



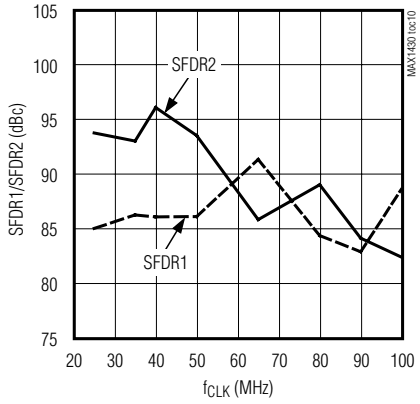
HD2/HD3 vs. ANALOG INPUT FREQUENCY (f_{CLK} = 100.0997MHz, A_{IN} = -2dBFS)



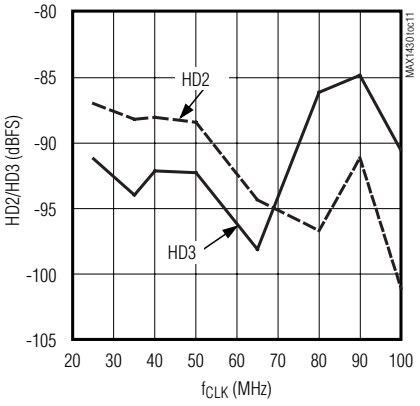
SNR vs. SAMPLING FREQUENCY (f_{IN} = 70MHz, A_{IN} = -2dBFS)



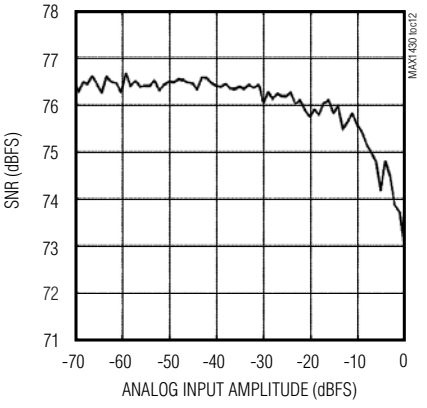
SFDR1/SFDR2 vs. SAMPLING FREQUENCY (f_{IN} = 70MHz, A_{IN} = -2dBFS)



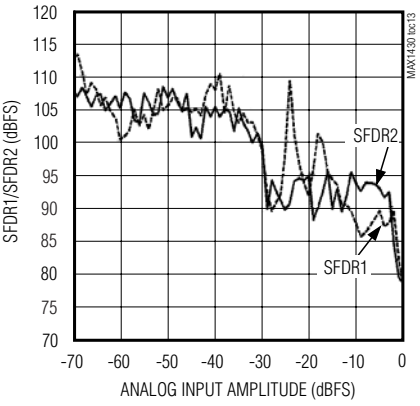
HD2/HD3 vs. SAMPLING FREQUENCY (f_{IN} = 70MHz, A_{IN} = -2dBFS)



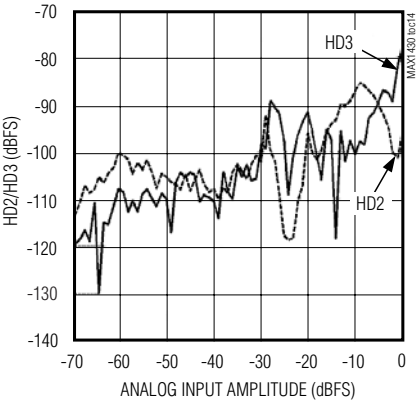
SNR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz)



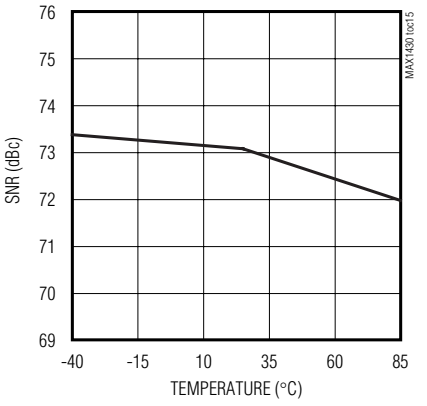
SFDR1/SFDR2 vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz)



HD2/HD3 vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz)



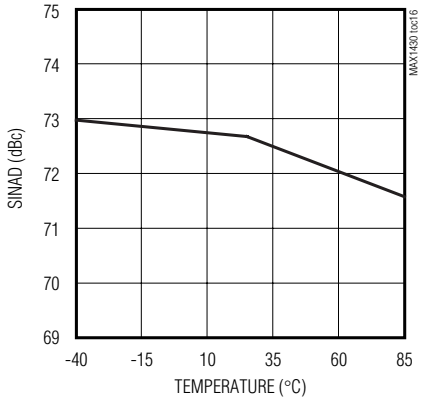
SNR vs. TEMPERATURE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz, A_{IN} = -2dBFS)



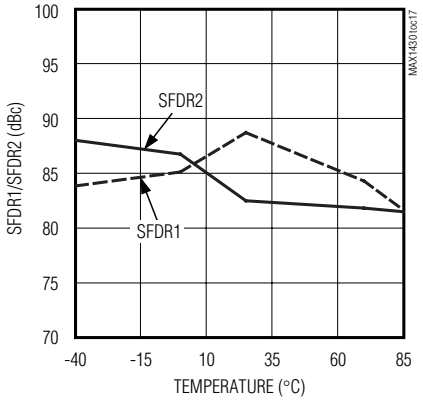
Typical Operating Characteristics (continued)

(AV_{CC} = 5V, DV_{CC} = DRV_{CC} = 2.5V, INP and INN driven differentially with a -2dBFS amplitude, CLKP and CLKN driven differentially with a $2V_{P-P}$ sinusoidal input signal, C_L = 5pF at digital outputs, f_{CLK} = 100MHz, T_A = 25°C. All AC data is based on a 32k-point FFT record and under coherent sampling conditions.)

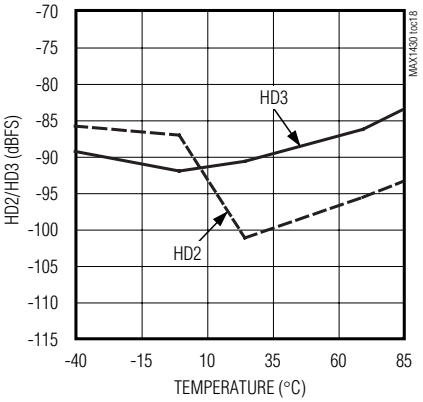
SINAD vs. TEMPERATURE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz, A_{IN} = -2dBFS)



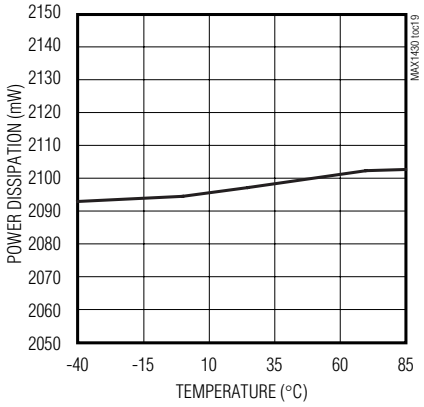
SFDR1/SFDR2 vs. TEMPERATURE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz, A_{IN} = -2dBFS)



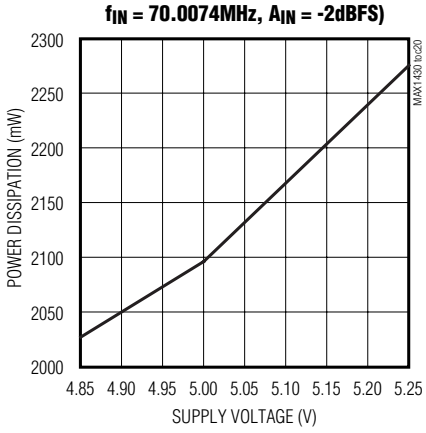
HD2/HD3 vs. TEMPERATURE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz, A_{IN} = -2dBFS)



POWER DISSIPATION vs. TEMPERATURE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz, A_{IN} = -2dBFS)



POWER DISSIPATION vs. SUPPLY VOLTAGE (f_{CLK} = 100.0997MHz, f_{IN} = 70.0074MHz, A_{IN} = -2dBFS)



15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 6, 9, 12, 14–17, 20, 23, 26, 27, 30, 52–56, EP	GND	Converter Ground. Analog, digital, and output driver grounds are internally connected to the same potential. Connect the converter's EP to GND.
4	CLKP	Differential Clock, Positive Input Terminal
5	CLKN	Differential Clock, Negative Input Terminal
7, 8, 18, 19, 21, 22, 24, 25, 28	AV_{CC}	Analog Supply Voltage. Provide local bypassing to ground with 0.1µF to 0.22µF capacitors.
10	INP	Differential Analog Input, Positive Terminal
11	INN	Differential Analog Input, Negative/Complementary Terminal
13	CM	Common-Mode Reference Terminal
29	DV_{CC}	Digital Supply Voltage. Provide local bypassing to ground with 0.1µF to 0.22µF capacitors.
31, 41, 42, 51	DRV_{CC}	Digital Output Driver Supply Voltage. Provide local bypassing to ground with 0.1µF to 0.22µF capacitors.
32	DOR	Data Overrange Bit. This control line flags an overrange condition in the ADC. If DOR transitions high, an overrange condition was detected. If DOR remains low, the ADC operates within the allowable full-scale range.
33	D0	Digital CMOS Output Bit 0 (LSB)
34	D1	Digital CMOS Output Bit 1
35	D2	Digital CMOS Output Bit 2
36	D3	Digital CMOS Output Bit 3
37	D4	Digital CMOS Output Bit 4
38	D5	Digital CMOS Output Bit 5
39	D6	Digital CMOS Output Bit 6
40	D7	Digital CMOS Output Bit 7
43	D8	Digital CMOS Output Bit 8
44	D9	Digital CMOS Output Bit 9
45	D10	Digital CMOS Output Bit 10
46	D11	Digital CMOS Output Bit 11
47	D12	Digital CMOS Output Bit 12
48	D13	Digital CMOS Output Bit 13
49	D14	Digital CMOS Output Bit 14 (MSB)
50	DAV	Data Valid Output. This output can be used as a clock control line to drive an external buffer or data-acquisition system. The typical delay time between the falling edge of the converter clock and the rising edge of DAV is 6.5ns.

Detailed Description

Figure 1 provides an overview of the MAX1430 architecture. The MAX1430 employs an input T/H amplifier, which has been optimized for low thermal noise and low distortion. The high-impedance differential inputs to the T/H amplifier (INP and INN) are self-biased at 4.158V, and support a full-scale differential input voltage of 2.2V_{P-P}. The output of the T/H amplifier is fed to a multistage pipelined ADC core, which has also been optimized to achieve a very low thermal noise floor and low distortion.

A clock buffer receives a differential input clock waveform and generates a low-jitter clock signal for the input T/H. The signal at the analog inputs is sampled at the rising edge of the differential clock waveform. The differential clock inputs (CLKP and CLKN) are high-impedance inputs, are self-biased at 2.4V, and support differential clock waveforms from 0.5V_{P-P} to 3.0V_{P-P}.

The outputs from the multistage pipelined ADC core are delivered to error correction and formatting logic, which in turn, deliver the 15-bit output code in two's-complement format to digital output drivers. The output drivers provide CMOS-compatible outputs with levels programmable over a 2.3V to 3.5V range.

Analog Inputs and Common Mode (INP, INN, CM)

The signal inputs to the MAX1430 (INP and INN) are balanced differential inputs. This differential configuration provides immunity to common-mode noise coupling and rejection of even-order harmonic terms. The differential signal inputs to the MAX1430 should be AC-coupled and carefully balanced to achieve the best dynamic performance (see the *Applications Information* section for more detail). AC-coupling of the input signal is easily accomplished because the MAX1430 inputs are self-biasing as illustrated in Figure 2. Although the T/H inputs are high impedance, the actual differential input impedance is nominally 1kΩ because of the two 500Ω bias resistors connected from each input to the common-mode reference.

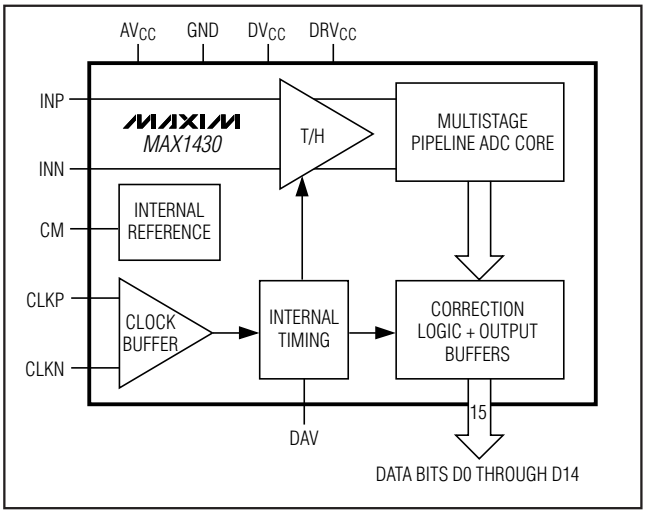


Figure 1. Simplified MAX1430 Diagram

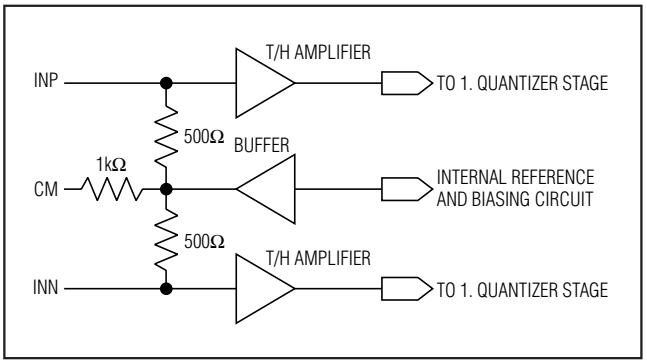


Figure 2. Simplified Analog and Common-Mode Input Architecture

The CM pin provides a monitor of the input common-mode self-bias potential. In most applications, in which the input signal is AC-coupled, this pin is not connected. If DC-coupling of the input signal is required, this pin may be used to construct a DC servo loop to control the input common-mode potential. See the *Applications Information* section for more details.

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

On-Chip Reference Circuit

The MAX1430 incorporates an on-chip 2.5V, low-drift bandgap reference. This reference potential establishes the full-scale range for the converter, which is nominally 2.2V_{P-P} differential. The internal reference potential is not accessible to the user, so the full-scale range for the MAX1430 cannot be externally adjusted.

Figure 3 shows how the reference is used to generate the common-mode bias potential for the analog inputs. The common-mode input bias is set to two diode potentials above the bandgap reference potential, and so varies over temperature.

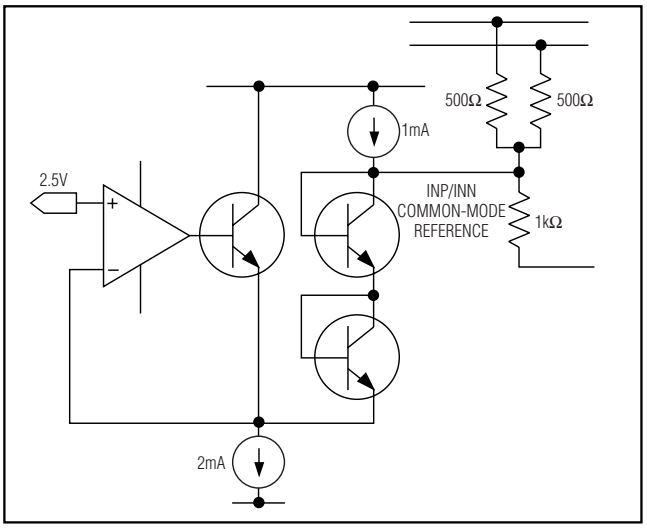


Figure 3. Simplified Reference Architecture

Clock Inputs (CLKP, CLKN)

The differential clock buffer for the MAX1430 has been designed to accept an AC-coupled clock waveform. Like the signal inputs, the clock inputs are self-biasing. In this case, the common-mode bias potential is 2.4V and each input is connected to the reference potential through a 1kΩ resistor. Consequently, the differential input resistance associated with the clock inputs is 2kΩ. While differential clock signals as low as 0.5V_{P-P} may be used to drive the clock inputs, best dynamic performance is achieved with clock input voltage levels of 2V_{P-P} to 3V_{P-P}. Jitter on the clock signal translates directly to jitter (noise) on the sampled signal. Therefore, the clock source should be a low-jitter (low phase noise) source. See the *Applications Information* section for additional details on driving the clock inputs.

System Timing Requirements

Figure 4 depicts the timing relationships for the signal input, clock input, data output, and DAV output. The variables shown in the figure correspond to the various timing specifications in the *Electrical Characteristics* table. These include:

- t_{DAT}: Delay from the rising edge of the clock until the 50% point of the output data transition
- t_{DAV}: Delay from the falling edge of the clock until the 50% point of the DAV rising edge
- t_{DNV}: Time from the rising edge of the clock until data is no longer valid
- t_{DGV}: Time from the rising edge of the clock until data is guaranteed to be valid

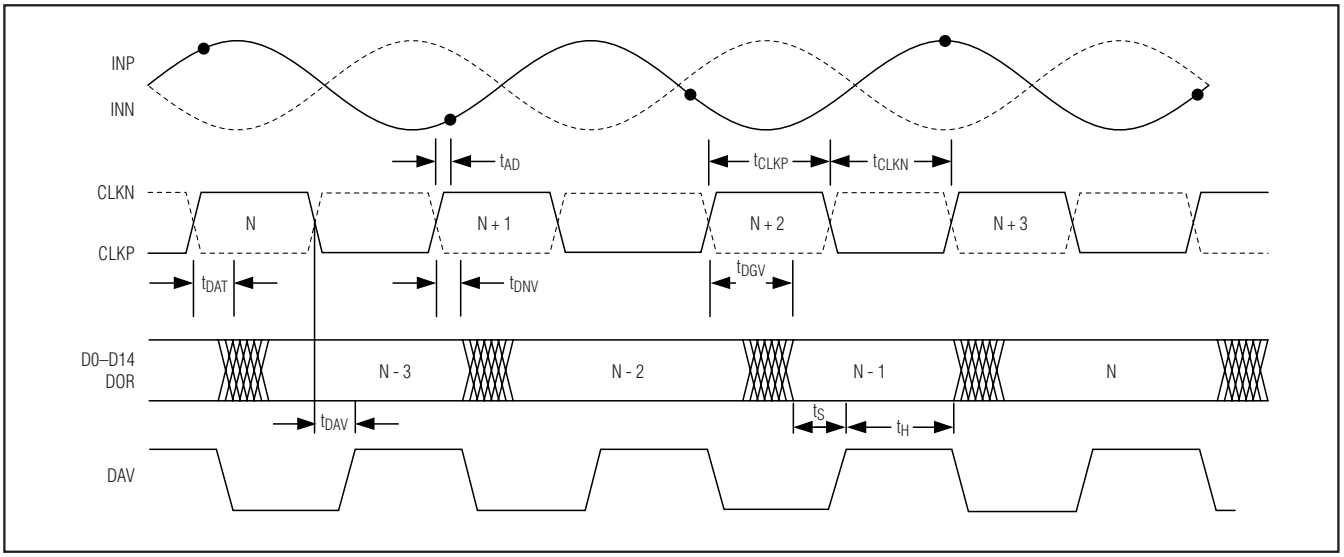


Figure 4. System and Output Timing Diagram

- t_{SETUP}: Time from data guaranteed valid until the rising edge of DAV
- t_{HOLD}: Time from the rising edge of DAV until data is no longer valid
- t_{CLKP}: Time from the 50% point of the rising edge to the 50% point of the falling edge of the clock signal
- t_{CLKN}: Time from the 50% point of the falling edge to the 50% point of the rising edge of the clock signal

The MAX1430 samples the input signal on the rising edge of the input clock. Output data is valid on the rising edge of the DAV signal, with a data latency of three clock cycles. Note that the clock duty cycle must be 50% ±5% for proper operation.

Digital Outputs (D0–D14, DAV, DOR)

The logic-high level of the CMOS-compatible digital outputs (D0–D14, DAV, and DOR) can be set in the 2.3V to 3.5V range. This is accomplished by setting the voltage at the DV_{CC} and DRV_{CC} pins to the desired logic-high level. **Note that the DV_{CC} and DRV_{CC} voltages must be the same value**.

For best performance, the capacitive loading on the digital outputs of the MAX1430 should be kept as low as possible (<10pF). Large capacitive loads result in large charging currents during data transitions, which may feed back into the analog section of the ADC and create distortion terms. The loading capacitance is kept low by keeping the output traces short and by driving a single CMOS buffer or latch input (as opposed to multiple CMOS inputs).

Inserting small series resistors (220Ω or less) between the MAX1430 outputs and the digital load, placed as closely as possible to the output pins, is helpful in controlling the size of the charging currents during data transitions and can improve dynamic performance. Keep the trace length from the resistor to the load as short as possible to minimize trace capacitance.

The output data is in two's complement format, as illustrated in Table 1.

Data is valid at the rising edge of DAV (Figure 4), and DAV can be used as a clock signal to latch the output data. The DAV output provides twice the drive strength of the data outputs, and may therefore be used to drive multiple data latches.

The DOR output is used to identify an overrange condition. If the input signal exceeds the positive or negative full-scale range for the MAX1430, then DOR is asserted high. The timing for DOR is identical to the timing for the data outputs, and DOR therefore provides an overrange indication on a sample-by-sample basis.

Table 1. MAX1430 Digital Output Coding

INP ANALOG VOLTAGE LEVEL	INN ANALOG VOLTAGE LEVEL	D14–D0 TWO'S COMPLEMENT CODE
V_{REF} + 0.64V	V_{REF} - 0.64V	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 (positive full scale)
V_{REF}	V_{REF}	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 (midscale + δ) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 (midscale - δ)
V_{REF} - 0.64V	V_{REF} + 0.64V	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 (negative full scale)

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

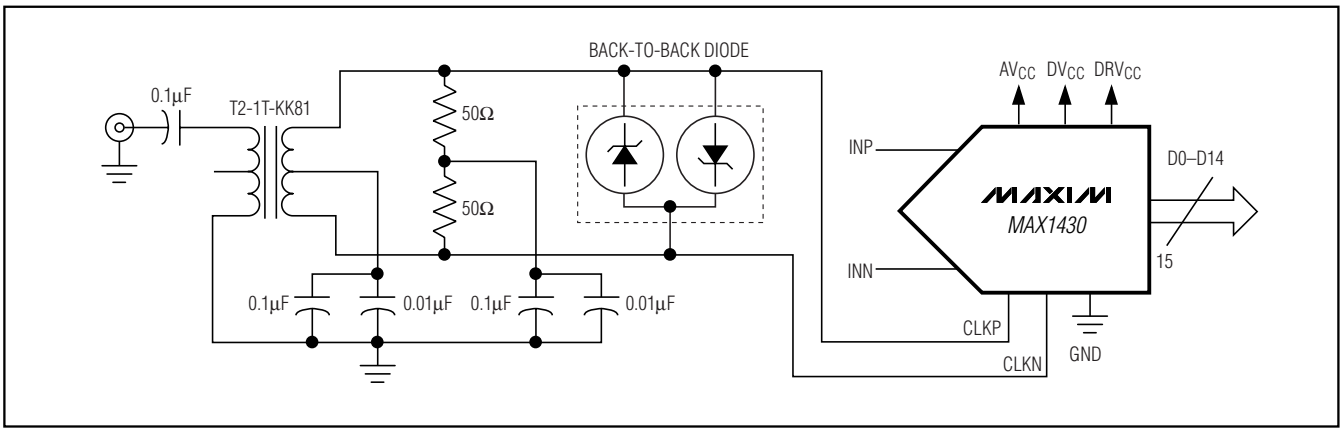


Figure 5. Transformer-Coupled Clock Input Configuration

Applications Information

Differential, AC-Coupled Clock Input

The clock inputs to the MAX1430 are designed to be driven with an AC-coupled differential signal, and best performance is achieved under these conditions. However, it is often the case that the available clock source is single ended. Figure 5 demonstrates one method for converting a single-ended clock signal into a differential signal through a transformer. In this example, the transformer turns ratio from the primary to secondary side is 1:1.414. The impedance ratio from primary to secondary is the square of the turns ratio, or 1:2, so that terminating the secondary side with a 100Ω differential resistance results in a 50Ω load looking into the primary side of the transformer. The termination resistor in this example comprises the series combination of two 50Ω resistors with their common node AC-coupled to ground. Alternatively, a single 100Ω resistor across the two inputs with no common-mode connection could be employed.

In the example of Figure 5, the secondary side of the transformer is coupled directly to the clock inputs. Since the clock inputs are self-biasing, the center tap of the transformer must be AC-coupled to ground or left floating. If the center tap of the secondary were DC-coupled to ground, then it would be necessary to add blocking capacitors in series with the clock inputs.

Clock jitter is generally improved if the clock signal has a high slew rate at the time of its zero crossing. Therefore, if a sinusoidal source is used to drive the clock inputs, it is desirable that the clock amplitude be as large as possible to maximize the zero-crossing slew rate. The back-to-back Schottky diodes shown in Figure 5 are not required as long as the input signal is held to $3V_{P-P}$ differential or less. If a larger amplitude signal is provided (to maximize the zero-crossing slew rate), then the diodes serve to limit the differential signal swing at the clock inputs.

Any differential-mode noise coupled to the clock inputs translates to clock jitter and degrades the SNR performance of the MAX1430. Any differential-mode coupling of the analog input signal into the clock inputs results in harmonic distortion. Consequently, it is important that the clock lines be well isolated from the analog signal input and from the digital outputs. See the *PC Board Layout Considerations* section for more discussion on noise coupling.

Differential, AC-Coupled Analog Input

The analog inputs (INP and INN) are designed to be driven with a differential AC-coupled signal. It is extremely important that these inputs be accurately balanced. Any common-mode signal applied to these inputs degrades even-order distortion terms. Therefore, any attempt at driving these inputs in a single-ended fashion results in significant even-order distortion terms.

Figure 6 presents one method for converting a single-ended signal to a balanced differential signal using a transformer. The primary-to-secondary turns ratio in this example is 1:1.414. The impedance ratio is the square of the turns ratio, so in this example, the impedance ratio is 1:2. To achieve a 50Ω input impedance at the primary side of the transformer, the secondary side is terminated with a 112Ω differential load. This load, in shunt with the differential input resistance of the MAX1430, results in a 100Ω differential load on the secondary side. It is reasonable to use a larger transformer turns ratio to achieve a larger signal step-up, and this may be desirable to relax the drive requirements for the circuitry driving the MAX1430. However, the larger the

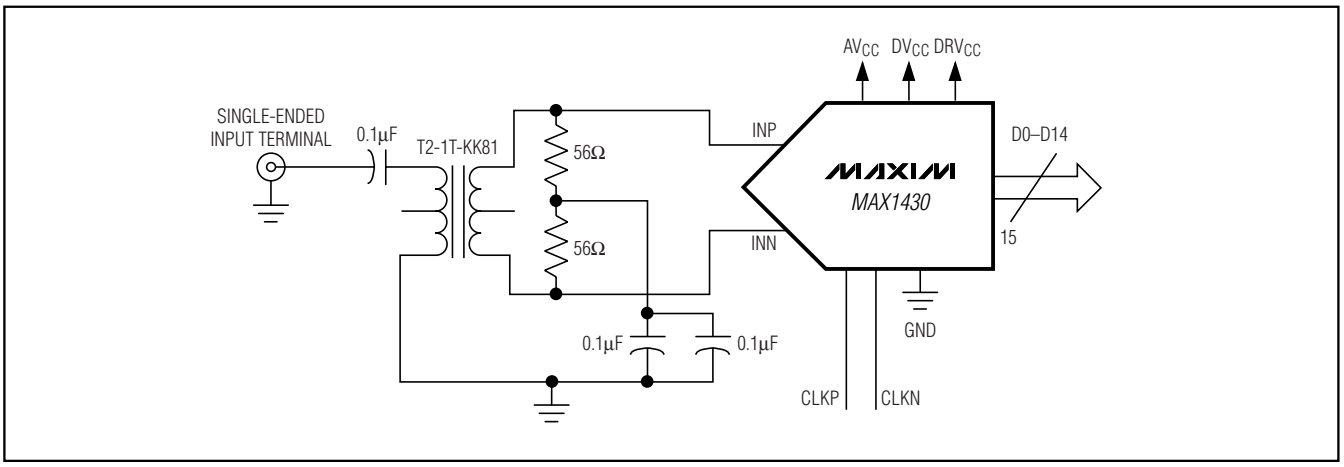


Figure 6. Transformer-Coupled Analog Input Configuration

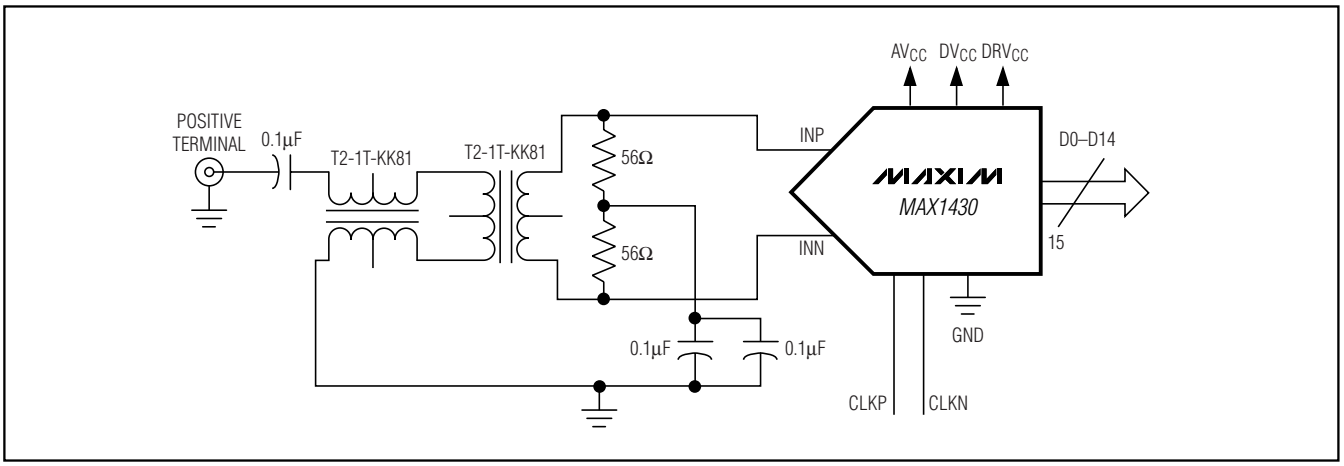


Figure 7. Transformer-Coupled Analog Input Configuration with Primary-Side Transformer

turns ratio, the larger the effect of the differential input resistance of the MAX1430 on the primary referred input resistance. At a turns ratio of 1:4.47, the 1kΩ differential input resistance of the MAX1430 by itself results in a primary referred input resistance of 50Ω.

Although the center tap of the transformer in Figure 6 is shown floating, it may be AC-coupled to ground. However, experience has shown that better balance is achieved if the center tap is left floating.

As stated previously, the signal inputs to the MAX1430 must be accurately balanced to achieve the best even-order distortion performance. Figure 7 provides improved balance over the circuit of Figure 6 by adding a balun on the primary side of the transformer, and can yield substantial improvement in even-order distortion terms over the circuit of Figure 6.

One note of caution in relation to transformers is important. Any DC current passed through the primary or secondary windings of a transformer may magnetically bias the transformer core. When this happens, the transformer is no longer accurately balanced and a degradation in the distortion of the MAX1430 may be observed. The core must be demagnetized to return to balanced operation.

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

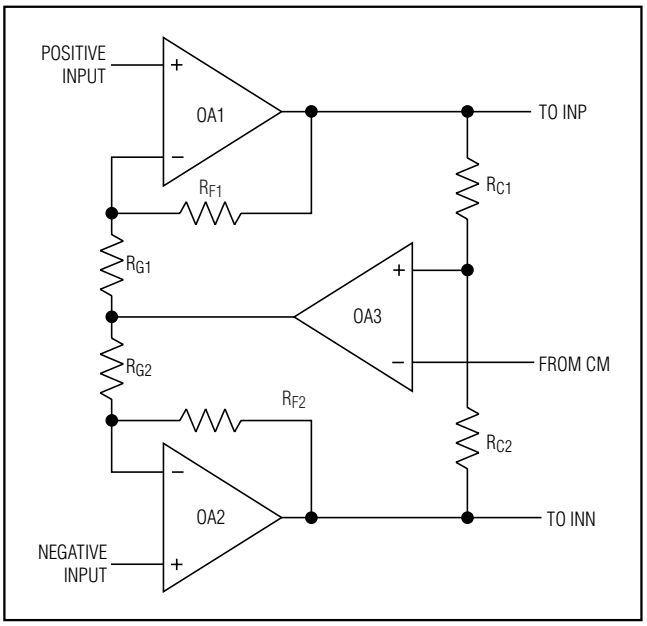


Figure 8. DC-Coupled Analog Input Configuration

DC-Coupled Analog Input

While AC-coupling of the input signal is the proper means for achieving the best dynamic performance, it is possible to DC-couple the inputs by making use of the CM potential. Figure 8 shows one method for accomplishing DC-coupling. The common-mode potentials at the outputs of amplifiers OA1 and OA2 are "servoed" by the action of amplifier OA3 to be equal to the CM potential of the MAX1430. Care must be taken to ensure that the common-mode loop is stable, and the R_F/R_G ratios of both half circuits must be well matched to ensure balance.

PC Board Layout Considerations

The performance of any high-dynamic-range, high-sample-rate converter can be compromised by poor PC board layout practices. The MAX1430 is no exception to the rule, and careful layout techniques must be observed to achieve the specified performance. Layout issues are addressed in the following four categories:

1) Layer assignments

2) Signal routing

3) Grounding

4) Supply routing and bypassing

The MAX1427 evaluation board (MAX1427 EV kit) provides an excellent frame of reference for board layout, and the discussion that follows is consistent with the practices incorporated on the evaluation board.

Layer Assignments

The MAX1427 EV kit is a six-layer board, and the assignment of layers is discussed in this context. It is recommended that the ground plane be on a layer between the signal routing layer and the supply routing layer(s). This practice prevents coupling from the supply lines into the signal lines. The MAX1427 EV kit PC board places the signal lines on the top (component) layer and the ground plane on layer 2. Any region on the top layer not devoted to signal routing is filled with ground plane with vias to layer 2. Layers 3 and 4 are devoted to supply routing, layer 5 is another ground plane, and layer 6 is used for the placement of additional components and for additional signal routing.

A four-layer implementation is also feasible using layer 1 for signal lines, layer 2 as a ground plane, layer 3 for supply routing, and layer 4 for additional signal routing. However, care must be taken to ensure the clock and signal lines are isolated from each other and from the supply lines.

Signal Routing

To preserve good even-order distortion, the signal lines (those traces feeding the INP and INN inputs) must be carefully balanced. To accomplish this, the signal traces should be made as symmetric as possible, meaning that each of the two signal traces should be the same length and should see the same parasitic environment. As mentioned previously, the signal lines must be isolated from the supply lines to prevent coupling from the supplies to the inputs. This is accomplished by making the necessary layer assignments as described in the previous section. Additionally, it is crucial that the clock lines be isolated from the signal lines. On the MAX1427 EV kit, this is done by routing the clock lines on the bottom layer (layer 6). The clock lines then connect to the ADC through vias placed in close proximity to the device. The clock lines are isolated from the supply lines by virtue of the ground plane on layer 5.

The digital output traces should be kept as short as possible to minimize capacitive loading. The ground plane on layer 2 beneath these traces should not be removed so the digital ground return currents have an uninterrupted path back to the bypass capacitors.

Grounding

The practice of providing a split ground plane in an attempt to confine digital ground return currents has often been recommended in ADC application literature. However, for converters such as the MAX1430, it is strongly recommended to employ a single, uninterrupted ground plane. The MAX1427 EV kit achieves excellent dynamic performance with such a ground plane.

The EP of the MAX1430 should be soldered directly to a ground pad on layer 1 with vias to the ground plane on layer 2. This provides excellent electrical and thermal connections to the printed circuit.

Supply Bypassing

The MAX1427 EV kit uses 220µF capacitors on each supply line (AV_{CC}, DV_{CC}, and DRV_{CC}) to provide low-frequency bypassing. The loss (series resistance) associated with these capacitors is actually of some benefit in eliminating high-Q supply resonances. Ferrite beads are also used on each of the supply lines to enhance supply bypassing (Figure 9).

Small value (0.01µF to 0.1µF) surface-mount capacitors should be placed at each supply pin or each grouping of supply pins to attenuate high-frequency supply noise (Figure 9). It is recommended to place these capacitors on the topside of the board and as close to the device as possible with short connections to the ground plane.

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. However, the static linearity parameters for the MAX1430 are measured using the histogram method with an input frequency of 15MHz.

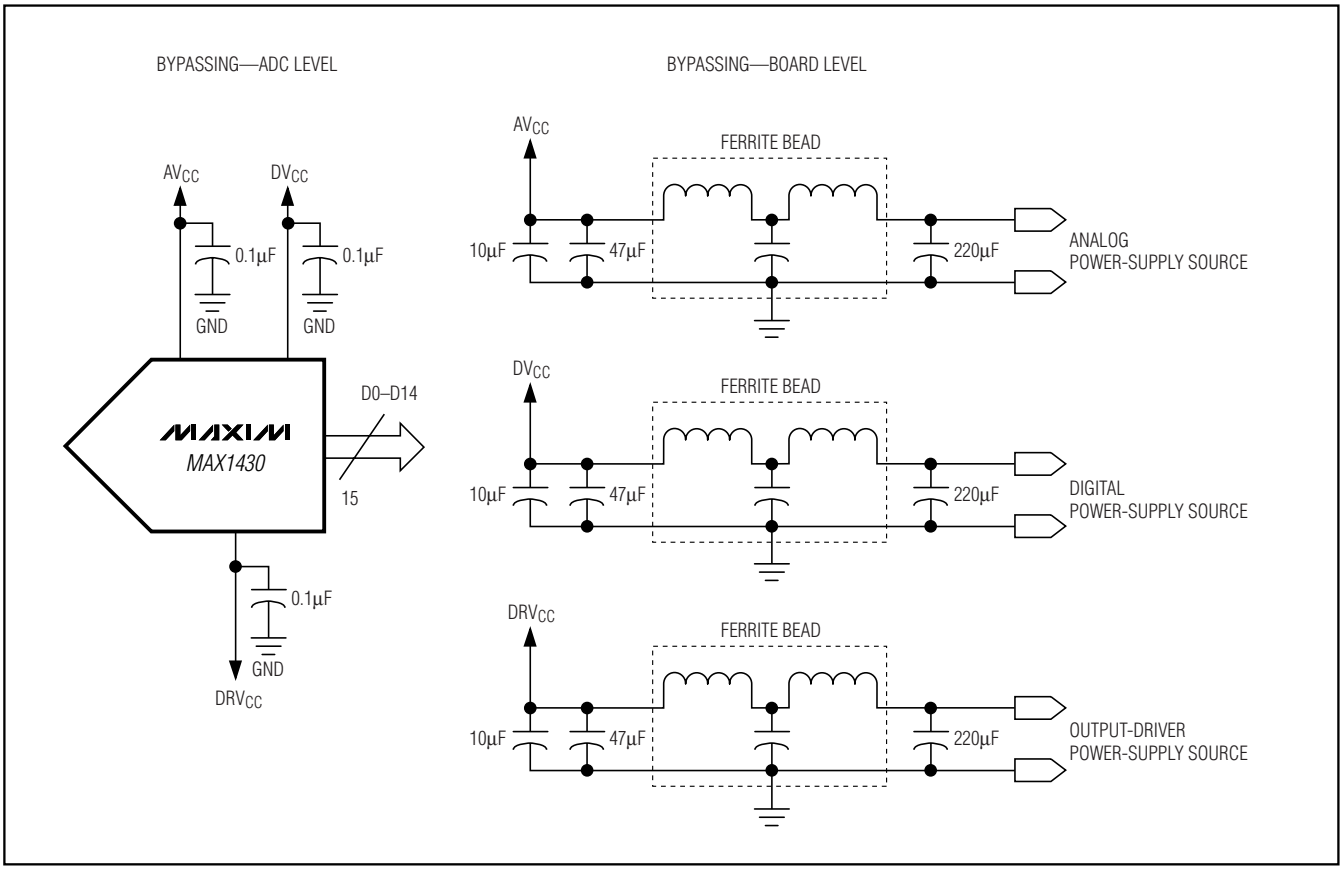


Figure 9. Grounding, Bypassing, and Decoupling Recommendations for MAX1430

15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

Differential Nonlinearly (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. The MAX1430's DNL specification is measured with the histogram method based on a 15MHz input tone.

Dynamic Parameter Definitions

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 4).

Aperture Jitter

The aperture jitter (t_{AJ}) is the sample-to-sample variation in the aperture delay.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, other noise sources such as thermal noise, clock jitter, signal phase noise, and transfer function nonlinearities are also contributing to the SNR calculation and should be considered when determining the SNR in ADC. For a near-full-scale analog input signal (-0.5dBFS to -1dBFS), thermal and quantization noise are uniformly distributed across the frequency bins. Error energy caused by transfer function nonlinearities on the other hand is not distributed uniformly, but confined to the first few hundred odd-order harmonics.

BTS applications, which are the main target application for the MAX1430 usually do not care about excess noise and error energy in close proximity to the carrier frequency or to DC. These low-frequency and sideband errors are test system artifacts and are of no consequence to the BTS channel sensitivity. They are therefore excluded from the SNR calculation.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components excluding the fundamental and the DC offset.

Single-Tone Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of the next-largest noise or harmonic distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the ADC's full-scale range.

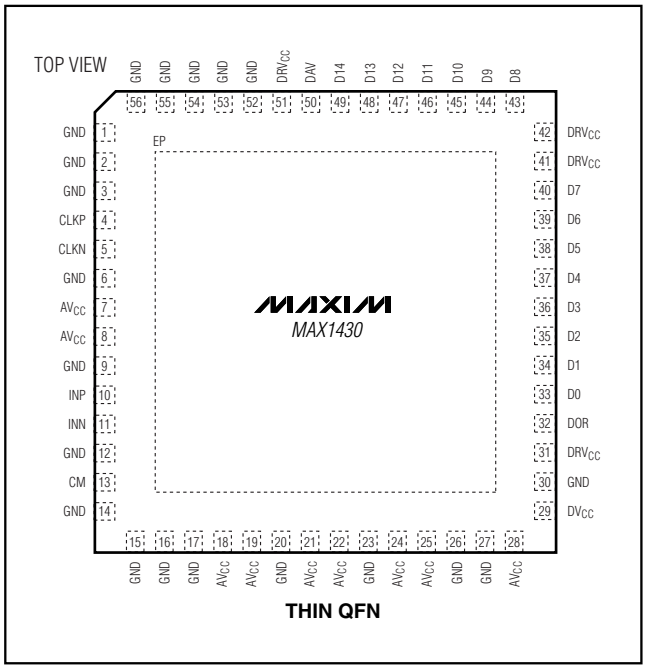
Two-Tone Spurious-Free Dynamic Range ($SFDR_{TT}$)

$SFDR_{TT}$ represents the ratio of the RMS value of either input tone to the RMS value of the peak spurious component in the power spectrum. This peak spur can be an intermodulation product of the two input test tones.

Two-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -8dB full scale.

Pin Configuration

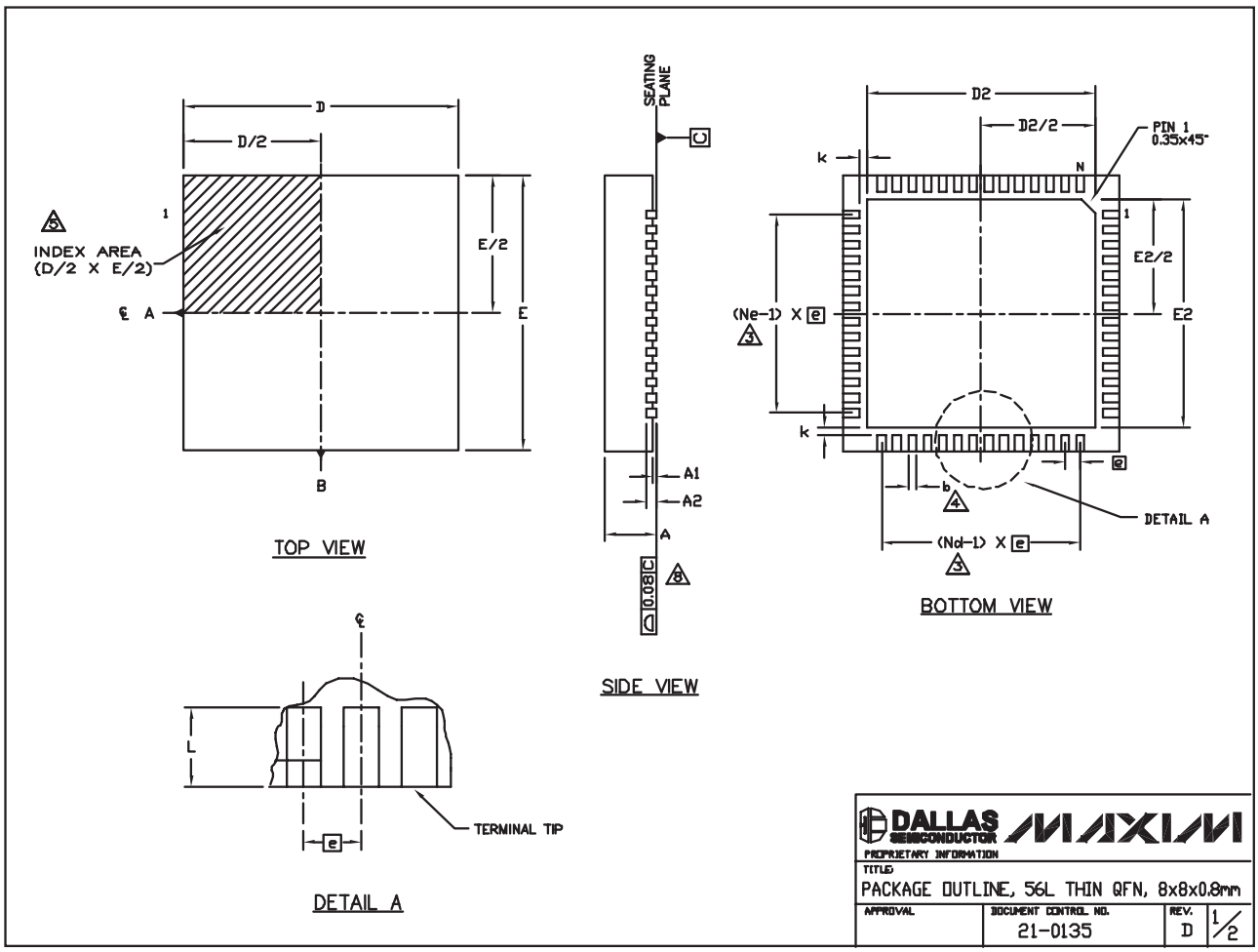


THIN QFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

56L THIN QFN.EPS



15-Bit, 100Msps ADC with -76.8dBFS Noise Floor for IF Applications

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.225mm MAXIMUM (0.009 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE WITHIN HATCHED AREA AS SHOWN.
   EITHER AN INDENTATION MARK OR INK/LASER MARK IS ACCEPTABLE.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. PACKAGE WARPAGE MAX 0.01mm.
8. APPLIES TO EXPOSED PAD AND TERMINALS.
   EXCLUDES INTERNAL DIMENSION OF EXPOSED PAD.
9. MEETS JEDEC MO220.

SYMBOL	56L 8x8			NOTE
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
b	0.20	0.25	0.30	4
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
e	0.50 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
A1	0.00	0.02	0.05	
A2	0.20 REF			
k	0.25	--	--	

PKG. CODE	EXPOSED PAD VARIATION						JEDEC	DOWN BONDS ALLOWED
	D2			E2				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T5688-1	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO
T5688-2	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	YES
T5688-3	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 56L THIN QFN, 8x8x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0135	D	2/2