

CMOS linear image sensors



S11106-10 S11107-10

Compact size and high cost-performance

The S11106-10 and S11107-10 are CMOS linear image sensors of resin sealing type that delivers a video data rate of 10 MHz and low current consumption. The pixel size is $63.5 \times 63.5 \mu m$ (S11106-10), $127 \times 127 \mu m$ (S11107-10).

Features

- **■** Compact size and high cost-performance
- Resin sealing type, surface mount package: 2.4 × 9.1 ×1.6^t mm
- Pixel size:

S11106-10: $63.5 \times 63.5 \ \mu\text{m}$, 128 pixels S11107-10: 127 \times 127 μm , 64 pixels

- → High-speed data rate: 10 MHz max.
- 3 V or 5 V single power supply operation
- Built-in timing generator allows operation with only Start and Clock pulse inputs
- Low current consumption
- Allows simultaneous charge integration

Applications

- Position detection
- Object measurement
- Rotary encoder
- **■** Image reading

Structure

Parameter	S11106-10	S11107-10	Unit		
Number of pixels	128	64	-		
Pixel pitch	63.5	127	μm		
Pixel height	63.5	127	μm		
Photosensitive area length	8.06				
Package	Glass epoxy				
Seal material	Silicon	-			

■ Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Operating temperature*1	Topr		-40 to +85	°C
Storage temperature*1	Tstg		-40 to +85	°C
Reflow soldering conditions*2	Tsol		Peak temperature 260 °C, 3 times (See p.11)	-

^{*1:} No condensation

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to the product within the absolute maximum ratings.

^{*2:} JEDEC level 2a

➡ Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Тур.	Max.	Unit
Supply voltage		Vdd	3.0	-	5.25	V
Clask pulsa valtaga	High level	V(CLK)	3.0	Vdd	Vdd + 0.25	V
Clock pulse voltage	Low level	V(CLK)	0	-	0.4	V
Start pulse voltage	High level	V(ST)	3.0	Vdd	Vdd + 0.25	V
	Low level	V(31)	0	-	0.4	V

➡ Electrical characterisitics (Ta=25 °C)

Parameter		Symbol	S11106-10			S11107-10			Unit
		Syllibol	Min.	Тур.	Max.	Min.	Тур.	Max.	Ullit
Clock pulse frequency		f(CLK)	5 k	-	10 M	5 k	-	10 M	Hz
Video data rate		VR	-	f(CLK)	-	-	f(CLK)	-	Hz
Output impedance		Zo	60	-	140	60	-	140	Ω
Current consumption*3	Vdd=3 V	т	4.0	6.0	8.0	2.5	4.5	6.5	m Λ
	Vdd=5 V	1	7.0	9.0	11.0	4.5	6.5	8.5	mA

^{*3:} f(CLK)=10 MHz, dark state, V(CLK)=V(ST)=Vdd

■ Electrical and optical characteristics [Ta=25 °C, Vdd=3 V/5 V, V(CLK)=V(ST)=Vdd, f(CLK)=10 MHz]

Parameter		Symbol		S11106-10		S11107-10			Linit
		Syllibol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Spectral response range		λ	4	100 to 1000)	4	100 to 100	0	nm
Peak sensitivity waveleng	gth	λр	-	700		-	700	-	nm
Photosensitivity*4		S	-	80	-	-	75	-	V/(<i>lx</i> ⋅s)
Conversion efficiency*5		CE	-	0.75	-	-	0.35	-	μV/e⁻
Output offset voltage		Vo	0.5	0.8	1.1	0.5	0.8	1.1	V
Dark output voltage*6		Vd	-	0.02	0.2	-	0.04	0.4	mV
Saturation output voltage*7	Vdd=3 V	Vsat	1.8	2.0	2.2	1.8	2.0	2.2	V
Saturation output voltage	Vdd=5 V		3.7	4.0	4.3	3.7	4.0	4.3	V
Readout noise*8	Vdd=3 V	- Nr	-	1.0	1.5	-	0.9	1.5	mV rms
Reducut Hoise	Vdd=5 V		-	0.7	1.2	-	0.6	1.1	IIIV IIIIS
Dynamic range 1*9	Vdd=3 V	DR1	-	2000	-	-	2200	-	times
Dynamic range 1"	Vdd=5 V	DKI	-	5700	-	-	6600	-	unies
Dynamic range 2*10	Vdd=3 V	DD2	-	100000	-	-	50000	-	times
	Vdd=5 V	DR2	-	200000	-	-	100000	-	umes
Photoresponse nonunifor	mity* ⁴ * ¹¹	PRNU	-	±2	±10	-	±2	±10	%

^{*4:} Measured with a 2856 K tungsten lamp

Appearance inspection standards

Parameter	Test criterion	Inspection method
Foreign matter on photosensitive area	10 μm max.	Automated camera



^{*5:} Output voltage generated per one electron

^{*6:} Integration time=10 ms

^{*7:} Voltage difference from Vo

^{*8:} Dark state

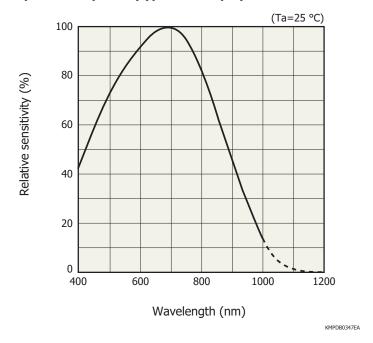
^{*9:} DR1 = Vsat/Nr

^{*10:} DR2 = Vsat/Vd

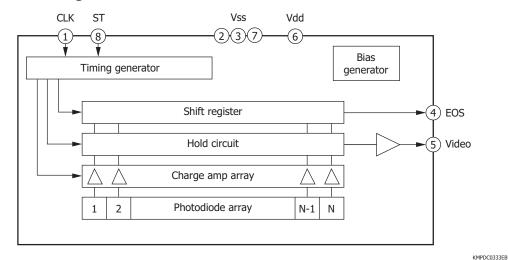
^{*11:} Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 112 pixels (S11106-10) excluding 8 pixels each at both ends or 56 pixels (S11107-10) excluding 4 pixels each at both ends, and is defined as follows: PRNU = $\Delta X/X \times 100 \, [\%]$

X: the average output of all pixels, ΔX : difference between X and maximum or minimum output

Spectral response (typical example)



Block diagram



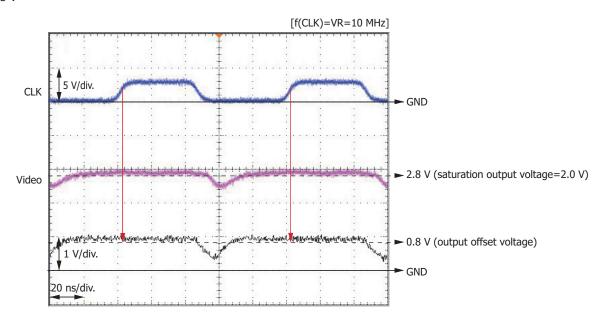
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- Output waveform of one pixel

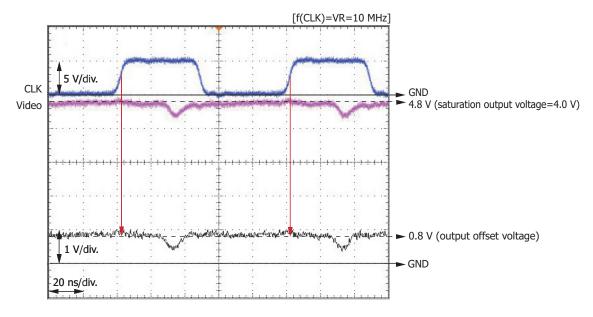
The timing for acquiring the Video signal is synchronized with the rising edge of CLK (See red arrow below).

S11106-10

■Vdd=3 V

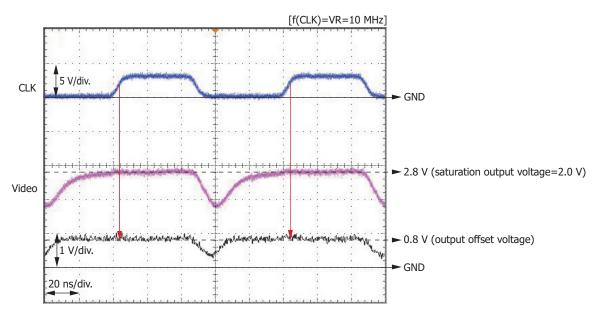


■Vdd=5 V

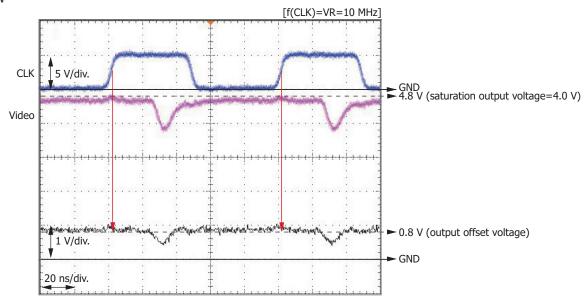


S11107-10

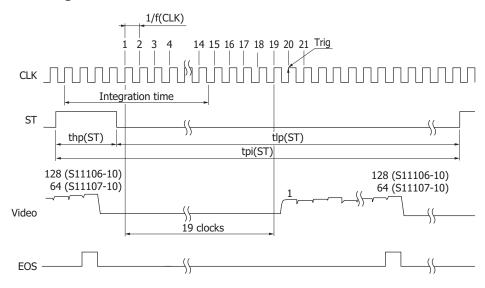
■Vdd=3 V

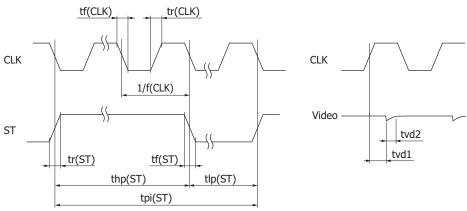


■Vdd=5 V



- Timing chart





KMPDC0515E

Parameter		Symbol		S11106-10			S11107-10		
		Syllibol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Start pulse interval		tpi(ST)	36/f(CLK)	-	-	36/f(CLK)	-	-	S
Start pulse high period	b	thp(ST)	4/f(CLK)	-	-	4/f(CLK)	-	-	S
Start pulse low period		tlp(ST)	32/f(CLK)	-	-	32/f(CLK)	-	-	S
Start pulse rise and fa	ll times	tr(ST), tf(ST)	0	10	15	0	10	15	ns
Clock pulse duty ratio		-	45	50	55	45	50	55	%
Clock pulse rise and fa	all times	tr(CLK), tf(CLK)	0	10	15	0	10	15	ns
Video delay time 1*12	Vdd=3 V	tvd1	-	60	-	-	60	-	ns
video delay time 1 12	Vdd=5 V		-	35	-	-	35	-	115
Video delay time 1×14	Vdd=3 V	tvd2	-	35	-	-	35	-	ns
video delay time 2	Vdd=5 V	ιναΖ	-	30	-	-	30	-	115

^{*12:} Ta=25 °C, CLK=10 MHz, V(CLK)=V(ST)=Vdd

Note: Dark output increases if the start pulse period or the start pulse high period is lengthened.

The internal timing generator starts operation at the rising edge of CLK immediately after ST goes low. The rising edge of this CLK is regarded as "1".

The integration time equals the high period of ST plus 14 CLK cycles and minus 100 ns.

When the ST pulse is set to low while the shift register is operating, the operation of the shift register is reset and the next shift register operation will start.

The integration time can be changed by changing the ratio of the high and low periods of ST.



Operation example

S11106-10

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (for outputting signals from all 128 channels)

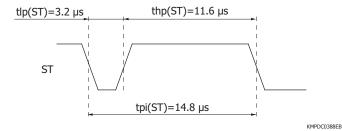
Clock pulse frequency = Video data rate = 10 MHz

Start pulse cycle = $148/f(CLK) = 148/10 \text{ MHz} = 14.8 \mu s$

High period of start pulse = Start pulse cycle - Start pulse's low period min.

= $148/f(CLK) - 32/f(CLK) = 148/10 \text{ MHz} - 32/10 \text{ MHz} = 11.6 \mu s$

Integration time is equal to the high period of start pulse + 14 cycles of clock pulses - 100 ns, so it will be $11.6 + 1.4 - 0.1 = 12.9 \mu s$.



S11107-10

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (for outputting signals from all 64 channels)

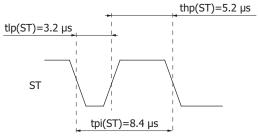
Clock pulse frequency = Video data rate = 10 MHz

Start pulse cycle = 84/f(CLK) = 84/10 MHz = $8.4 \mu s$

High period of start pulse = Start pulse cycle - Start pulse's low period min.

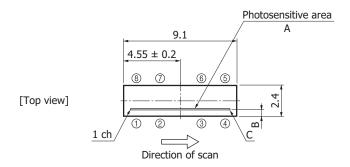
= $84/f(CLK) - 32/f(CLK) = 84/10 \text{ MHz} - 32/10 \text{ MHz} = 5.2 \mu s$

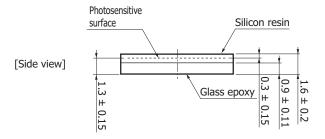
Integration time is equal to the high period of start pulse + 14 cycles of clock pulses - 100 ns, so it will be $5.2 + 1.4 - 0.1 = 6.5 \mu s$.



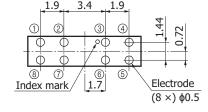
KMPDC0389EB

Dimensional outline (unit: mm)





[Bottom view]



Tolerance unless otherwise noted: ±0.2

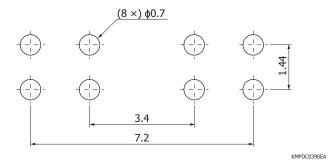
Type no.	А	В	С
S11106-10	8.06×0.0635	0.4	128 ch
S11107-10	8.06×0.127	0.5	64 ch

KMPDA0314EB

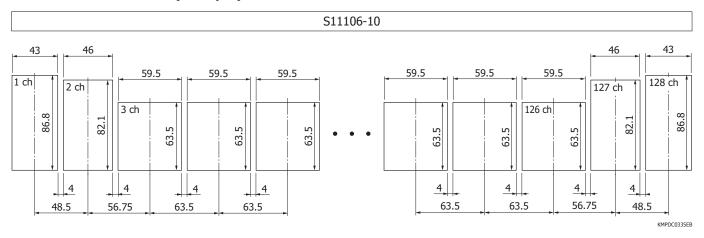
- Pin connections

Pin no.	Symbol	Description	Input/Output
1	CLK	Clock pulse	Input
2	Vss	Ground	-
3	Vss	Ground	-
4	EOS	End of scan	Output
5	Video	Video signal	Output
6	Vdd	Supply voltage	Input
7	Vss	Ground	-
8	ST	Start pulse	Input

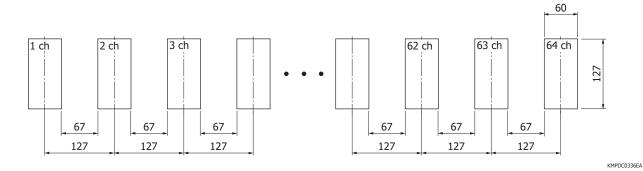
- Recommended land pattern



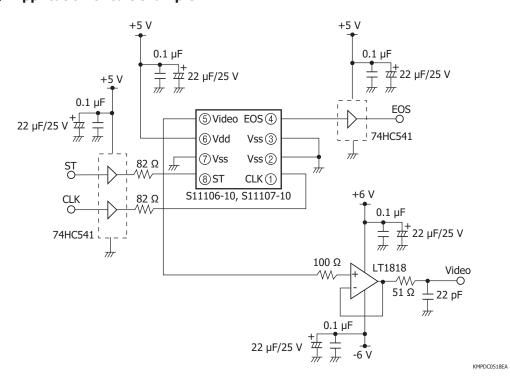
- Details of active area (unit: μm)



S11107-10



- Application circuit example

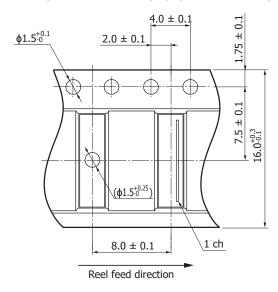


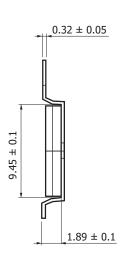
Standard packing specifications

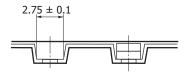
■ Reel (conforms to JEITA ET-7200)

Dimensions	Hub diameter	Tape width	Material	Electrostatic characteristics
330 mm	100 mm	16 mm	PPE	Conductive

■ Embossed (unit: mm, material: polystyrene, conductive)







KMPDC0451EA

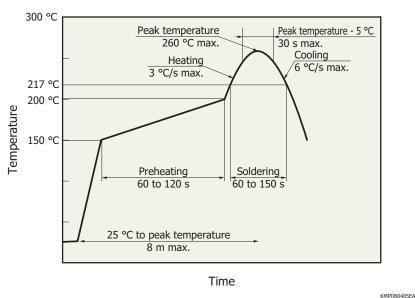
■ Packing quantity 2000 pcs/reel

Packing specifications may vary on orders less than 2000 pieces.

■ Packing type

Reel and desiccant in moisture-proof packing (vaccum-sealed)

Recommended temperature profile for reflow soldering (typical example)



- This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 4 weeks.
- The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by tesitng out the reflow soldering methods in advance.
- · When three or more months have passed or if the packing bag has not been stored in an environment described above, perform baking. For the baking method, see the precautons "Resin sealed type CMOS linear image sensors."

Precautions

(1) Electrostatic countermeasures

- This device has a built-in protection circuit as a safeguard against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools.
- · Protect this device from surge voltages which might be caused by peripheral equipment.

(2) Package handling

- The photosensitive area of this device is sealed and protected by transparent resin. When compared to a glass faceplate, the surface of transparent resin may be less uniform and is more likely to be scratched. Be very careful when handling this device and also when designing the optical systems.
- · Dust or grime on the light input window might cause nonuniform sensitivity. To remove dust or grime, blow it off with compressed air.

(3) Surface protective tape

· Protective tape is affixed to the surface of this product to protect the photosensitive area. After assembling the product, remove the tape before use.

(4) Operating and storage environments

· Handle the device within the temperature range specified in the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

(5) UV exposure

This product is not designed to prevent deterioration of characteristics caused by UV exposure, so do not expose it to UV light.



Related information

www.hamamatsu.com/sp/ssd/doc_en.html

- Precautions
- · Notice
- · Image sensor
- · Resin-sealed CMOS linear image sensors

Information described in this material is current as of August 2014.

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