STK5U4UFB0D-E

Product Preview
Intelligent Power Module (IPM)
1200 V, 25 A

The STK5U4UFB0D-E is a fully-integrated inverter power module consisting of an independent gate driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a three-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.
The power stage has undervoltage lockout protection (UVP) and V_{CE} desaturation protection (DESATP) with a fault detection output flag. Internal boost diodes are provided for high side gate boost drive.

Features

- Three-phase 1200 V, 25 A IGBT module with independent drivers.
- Negative logic interface.
- Built-in undervoltage protection (UVP) and V_{CE} desaturation Protection (DESATP) with a fault detection output flag.
- Integrated bootstrap diodes and resistors.
- Separate low-side IGBT emitter connections for individual current sensing of each phase.
- Thermistor

Typical Applications

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation

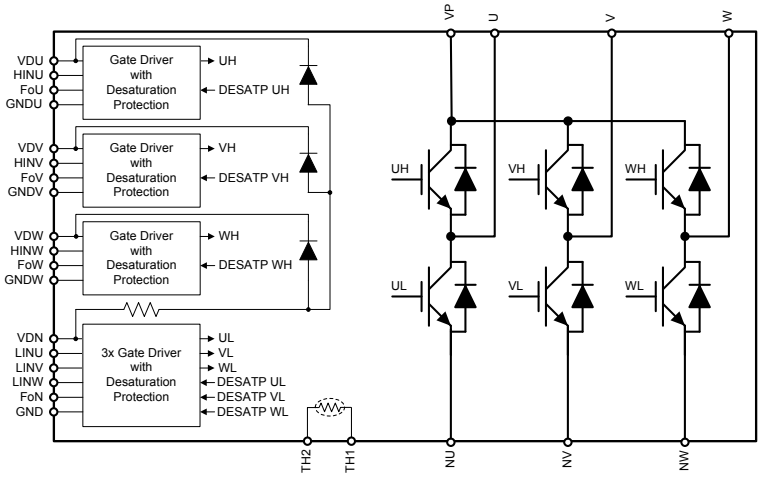

Figure 1. Functional Diagram

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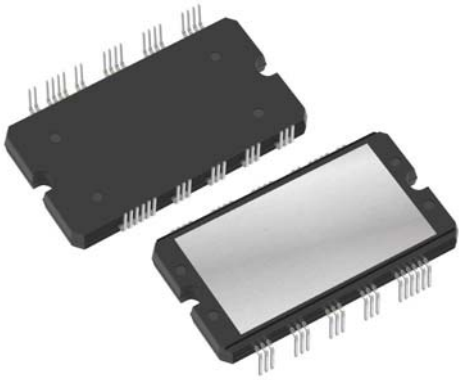
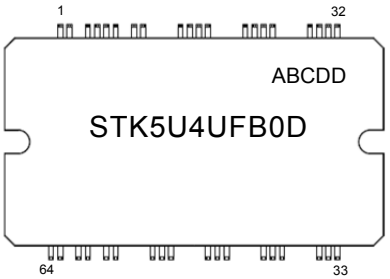
PACKAGE PICTURE



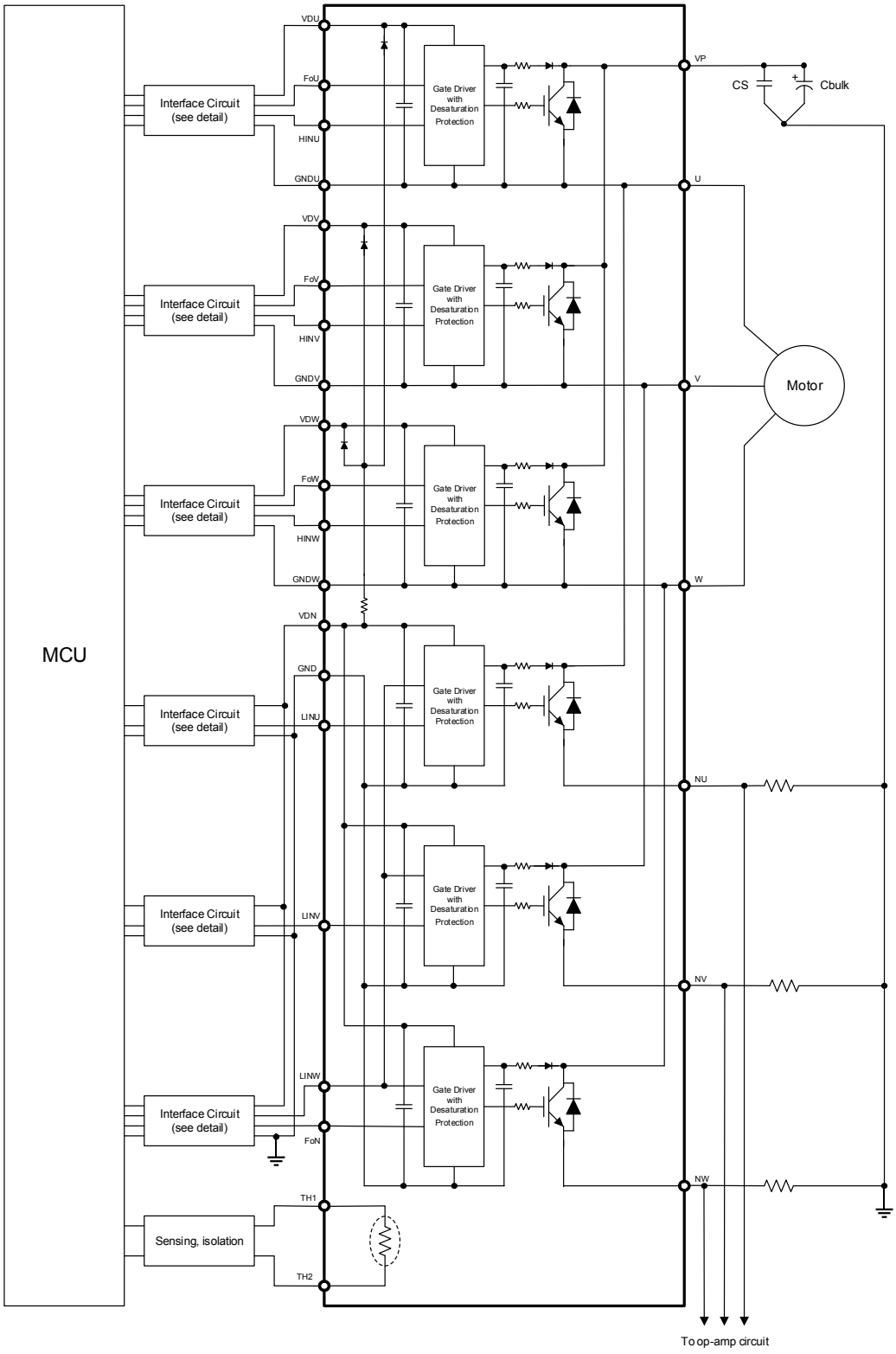
MARKING DIAGRAM



STK5U4UFB0D = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot Code

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5U4UFB0D-E	TBD	TBD



Sample interface circuit detail

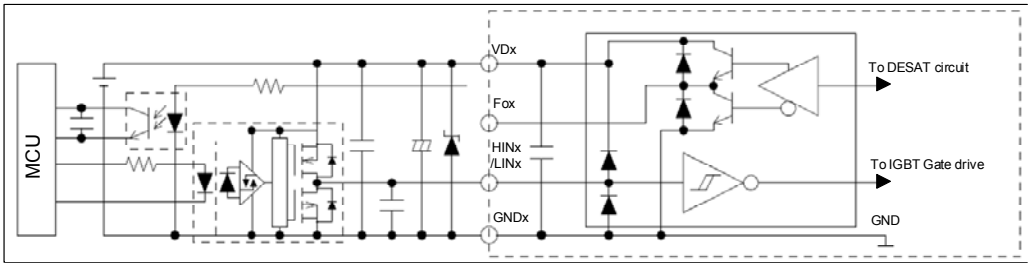


Figure 2. Application Schematic

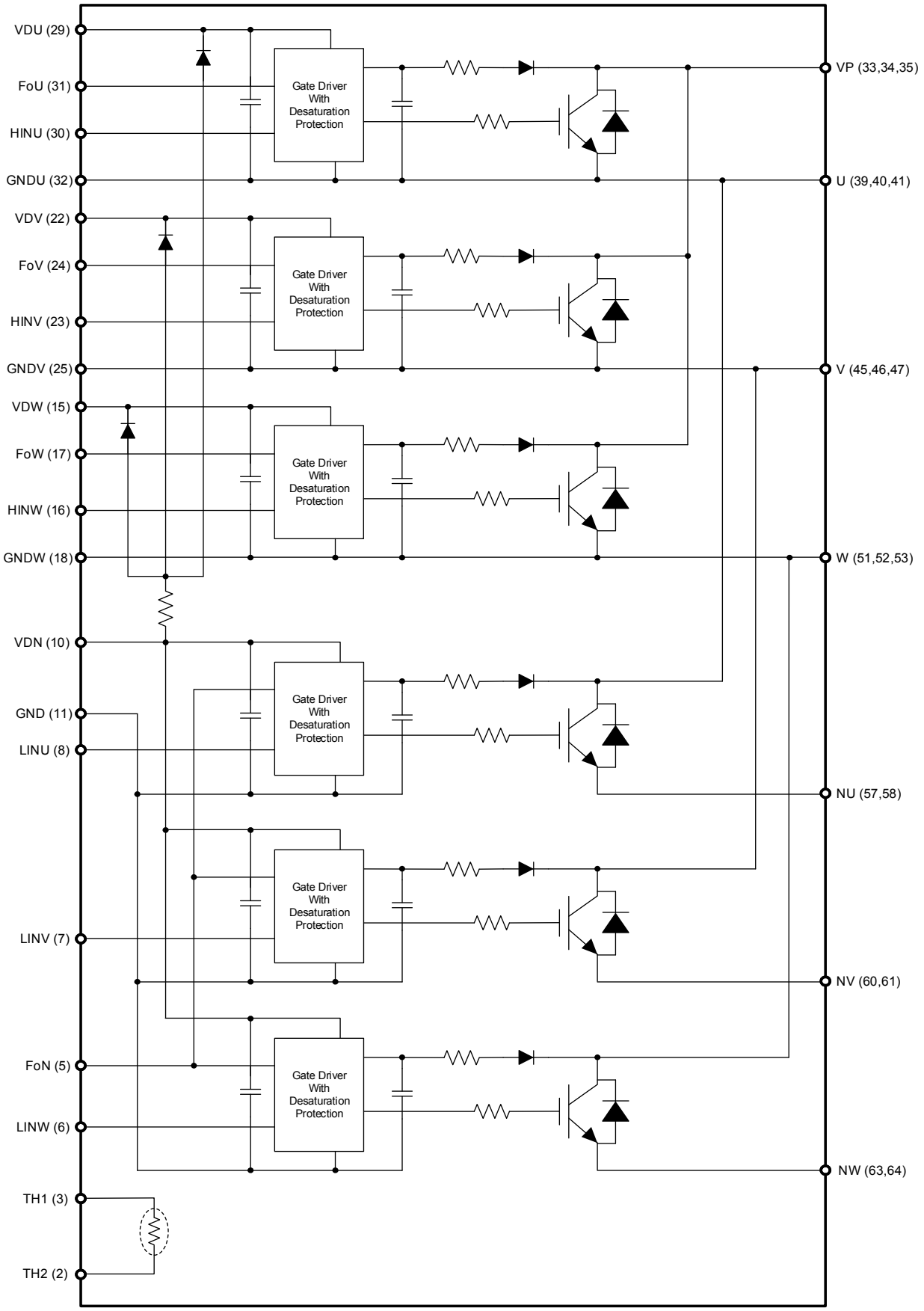


Figure 3. Equivalent Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Description
2	TH1	Thermistor connection
3	TH2	Thermistor connection
5	FoN	Fault output low side
6	LINW	Logic Input Low Side Gate Driver - Phase W
7	LINV	Logic Input Low Side Gate Driver - Phase V
8	LINU	Logic Input Low Side Gate Driver - Phase U
10	VDN	Control power supply low side
11	GND	Control power GND low side
15	VDW	Control power supply high side – Phase W
16	HINW	Logic input high side – Phase W
17	FoW	Fault output high side – Phase W
18	GNDW	Control power GND high side – Phase W
22	VDV	Control power supply high side – Phase V
23	HINV	Logic input high side – Phase V
24	FoV	Fault output high side – Phase V
25	GNDV	Control power GND high side – Phase V
29	VDU	Control power supply high side – Phase U
30	HINU	Logic input high side – Phase U
31	FoU	Fault output high side – Phase U
32	GNDU	Control power GND high side – Phase U
33,34,35	VP	Positive Bus Input Voltage
39,40,41	U	U Phase Output
45,46,47	V	V Phase Output
51,52,53	W	W Phase Output
57,58	NU	Low Side Emitter Connection - Phase U
60,61	NV	Low Side Emitter Connection - Phase V
63,64	NW	Low Side Emitter Connection - Phase W

Note : Pins 1, 4, 9, 12, 13, 14, 19, 20, 21, 26, 27, 28, 36, 37, 38, 42, 43, 44, 48, 49, 50, 54, 55, 56, 59 and 62 are not present

ABSOLUTE MAXIMUM RATINGS at Tc = 25°C (Notes 1, 2)

Rating	Symbol	Conditions	Value	Unit
Supply voltage	V_{CC}	VP to NU, NV, NW, surge < 1000 V (Note 3)	900	V
Collector-emitter voltage	V_{CE}	VP to U, V, W; U to NU, V to NV, W to NW	1200	V
Self-protection supply voltage limit (DESATP capability)	V_{CC}(SC)	VD1, 2, 3, 4 = between 13.5 V and 16.5 V, Tj ≤ 150°C, up to “tdesatbl”, non-repetitive	800	V
Output current	Io	VP, NU, NV, NW, U, V, W terminal current	±25	A
Output peak current	Iop	VP, NU, NV, NW, U, V, W terminal current pulse width 1 ms	±50	A
Gate driver supply voltages	VD	VDU to GNDU, VDV to GNDV, VDW to GNDW, VDN to GND (Note 4)	−0.3 to VD	V
Input signal voltage	VIN	HINU to GNDU, HINV to GNDV, HINW to GNDW; LINU, LINV, LINW to GND	−0.3 to VD	V
FAULT terminal voltage	VFo	FoU to GNDU, FoV to GNDV, FoW to GNDW, FoN to GND	−0.3 to VD	V
Fault output	IFo	FoU, FoV, FoW, FoN Source current	25	mA
		FoU, FoV, FoW, FoN Sink current	10	
Maximum power dissipation	Pd	IGBT per channel	TBD	W
Junction temperature	Tj	IGBT, FRD	150	°C
Storage temperature	Tstg		−40 to +125	°C
Operating case temperature	Tc	IPM case temperature	−40 to +100	°C
Package mounting torque		Case mounting screw M4 (Note 5)	1.17	Nm
Isolation voltage	Vis	50 Hz sine wave AC 1 minute	2500	V rms

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This surge voltage developed by the switching operation due to the wiring inductance between VP and NU, NV, NW terminal.
4. VD1 = VDU to GNDU, VD2 = VDV to GNDV, VD3 = VDW to GNDW, VD4 = VDN to GND
5. Flatness tolerance of the heatsink should be within −50 μm to +100 μm.

RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}	VP to NU, NV, NW	0	-	800	V
Gate driver supply voltage	VD1, 2, 3	VDU to GNDU, VDV to GNDV, VDW to GNDW	12.6	15	17.5	V
	VD4	V_{DD} to GND	13.5	15	16.5	V
ON-state input voltage	VIN(ON)	HINU to GNDU, HINV to GNDV, HINW to GNDW; LINU, LINV, LINW to GND	0	-	0.7	V
OFF-state input voltage	VIN(OFF)		3.3	-	15	V
PWM frequency	fPWM		1	-	20	kHz
Dead time	DT	Turn-off to Turn-on (external)	2	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Package mounting torque		M4 type screw	0.79	-	1.17	Nm

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS at Tc = 25°C, VD = 15 V (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power output section						
Collector-emitter leakage current	V_{CE} = 1200 V	I_{CE}	-	-	1	mA
Collector to emitter saturation voltage	IC = 25 A, Tj = 25°C	V_{CE}(SAT)	-	(2.1)	TBD	V
	IC = 25 A, Tj = 100°C		-	(2.2)	-	V
Diode forward voltage	IF = 25 A, Tj = 25°C	VF	-	(2.5)	TBD	V
	IF = 25 A, Tj = 100°C		-	(2.8)	-	V
Junction to case thermal resistance	IGBT	θj-c(T)	-	(0.74)	TBD	°C/W
	FWD	θj-c(D)	-	(1.06)	TBD	°C/W
Switching time	IC = 25 A, V_{CC} = 600 V, Tj = 25°C	t_{ON}	-	(0.2)	-	μs
		t_{OFF}	-	(0.6)	-	μs
Turn-on switching loss	IC = 25 A, V_{CC} = 600 V, Tj = 25°C	E_{ON}	-	(2.0)	-	mJ
Turn-off switching loss		E_{OFF}	-	(0.8)	-	mJ
Total switching loss		E_{TOT}	-	(2.8)	-	mJ
Turn-on switching loss	IC = 25 A, V_{CC} = 600 V, Tj = 100°C	E_{ON}	-	(2.3)	-	mJ
Turn-off switching loss		E_{OFF}	-	(1.1)	-	mJ
Total switching loss		E_{TOT}	-	(3.4)	-	mJ
Diode reverse recovery energy	IC = 25 A, V_{CC} = 600 V, Tj = 100°C (di/dt set by internal driver)	E_{REC}	-	(0.3)	-	mJ
Diode reverse recovery time		trr	-	(0.2)	-	μs
Driver Section						
Gate driver power dissipation	VD1, 2, 3 = 15 V	ID	-	8	17	mA
	VD4 = 15 V		-	24	51	mA
High level Input voltage	HINU to GNDU, HINV to GNDV, HINW to GNDW; LINU, LINV, LINW to GND	VIN H	3.2	-	-	V
Low level Input voltage		VIN L	-	-	1.2	V
Logic 1 input current	VIN = 3.0 V	I_{IN+}	-	-	500	μA
Logic 0 input current	VIN = 1.2 V	I_{IN-}	-	-	100	μA
FAULT terminal output voltage	FoU, FoV, FoW, FoN Sink: 5 mA	VFL	-	0.2	1	V
	FoU, FoV, FoW, FoN Source: 20 mA	VFH	12	13.3	-	V
Desaturation protection blanking time		tdeasatbl	-	2	-	μs
VD supply undervoltage positive going input threshold		V_{DUVP+}	11.3	12	12.6	V
VD supply undervoltage negative going input threshold		V_{DUVP-}	10.4	11	11.7	V
Bootstrap diode reverse current	VR(BD) = 1200 V	IR(BD)	-	-	1	mA
Bootstrap diode forward voltage	IF(BD) = 0.1 A Including voltage drop by resistor	VF(BD)	-	(2.6)	-	V
Bootstrap current controlling resistor		RB	-	15	-	Ω

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

APPLICATIONS INFORMATION

Logic and Protection Timing Chart

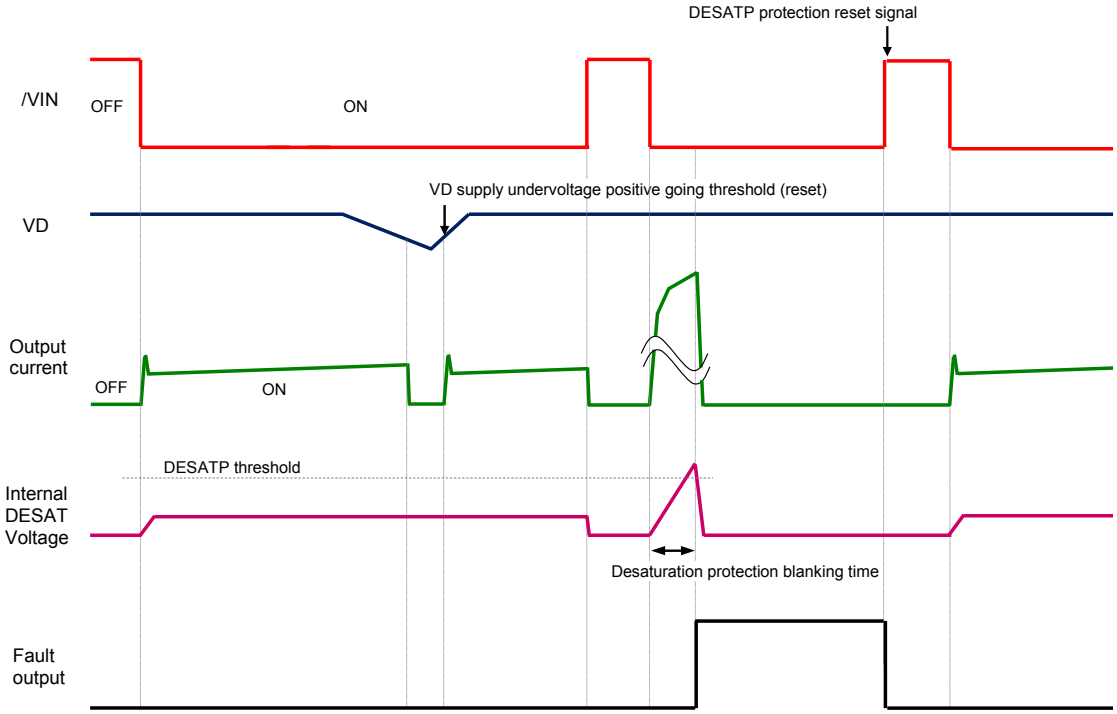


Figure 4. Logic and Protection Timing Chart

Notes

1. The VD supply undervoltage protection the module when the pre-driver supply voltage falls due to an operating malfunction. It will typically start up at 12 V (typical). The UVP circuit has typically 1 V of hysteresis and will disable the output if the supply voltage falls below 11 V (typical). The driver power supply low voltage protection turns off the gate and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.
2. The three high-side and three low-side gate driver ICs have their own separate undervoltage protection which functions independently of the other phases. For the low-side drivers, there is one combined fault output; it is therefore not possible to determine which output has caused the desaturation fault. The fault condition is cleared as soon as the input signal is set HIGH (off state, negative logic levels).
3. When using the over-current protection with an external shunt resistor, please set the current protection level to be less than or equal to the peak output current rating (Iop).

Input / Output Logic Table

	Protected Operation	IGBT output						Fault output			
		High side			Low side			High side			Low side
		U	V	W	U	V	W	U	V	W	
High side - U	UVP	OFF	-	-	-	-	-	Low	Low	Low	Low
	DESATP	OFF	-	-	-	-	-	High	Low	Low	Low
High side - V	UVP	-	OFF	-	-	-	-	Low	Low	Low	Low
	DESATP	-	OFF	-	-	-	-	Low	High	Low	Low
High side - W	UVP	-	-	OFF	-	-	-	Low	Low	Low	Low
	DESATP	-	-	OFF	-	-	-	Low	Low	High	Low
Low side - U	UVP	-	-	-	OFF	OFF	OFF	Low	Low	Low	Low
	DESATP	-	-	-	OFF	-	-	Low	Low	Low	High
Low side - V	UVP	-	-	-	OFF	OFF	OFF	Low	Low	Low	Low
	DESATP	-	-	-	-	OFF	-	Low	Low	Low	High
Low side - W	UVP	-	-	-	OFF	OFF	OFF	Low	Low	Low	Low
	DESATP	-	-	-	-	-	OFF	Low	Low	Low	High

*) - (hyphen) follows the actual input signals using negative logic (e.g. LINU = LOW turns on the low-side U phase IGBT).

Thermistor characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	97	100	103	kΩ
Resistance	R_{100}	Tc = 100°C	5.07	5.38	5.71	kΩ
B-Constant (25-50°C)	-	B	4208	4250	4293	K
Temperature range	-	-	−40	-	+125	°C

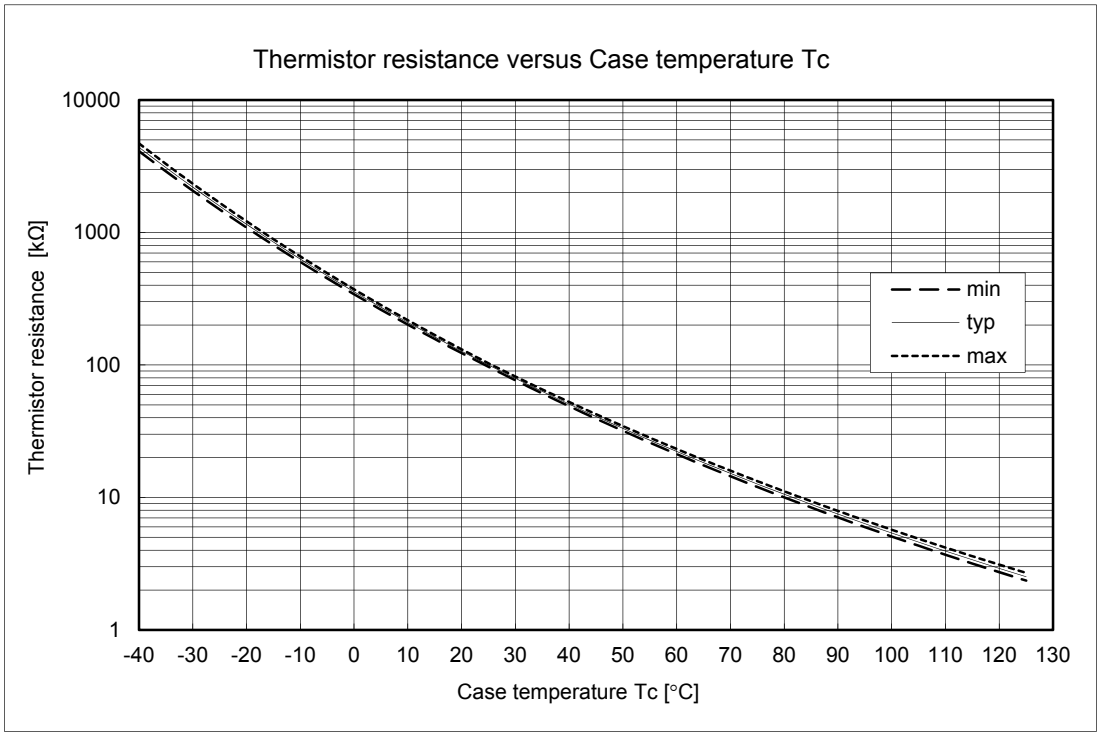


Figure 5. Thermistor Resistance versus Case Temperature

Undervoltage lockout protection (UVP)

If VD goes below the VD supply undervoltage negative going input threshold, the IGBT gate drives will be turned off. If VD rises above the positive going input threshold, the IGBT gate drivers will return to normal operation. The Fox signal outputs stay low during the UVP state. The UVP does not depend on input signal voltage.

Desaturation Protection function (DESATP)

The Desaturation Protection function (DESATP) is implemented by comparing the voltage between the collector and the emitter of IGBT with an internal reference of 6.5 V (typ). If a short circuit occurs after the IGBT is turned on and saturated, there will be a delay while the blanking capacitor is charged from the V_{CE}(sat) level of the IGBT to the trip voltage of the comparator. If the collector voltage exceeds the trip level, a DESATP fault is triggered and the Fox signal (FoU, FoV, FoW, FoN) is set HIGH. The fault condition is cleared after the input signal is set to inactive (HIGH due to negative logic on input).
Additional protection against abnormal current levels such as a protection circuit using external shunt resistors, and a fuse on the input voltage line is strongly recommended.

Capacitors on High Voltage and VD supplies

Both the high voltage and VD supplies require an electrolytic capacitor and an additional high frequency capacitor.

Disconnection of U, V and W terminals

Disconnection of terminals U, V, or W during normal motor operation will cause damage to IPM, use caution with this connection.

Minimum input pulse width

When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON and OFF signal)

Layout

The traces between the IPM terminals and each optocoupler must be as short as possible, and the stray capacitance between the primary and the secondary must be considered in order to select a layout pattern.
It is essential that trace length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of "CS" is in the range of 0.1 to 10 μF. This capacitor should be a high frequency capacitor.

Thermistor

Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between "TH1" and "TH2". The variation of thermistor resistance with temperature is shown in this datasheet.

Dimensioning of bootstrap capacitor

The module includes an internal bootstrap circuit requiring one bootstrap capacitor for each phase, each with a value CB. The recommended value of CB is in the range of 1 to 47 μF, however, this value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent floating power supply. If the selected capacitance is more than 47 μF (±20%), connect a resistor (about 40 Ω) in series between each three-phase upper side power supply terminals (VDU, VDV, VDW) and each bootstrap capacitor. When not using the bootstrap circuit, each upper side gate driver power supply requires an external independent floating power supply.
Also we recommend adopting safety measures such as using Zener diodes for surge absorption or low impedance capacitors around each power supply terminal to suppress voltage transients.

CB value calculation for bootstrap circuit

Calculate condition

Item	Symbol	Value	Unit
High-side power supply.	VD1,2,3	15	V
Total gate charge of output power IGBT at 15 V.	Qg	220	nC
High-side power supply undervoltage protection.	UDUVP-	12	V
High-side power dissipation.	ID max	17	mA
ON time required for CB voltage to fall from 15 V to UVP	Ton-max	-	s

Capacitance calculation formula

CB must not be discharged below to the upper limit of the UVP - the maximum allowable on-time (Ton-max) of the upper side is calculated as follows:

VD1, 2, 3 * CB – Qg – ID max * Ton-max = UVP * CB

CB = (Qg + ID max * Ton-max) / (VD1, 2, 3 – UVP)

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production.

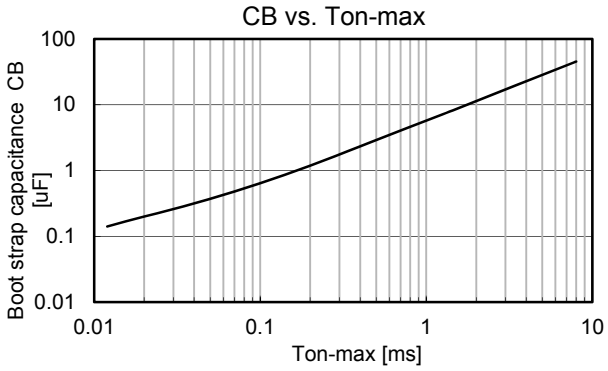


Figure 6. Bootstrap selection as a function of maximum ON time

Mounting Instructions

Item	Recommended Condition
Pitch	67.8 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	diameter : M4 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer The size is D : 9 mm, d : 4.8 mm and t : 0.8 mm JIS B 1256
Heat sink	Material : Aluminum or Copper Warpage (the surface that contacts IPM) : −50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening : 20 to 30% of final tightening on first screw Temporary tightening : 20 to 30% of final tightening on second screw Final tightening : 0.79 to 1.17 Nm on first screw Final tightening : 0.79 to 1.17 Nm on second screw
Grease	Silicone grease. Thickness : 100 to 200 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

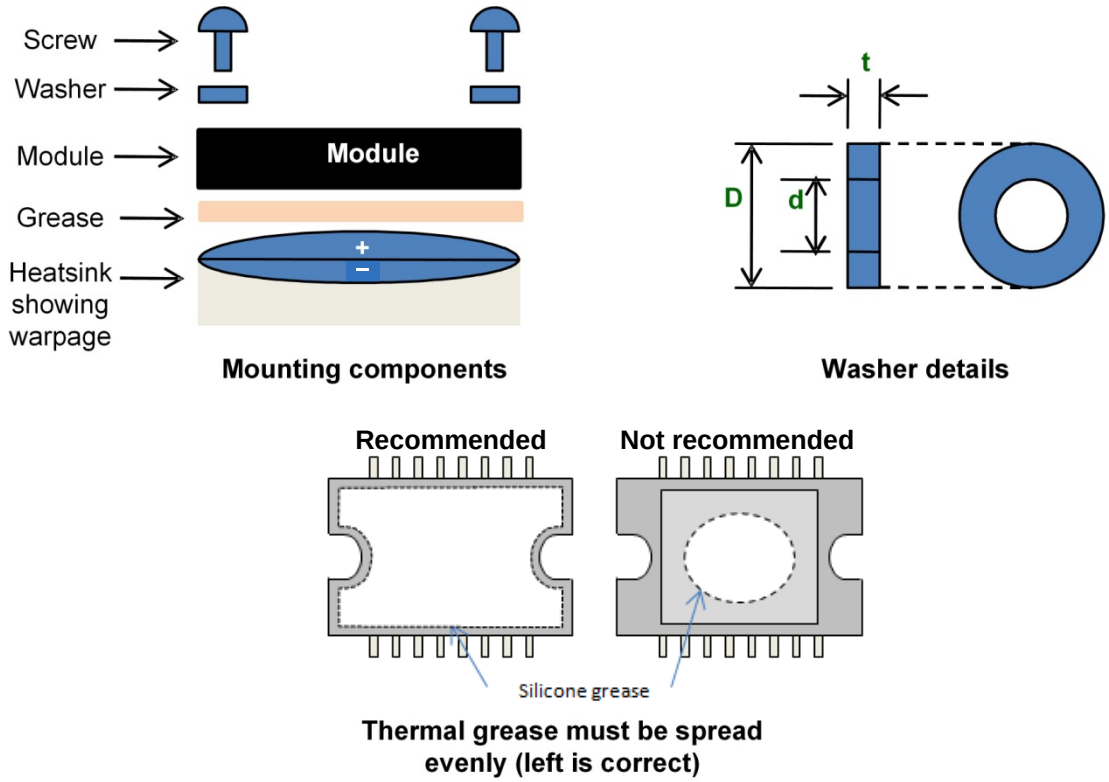


Figure 7. Module mounting details: components; washer drawing; need for even spreading of thermal grease

TYPICAL CHARACTERISTICS

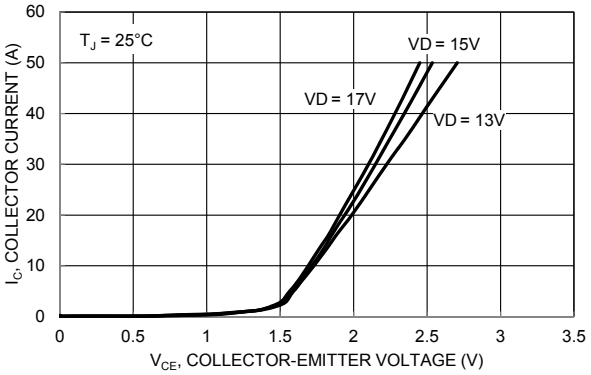


Figure 8. IC versus V_{CE} for different VD

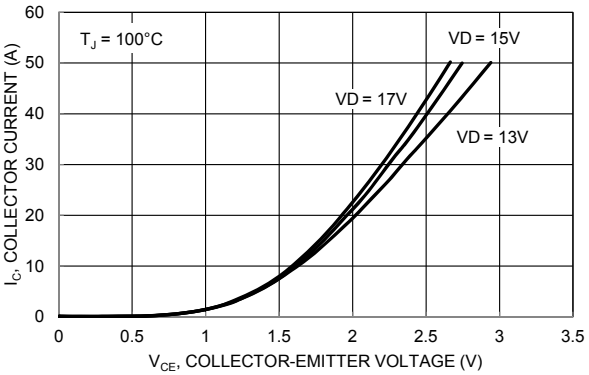


Figure 9. IC versus V_{CE} for different VD

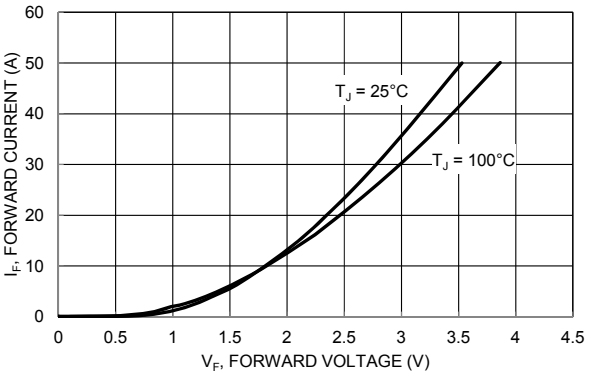


Figure 10. IF versus VF for different temperatures

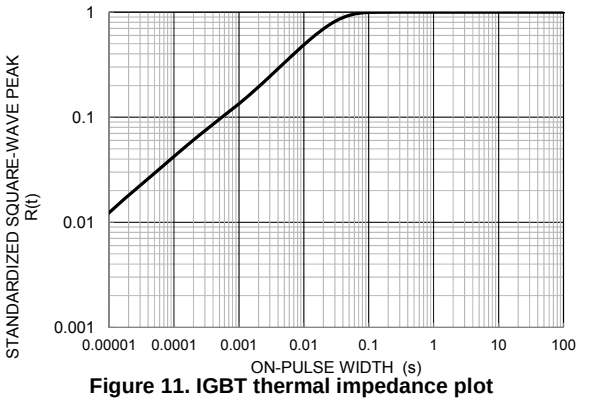


Figure 11. IGBT thermal impedance plot

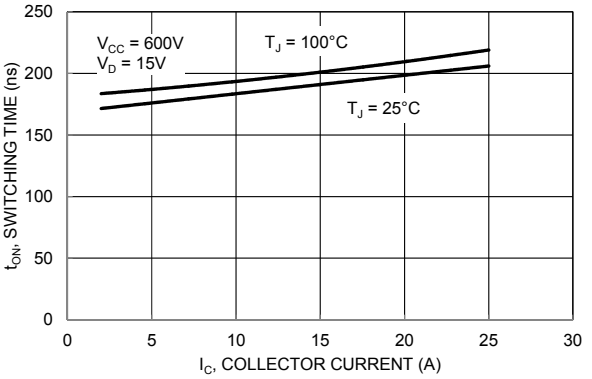


Figure 12. ton versus IC for different temperatures

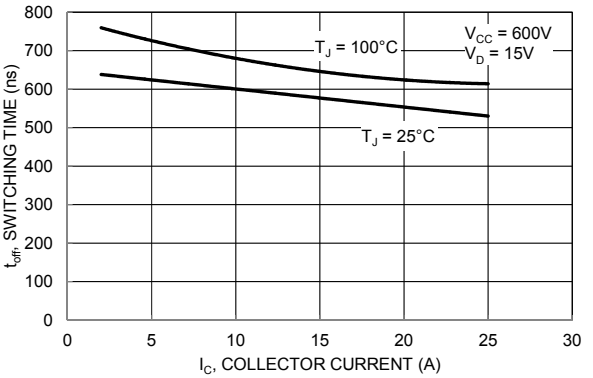


Figure 13. toff versus IC for different temperatures

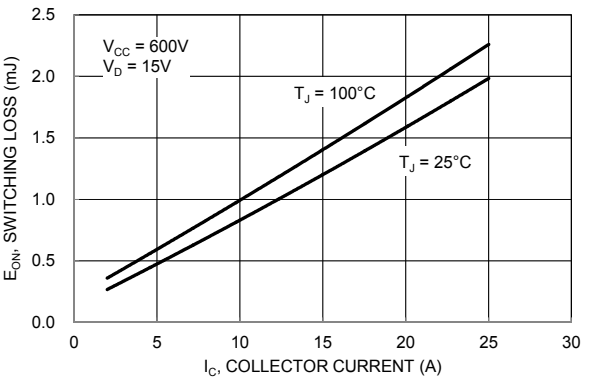


Figure 14. Eon versus IC for different temperatures

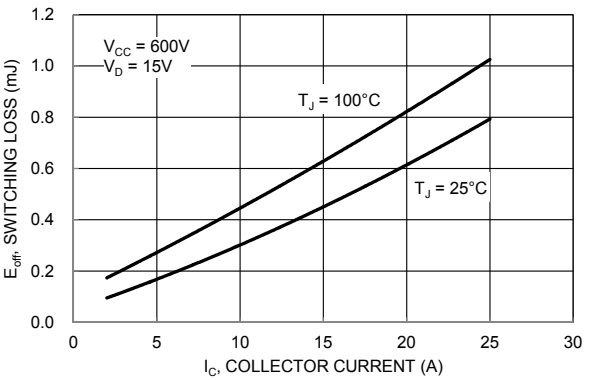


Figure 15. Eoff versus IC for different temperatures

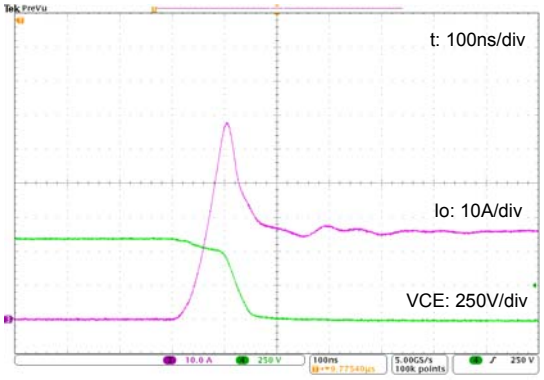


Figure 16. Turn-on waveform Tj = 25°C, V_{CC} = 600 V

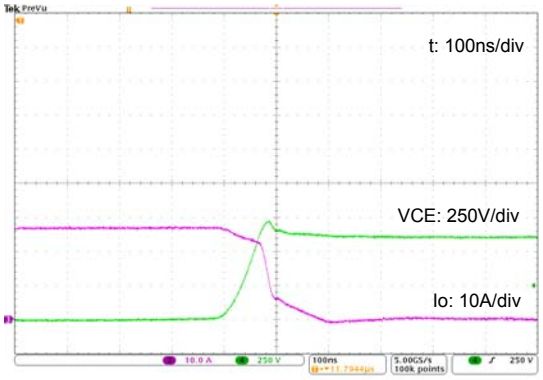


Figure 17. Turn-off waveform Tj = 25°C, V_{CC} = 600 V

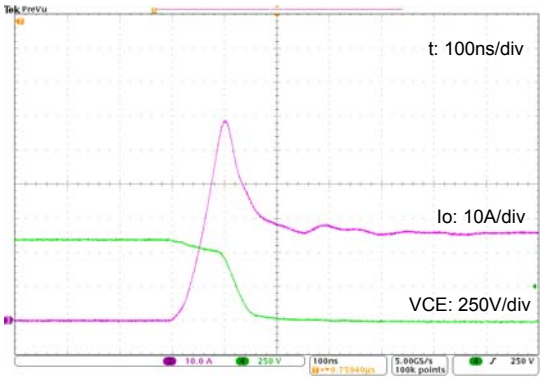


Figure 18. Turn-on waveform Tj = 100°C, V_{CC} = 600 V

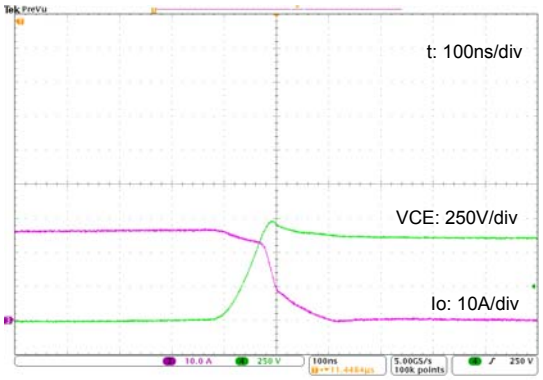


Figure 19. Turn-off waveform Tj = 100°C, V_{CC} = 600 V

PACKAGE DIMENSIONS
unit : mm

[TENTATIVE]

Missing pins : 1, 4, 9, 12, 13, 14, 19, 20, 21, 26, 27, 28,
36, 37, 38, 42, 43, 44, 48, 49, 50, 54, 55, 56, 59 and 62