

# 74HC32-Q100; 74HCT32-Q100

Quad 2-input OR gate

Rev. 1 — 1 August 2012

Product data sheet

## 1. General description

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The 74HC32-Q100; 74HCT32-Q100 is a quad 2-input OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ °C}$  to  $+85\text{ °C}$  and from  $-40\text{ °C}$  to  $+125\text{ °C}$
- Wide supply voltage range from 2.0 V to 6.0 V
- Complies with JEDEC standard JESD7A
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Input levels:
  - ◆ For 74HC32-Q100: CMOS level
  - ◆ For 74HCT32-Q100: TTL level
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\ \Omega$ )
- Multiple package options



## 3. Ordering information

**Table 1. Ordering information**

Type number	Package			Version
	Temperature range	Name	Description	
74HC32D-Q100 74HCT32D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC32PW-Q100 74HCT32PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HC32BQ-Q100 74HCT32BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

## 4. Functional diagram

*mna242*

*mna243*

*mna241*

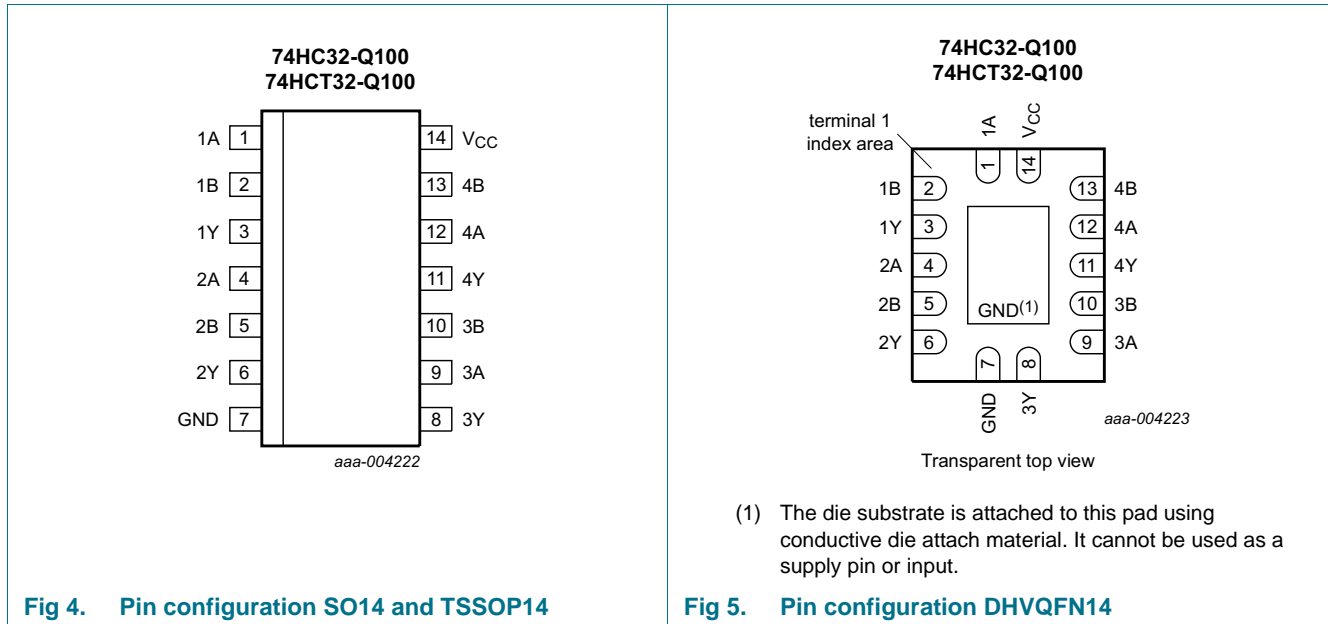
**Fig 1. Logic symbol**

**Fig 2. IEC logic symbol**

**Fig 3. Logic diagram (one gate)**

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation		[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

For TSSOP14 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC32			74HCT32			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC32-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
		I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	2.0	-	20	-
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT32-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 5.2 mA	-	0.15	0.25	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1	-	±1	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V	-	-	430	-	540	-	590	$\mu$ A
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**GND = 0 V;  $C_L = 50$  pF; for load circuit see [Figure 7](#).

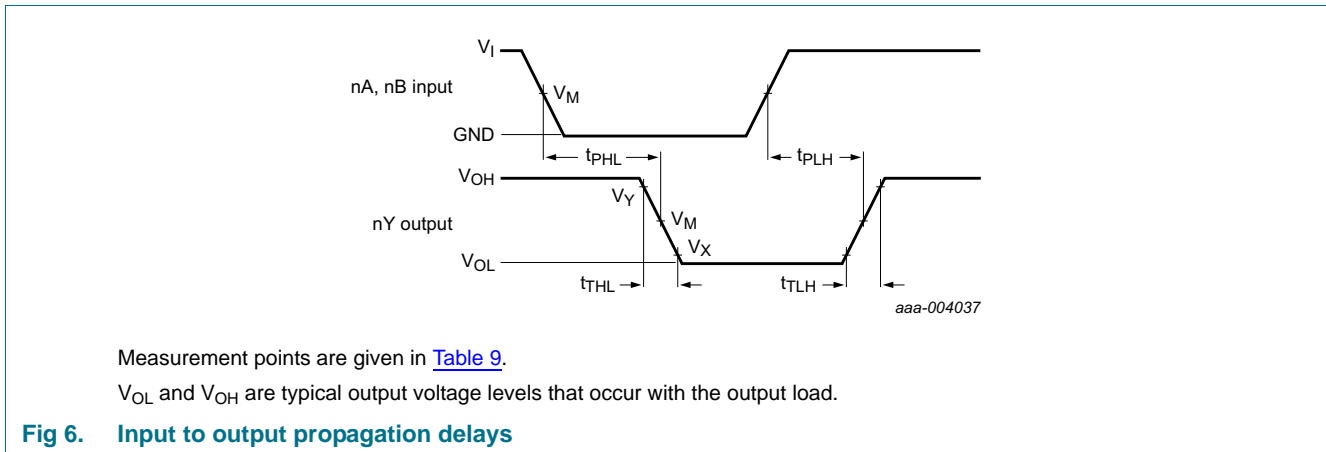
Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
<b>74HC32-Q100</b>									
$t_{pd}$	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a>		[1]					
		$V_{CC} = 2.0$ V	-	22	90	115	135	ns	
		$V_{CC} = 4.5$ V	-	8	18	23	27	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	6	-	-	-	ns	
		$V_{CC} = 6.0$ V	-	6	15	20	23	ns	
$t_t$	transition time	see <a href="#">Figure 6</a>		[2]					
		$V_{CC} = 2.0$ V	-	19	75	95	110	ns	
		$V_{CC} = 4.5$ V	-	7	15	19	22	ns	
		$V_{CC} = 6.0$ V	-	6	13	16	19	ns	
$C_{PD}$	power dissipation capacitance	per package; $V_I =$ GND to $V_{CC}$	[3]	-	16	-	-	-	pF

**Table 7. Dynamic characteristics**  
 GND = 0 V; C<sub>L</sub> = 50 pF; for load circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
<b>74HCT32-Q100</b>									
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a>	[1]						
		V <sub>CC</sub> = 4.5 V	-	11	24	30	36	ns	
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	9	-	-	-	ns	
t <sub>t</sub>	transition time	V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 6</a>	[2]	-	7	15	19	22	ns
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	[3]	-	28	-	-	-	pF

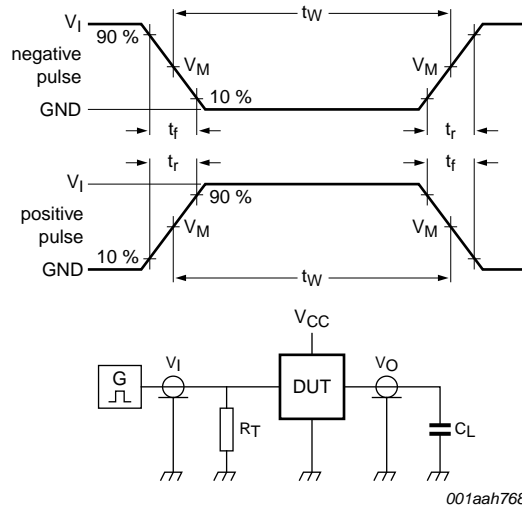
- [1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.
- [2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms



**Table 8. Measurement points**

Type	Input	Output		
	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
74HC32-Q100	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>
74HCT32-Q100	1.3 V	1.3 V	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 7. Load circuitry for measuring switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74HC32-Q100	$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT32-Q100	3.0 V	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$



## 12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

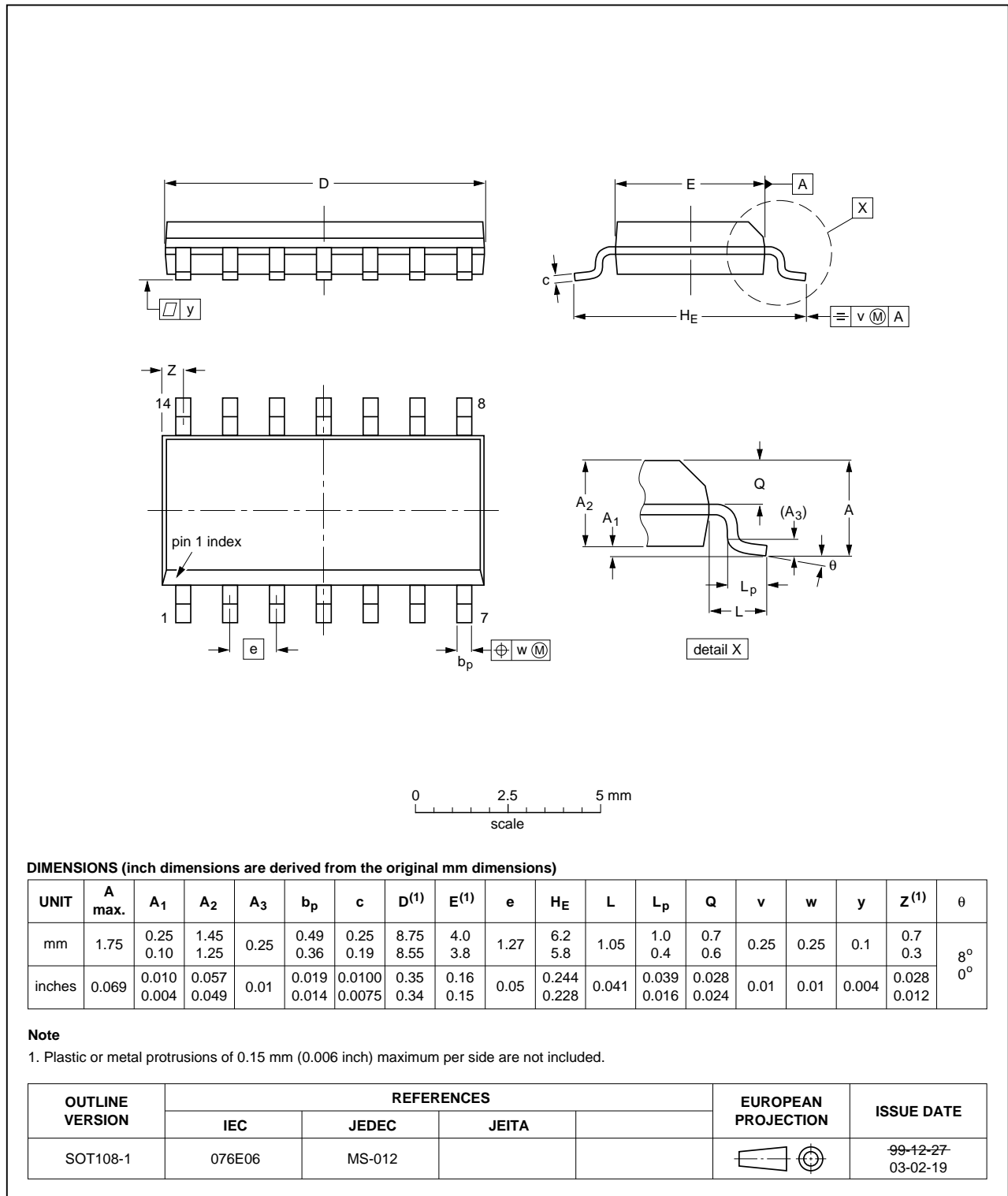


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

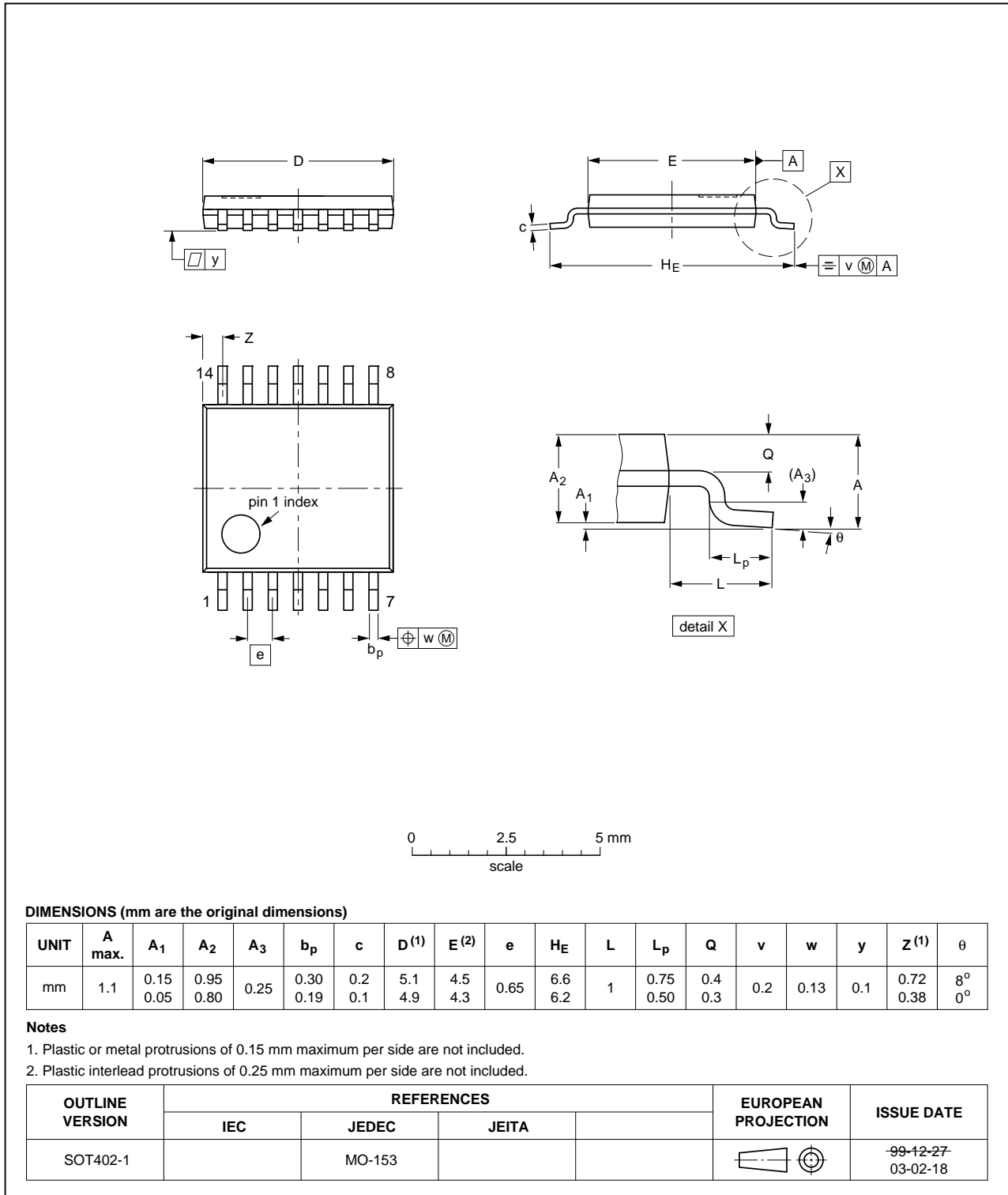


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

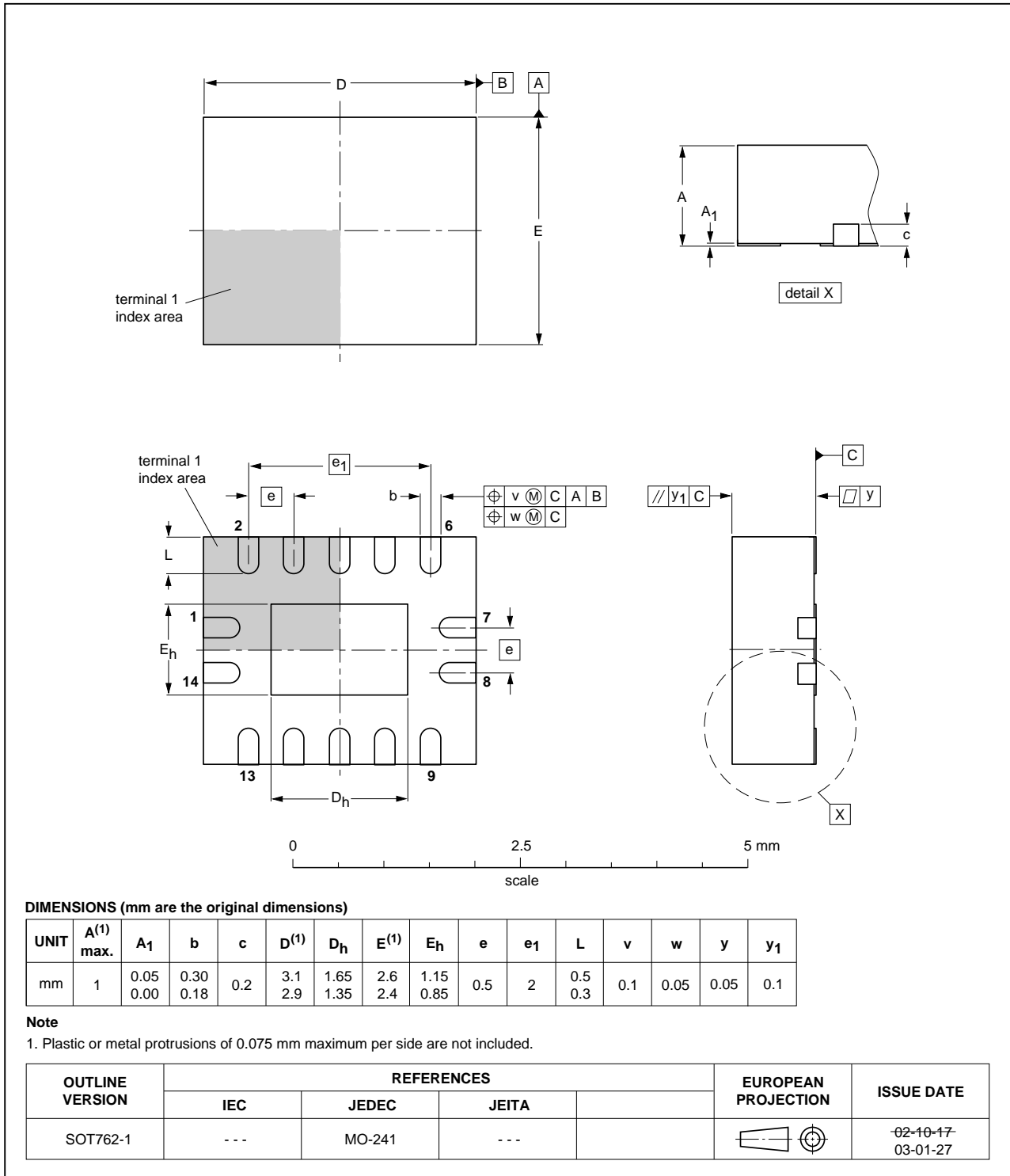


Fig 10. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic
MIL	Military

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT32_Q100 v.1	20120801	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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