ChipScope Integrated Bit Error Ratio Test (IBERT) for Spartan-6 GTP (v2.02a)

DS782 October 19, 2011 **Product Specification**

Introduction

The Xilinx ChipScope™ Pro IBERT core for Spartan®-6 GTP transceivers is customizable and can be used to evaluate and monitor Spartan-6 GTP transceivers. The design includes pattern generators and checkers implemented in FPGA logic, and access to the ports and the DRP attributes of the transceivers. Communication logic is also included to allow the design to be run-time, and is accessible through JTAG pins. The IBERT core is a self-contained design; when generated, it runs through the entire implementation flow, including bitstream generation.

Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core.
- Has a user-selectable number of Spartan-6 GTP transceivers.
- Each transceiver can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width.
- Requires a system clock that can be sourced from a pin or one of the enabled serial transceivers.

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Spartan-6				
Supported User Interfaces	N/A				
Resources(2)					**Frequency**
Configuration	**LUTs**	**FFs**	**I/O**	**Block RAMs**	**Max. Freq**
Config1	5921	9750	18	0	139.567 MHz
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Netlist				
Example Design	N/A				
Test Bench	N/A				
Constraints File	N/A				
Simulation Model	Not Provided				
Tested Design Tools					
Design Entry Tools	Xilinx CORE Generator™ tool				
Simulation	Not Provided				
Synthesis Tools	Not Provided				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. Including the variants of this FPGA device.
2. For single-serial transceiver design with 20-bit FPGA logic width.

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of Spartan-6 GTP transceivers.

Functional Description

The IBERT core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration platform for Spartan-6 GTP Transceivers. Parameterizable to use different serial transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and FPGA logic widths. Data pattern generators and checkers are included for each serial transceiver desired, giving a variety of different PRBS and clock patterns to be sent over the channels. In addition, the configuration and tuning of the serial transceivers is accessible though logic that communicates to the DRP port of the serial transceiver, in order to change attribute settings, as well as registers that control the values on the ports. At run time, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

Serial Transceiver Features

IBERT is designed for PMA evaluation and demonstration. All the major PMA features of the serial transceiver are supported and controllable in IBERT, including:

- Transmit (TX) pre-emphasis and post-emphasis
- TX differential swing
- Receive (RX) equalization
- Phase-Locked Loop (PLL) Divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

Generating the Core

Using the Xilinx CORE Generator™ software, you can define and generate a customized IBERT core for Spartan-6 FPGA GTP transceivers. When all the IBERT parameters have been chosen, a full design is generated, including a bitstream. The IBERT core cannot be included in your design; it can only be generated in its own stand-alone design. The ISE tools are invoked by the CORE Generator tool to generate a bitstream file (.bit) rather than a design netlist file (.ngc or .edn).

1. In the **Debug & Verification > ChipScope Pro IP** category of CORE Generator, select **IBERT Spartan6 GTP (ChipScope Pro - IBERT)** core.
2. Then click **Customize** in the right side of the window.

General IBERT Options

The first screen in the CORE Generator tool is used to set up general IBERT options, described in the following sections.

Choosing the Component Name

The Component Name can be any combination of alpha-numeric characters, including the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Selecting the Number of Line Rates (Protocols)

The IBERT core can have multiple MGTs, which do not have to operate at the same line rate, or use the same reference clock. Choose the number of distinct line rate/reference clock rate combinations needed from the Number of Line Rates (protocols) dialog.

Choosing the Line Rate Settings

For each line rate setting desired, choose between a custom setting ("Start from scratch") or a pre-defined protocol setting from the Protocol combo box. If a named protocol is chosen, the fields for Max Rate, Data Width, and REFCLK are automatically filled in according to the protocol. If specifying a custom protocol, type in the values desired.

Selecting the GTPA1_DUALs and Reference Clocks

After selecting the protocol options for the IBERT core, click **Next** to view the GTPA1_DUALs. Select GTXs and Reference Clocks for Line Rate 1. After Line Rate 1 is complete, click **Next** to access Line Rate 2, etc. until all the line rates are completed.

Choosing GTPA1_DUALs

Each available GTPA1_DUAL (also referred to as "DUAL" is listed with its location and a checkbox next to it. You cannot select a single transceiver within the DUAL: both transceivers must be used. If the checkbox is greyed out, the transceiver is already configured with a different line rate. Check the DUALs that will use the given line rate. Although both DUALs must be configured at the same line rate at generate time, that can be altered at runtime.

Choosing REFCLK Sources

From the GTP1 REFCLK Source combo box, choose the reference clock for each transceiver. One reference clock is available from the DUAL, and reference clocks are also available from neighboring DUALs. See the *Spartan-6 FPGA GTP Transceivers User Guide* for more information on the clocking topology.

Enabling RXRECCLK Probes

After selecting the GTP transceivers and REFCLK options for the IBERT core for all the line rates, click **Next** to view the RXRECCLK Probe options.

For each of the GTP transceivers used, it is possible to drive the RXRECCLK (recovered clock) out to a pin for use in external measurement. To enable this, check the Enable checkbox next to the desired recovered clock. Then specify the pin location in the Location text field, and choose the I/O Standard from the IO Standard combo box. For differential standards, specify the P pin location.

Choosing the System Clock Source

After selecting the RXRECCLK probing options, click Next to view the System Clock options.

IBERT needs a clock for the internal communication logic. This can come from an external pin, or from the TXOUTCLK of one of the GTP transceivers enabled in the IBERT design. To use a clock from a pin, enable the Use External Clock source radio button, type the frequency in the Frequency field, type the pin location in the Pin Location field, and choose the Pin Input Standard. For differential standards, specify the P pin location.

To specify an internal clock, disable the Use External Clock source radio button in the first panel. In the System Clock Source panel, specify the GTP transceiver in the GTP Dual Source combo box.

Generating the Design

After entering the IBERT core parameters, click **Next** to view the IBERT Design Summary. This includes the GTP transceivers used, system clock, and the details of the global clock resources. To generate the design, click **Generate**.

Pattern Generation and Checking

Each serial transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(11111111110000000000...) patterns. These patterns are optimized for the FPGA logic width chosen, and are selectable at run time. The TX pattern and RX pattern are individually selectable.

The pattern checker logic also generates a 'link' signal that displays in the Analyzer software. The channel is linked when there are five consecutive cycles of data with no errors. The incoming data is compared against a pattern that is generated internally. When the checker receives five consecutive cycles of data with errors, it removes the channel link. Internal counters accumulate the number of words and error received.

DRP and Ports Access

IBERT also provides flexibility to change serial transceiver ports and attributes. DRP interface logic is included that allows the run-time software to monitor and change any attribute in any of the serial transceivers included in the IBERT core. Readable and writable (when applicable) registers are also included that are connected to the various ports of the serial transceiver. All are accessible at run time using the ChipScope Analyzer tool.

System Clock

The IBERT Core requires a free-running system clock to clock the communication and other logic included in the IBERT core. This clock can be chosen at generation time to come from an FPGA pin, or be driven from the TXOUTCLK port of one of the serial transceivers in the core. If the system clock is running faster than 150 MHz, it is divided down internally using an DCM to satisfy timing constraints.

Interface Ports

The Input/Output (I/O) signals of the IBERT core consist only of the serial transceiver reference clocks, the serial transceiver transmit and receive pins, and a system clock (optional).

Table 1: **Interface Ports**

Port Name	Direction	Description
SYSCLK	IN	Design clock that clocks all communication logic. This port is optional, because you can select an internal serial transceiver clock at generation time to perform this function.
TXN[n-1:0], TXP[n-1:0]	OUT	Transmit differential pairs for each of the n serial transceivers used.

Table 1: **Interface Ports *(Cont'd)***

Port Name	Direction	Description
RXN[n-1:0], RXP[n-1:0]	OUT	Receive differential pairs for each of the n serial transceivers used.
MGTREFCLK_P[m-1:0], MGTREFCLK_N[m-1:0]	IN	Serial transceiver reference clocks used. Not necessarily m = n because some serial transceivers can share clock inputs.

Restrictions

Only one IBERT core can be generated for a device, and the IBERT core will constitute the entire design. The IBERT core cannot be merged in with user logic.

Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

References

- More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at http://www.xilinx.com/documentation.
- Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio 11 online help, located at http://www.xilinx.com/documentation.
- Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the *Xilinx System Generator for DSP User Guide*, located at http://www.xilinx.com/documentation.

Support

Xilinx provides technical support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The IBERT core is provided under the Integrated Software Environment (ISE®) Design Suite End-User License Agreement and can be generated using the Xilinx CORE Generator system 11 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

List of Acronyms

Table 2: **List of Acronyms**

Acronym	Definition
DRP	Dynamic Reconfiguration Port
FF	Flip-Flop
FPGA	Field Programmable Gate Array
I/O	Input/Output
IBERT	Integrated Bit Error Radio Tester
IP	Intellectual Property
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
LUT	Lookup Table
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
PMA	Physical Medium Attachment
PRBS	Pseudorandom binary sequence
RAM	Random Access Memory
RX	Receive
TX	Transmit
XST	Xilinx Synthesis Technology

Revision History

The following table sumarizes the change history for this document:

Date	Version	Description of Revisions
09/16/2009	1.0	Release 11.3 (Initial Xilinx release).
10/19/2011	2.0	• Updated to 2.02.a core version and 13.3 Xilinx tools. • Added new section for generating the IBERT core. • Added List of Acronyms. • Updated Notice of Disclaimer and Copyright notice. • Replaced “MGT” with “serial transceiver”

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