

Features

- Optimized for 1.8V systems
 - As fast as 4.0 ns pin-to-pin logic delays
 - As low as 15 μ A quiescent current
 - 64 macrocells with up to 1,600 logic gates
 - Fast input registers
 - Slew rate control on individual outputs
 - LVCMOS 1.8V through 3.3V
 - 1.5V I/O compatible
 - LVTTL 3.3V
- Available in multiple package options
 - 44-pin PLCC with 33 user I/O
 - 44-pin VQFP with 33 user I/O
 - 56-ball CP BGA with 45 user I/O
 - 100-pin VQFP with 64 user I/O
- Advanced system features
 - Fastest in system programming
 - 1.8V ISP using IEEE 1532 (JTAG) interface
 - IEEE1149.1 JTAG Boundary Scan Test
 - Optional Schmitt-trigger input (per pin)
 - Fast Zero Power[™] (FZP) 100% CMOS product term generation
 - Flexible clocking modes
 - Optional DualEDGE triggered registers
 - Global signal options with macrocell control
 - Multiple global clocks with phase selection per macrocell
 - Multiple global output enables
 - Global set/reset
 - Efficient control term clocks, output enables and set/resets for each macrocell and shared across function blocks
 - Advanced design security
 - Open-drain output option for Wired-OR and LED drive
 - Optional configurable grounds on unused I/Os
 - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
 - PLA architecture
 - Superior pinout retention
 - 100% product term routability across function block
 - Hot pluggable

Refer to the CoolRunner[™]-II family data sheet for architecture description.

Description

The CoolRunner-II 64-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved.

This device consists of four Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term types, configured on a per macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain and programmable grounds. A Schmitt trigger input is available on a per input pin basis. In addition to storing macrocell output states, the macrocell registers may be configured as "fast input" registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchronous set/reset and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

The CoolRunner-II 64-macrocell CPLD is I/O compatible with standard LVTTL and LVCMOS18, LVCMOS25, and LVCMOS33 (see [Table 1](#)). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Fast Zero Power Design Technology

Xilinx CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ Fast Zero Power™ (FZP), a design technique that makes use of CMOS technology in both the fabrication and design methodology. FZP design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high performance and low power operation.

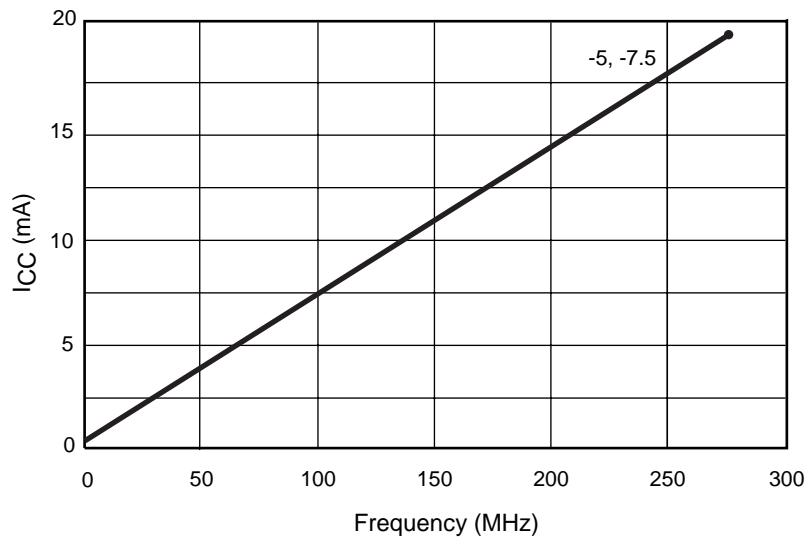
Supported I/O Standards

The CoolRunner-II 64 macrocell features both LVCMOS and LVTTTL I/O implementations. See [Table 1](#) for I/O standard voltages. The LVTTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an

LVTTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: I/O Standards for XC2C64

| I/O Types | Output V _{CCIO} | Input V _{CCIO} | Input V _{REF} | Board Termination Voltage V _T |
|-----------|--------------------------|-------------------------|------------------------|--|
| LVTTTL | 3.3 | 3.3 | N/A | N/A |
| LVCMOS33 | 3.3 | 3.3 | N/A | N/A |
| LVCMOS25 | 2.5 | 2.5 | N/A | N/A |
| LVCMOS18 | 1.8 | 1.8 | N/A | N/A |
| 1.5V I/O | 1.5 | 1.5 | N/A | N/A |



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Figure 1: I_{CC} vs Frequency

Table 2: I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)⁽¹⁾

| | Frequency (MHz) | | | | | | | | | | |
|---------------------------------------|-----------------|------|------|------|------|-------|-------|-------|-------|-------|------|
| | 0 | 25 | 50 | 75 | 100 | 150 | 175 | 200 | 225 | 250 | 270 |
| Typical -5, -7.5 I _{CC} (mA) | 0.015 | 1.85 | 3.69 | 5.55 | 7.35 | 10.87 | 12.54 | 14.22 | 15.91 | 17.56 | 18.9 |
| Typical -4 I _{CC} (mA) | | | | | | | | | | | |

Notes:

- 16-bit up/down, resettable binary counter (one counter per function block).

Absolute Maximum Ratings

| Symbol | Description | Value | Units |
|------------|---|-------------|-------|
| V_{CC} | Supply voltage relative to ground | -0.5 to 2.0 | V |
| V_{CCIO} | Supply voltage for output drivers | -0.5 to 4.0 | V |
| V_{JTAG} | JTAG input voltage limits | -0.5 to 4.0 | V |
| V_{AUX} | JTAG input supply voltage | -0.5 to 4.0 | V |
| V_{IN} | Input voltage relative to ground ⁽¹⁾ | -0.5 to 4.0 | V |
| V_{TS} | Voltage applied to 3-state output ⁽¹⁾ | -0.5 to 4.0 | V |
| T_{STG} | Storage Temperature (ambient) | -65 to +150 | °C |
| T_{SOL} | Maximum Soldering temperature (10s @ 1/16in. = 1.5mm) | +260 | °C |
| T_J | Junction Temperature | +150 | °C |

Notes:

- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to -2.0V or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units | |
|------------|---|---|-----|-------|---|
| V_{CC} | Supply voltage for internal logic and input buffers | Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | 1.7 | 1.9 | V |
| | | Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 1.7 | 1.9 | V |
| V_{CCIO} | Supply voltage for output drivers @ 3.3V operation | 3.0 | 3.6 | V | |
| | Supply voltage for output drivers @ 2.5V operation | 2.3 | 2.7 | V | |
| | Supply voltage for output drivers @ 1.8V operation | 1.7 | 1.9 | V | |
| | Supply voltage for output drivers @ 1.5V operation | 1.4 | 1.6 | V | |
| V_{AUX} | JTAG programming pins | 1.7 | 3.6 | V | |

DC Electrical Characteristics (Over Recommended Operating Conditions)

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|--------------------------------|---|------|------|---------------|
| I_{CCSB} | Standby current (-5, -7) | $V_{CC} = 1.9\text{V}$, $V_{CCIO} = 3.6\text{V}$ | | 100 | μA |
| I_{CCSB} | Standby current (-4) | $V_{CC} = 1.9\text{V}$, $V_{CCIO} = 3.6\text{V}$ | | | mA |
| I_{CC} | Dynamic current (-5, -7) | $f = 1\text{ MHz}$ | | | mA |
| | | $f = 50\text{ MHz}$ | | | mA |
| I_{CC} | Dynamic current (-4) | $f = 1\text{ MHz}$ | | | mA |
| | | $f = 50\text{ MHz}$ | | | mA |
| C_{JTAG} | JTAG input capacitance | $f = 1\text{ MHz}$ | | | pF |
| C_{CLK} | Global clock input capacitance | $f = 1\text{ MHz}$ | | | pF |
| C_{IO} | I/O capacitance | $f = 1\text{ MHz}$ | | | pF |

LVC MOS 3.3V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|--------------------------------|---|-------------------|-------------------|---------------|
| V_{CCIO} | Input source voltage | | 3.0 | 3.6 | V |
| V_{IH} | High level input voltage | | 2 | $V_{CCIO} + 0.3V$ | V |
| V_{IL} | Low level input voltage | | -0.3 | 0.8 | V |
| V_{OH} | High level output voltage | $I_{OH} = -8 \text{ mA}, V_{CCIO} = 3V$ | $V_{CCIO} - 0.4V$ | - | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 3V$ | $V_{CCIO} - 0.2V$ | - | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 3V$ | - | 0.4 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 3V$ | - | 0.2 | V |
| I_{IL} | Input leakage current | $V_{IN} = 0V$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| I_{IH} | I/O High-Z leakage | $V_{IN} = 0V$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| C_{JTAG} | JTAG input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{CLK} | Global clock input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{IO} | I/O capacitance | $f = 1 \text{ MHz}$ | | | pF |

LVC MOS 2.5V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|--------------------------------|---|-------------------|------|---------------|
| V_{CCIO} | Input source voltage | | 2.3 | 2.7 | V |
| V_{IH} | High level input voltage | | 1.7 | 3.9 | V |
| V_{IL} | Low level input voltage | | -0.3 | 0.7 | V |
| V_{OH} | High level output voltage | $I_{OH} = -8 \text{ mA}, V_{CCIO} = 2.3V$ | $V_{CCIO} - 0.4V$ | - | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 2.3V$ | $V_{CCIO} - 0.2V$ | - | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 2.3V$ | - | 0.4 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 2.3V$ | - | 0.2 | V |
| I_{IL} | Input leakage current | $V_{IN} = 0V$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| I_{IH} | I/O High-Z leakage | $V_{IN} = 0V$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| C_{JTAG} | JTAG input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{CLK} | Global clock input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{IO} | I/O capacitance | $f = 1 \text{ MHz}$ | | | pF |

LVC MOS 1.8V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|--------------------------------|--|-----------------------|-----------------------|---------------|
| V_{CCIO} | Input source voltage | | 1.7 | 1.9 | V |
| V_{IH} | High level input voltage | | $0.7 \times V_{CCIO}$ | 3.9 | V |
| V_{IL} | Low level input voltage | | -0.3 | $0.2 \times V_{CCIO}$ | V |
| V_{OH} | High level output voltage | $I_{OH} = -8 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | $V_{CCIO} - 0.45$ | - | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | $V_{CCIO} - 0.2$ | - | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | - | 0.45 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | - | 0.2 | V |
| I_{IL} | Input leakage current | $V_{IN} = 0$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| I_{IH} | I/O High-Z leakage | $V_{IN} = 0$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| C_{JTAG} | JTAG input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{CLK} | Global clock input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{IO} | I/O capacitance | $f = 1 \text{ MHz}$ | | | pF |

1.5V DC Voltage Specifications⁽¹⁾

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|--------------------------------|--|-----------------------|------|---------------|
| V_{CCIO} | Input source voltage | | 1.4 | 1.6 | V |
| V_{IH} | High level input voltage | | $0.7 \times V_{CCIO}$ | 3.9 | V |
| V_{IL} | Low level input voltage | | -0.3 | 0.3 | V |
| V_{OH} | High level output voltage | $I_{OH} = -4 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | $V_{CCIO} - 0.45$ | | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | $V_{CCIO} - 0.2$ | | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | | 0.4 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | | 0.2 | V |
| I_{IL} | Input leakage current | $V_{IN} = 0$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| I_{IH} | I/O High-Z leakage | $V_{IN} = 0$ or V_{CCIO} to 3.9V | -10 | 10 | μA |
| C_{JTAG} | JTAG input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{CLK} | Global clock input capacitance | $f = 1 \text{ MHz}$ | | | pF |
| C_{IO} | I/O capacitance | $f = 1 \text{ MHz}$ | | | pF |

Notes:

1. Hysteresis used on 1.5V inputs.

AC Electrical Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | -4 | | -5 | | -7 | | Units |
|-------------------------------------|--|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| T _{PD1} | Propagation delay single p-term | - | 3.7 | - | 4.6 | - | 6.7 | ns |
| T _{PD2} | Propagation delay OR array | - | 4.0 | - | 5.0 | - | 7.5 | ns |
| T _{SUF} | Fast input register p-term clock setup time | 1.6 | - | 1.9 | - | 2.3 | - | ns |
| T _{SU1} | Setup time fast (single p-term) | 1.7 | - | 2.0 | - | 2.5 | - | ns |
| T _{SU2} | Setup time (OR array) | 2.0 | - | 2.4 | - | 3.3 | - | ns |
| T _{HF} | Fast input register hold time | 0 | - | 0 | - | 0 | - | ns |
| T _H | P-term hold time | 0 | - | 0 | - | 0 | - | ns |
| T _{CO} | Clock to output | - | 3.0 | - | 3.9 | - | 6.0 | ns |
| F _{TOGGLE} ⁽¹⁾ | Internal toggle rate | - | 416 | - | 250 | - | 168 | MHz |
| F _{SYSTEM1} ⁽²⁾ | Maximum system frequency | - | 294 | - | 233 | - | 159 | MHz |
| F _{SYSTEM2} ⁽²⁾ | Maximum system frequency | - | 270 | - | 213 | - | 141 | MHz |
| F _{EXT1} ⁽³⁾ | Maximum external frequency | - | 213 | - | 169 | - | 118 | MHz |
| F _{EXT2} ⁽³⁾ | Maximum external frequency | - | 200 | - | 159 | - | 108 | MHz |
| T _{PSUF} | Fast input register p-term clock setup time | 1.0 | - | 1.2 | - | 1.5 | - | ns |
| T _{PSU1} | P-term clock setup time (single p-term) | 1.0 | - | 1.2 | - | 1.5 | - | ns |
| T _{PSU2} | P-term clock setup time (OR array) | 1.4 | - | 1.7 | - | 2.5 | - | ns |
| T _{PHF} | Fast input register p-term clock hold time | 0.4 | - | 0.6 | - | 0.7 | - | ns |
| T _{PH} | P-term clock hold | 0.3 | - | 0.5 | - | 0.5 | - | ns |
| T _{PCO} | P-term clock to output | - | 3.6 | - | 4.6 | - | 6.8 | ns |
| T _{OE} /T _{OD} | Global OE to output enable/disable | - | 3.9 | - | 4.9 | - | 7.0 | ns |
| T _{POE} /T _{POD} | P-term OE to output enable/disable | - | 4.3 | - | 5.3 | - | 7.3 | ns |
| T _{MOE} /T _{MOD} | Macrocell driven OE to output enable/disable | - | 4.9 | - | 6.3 | - | 9.2 | ns |
| T _{PAO} | P-term set/reset to output valid | - | 5.4 | - | 6.4 | - | 9.1 | ns |
| T _{AO} | Global set/reset to output valid | - | 5.5 | - | 6.5 | - | 9.3 | ns |
| T _{SUEC} | Register clock enable setup time | 1.8 | - | 2.1 | - | 2.6 | - | ns |
| T _{HEC} | Register clock enable hold time | 0 | - | 0 | - | 0 | - | ns |
| T _{CW} | Global clock pulse width High or Low | 1.2 | - | 2.0 | - | 3.0 | - | ns |
| T _{PCW} | P-term pulse width High or Low | 4.0 | - | 5.0 | - | 7.5 | - | ns |
| T _{CONFIG} | Configuration time | | | | | | | μs |

Notes:

1. F_{TOGGLE} (1/2*T_{CW}) is the maximum frequency of a dual edge triggered T flip-flop with output enabled.
2. F_{SYSTEM1} (1/T_{CYCLE}) is the internal operating frequency for a device fully populated with 16-bit resettable binary counter through one p-term per macrocell while F_{SYSTEM2} is through the OR array (one counter per function block).
3. F_{EXT1} (1/T_{SU2}+T_{CO}) is the maximum external frequency using one p-term while F_{EXT2} is through the OR array.

Internal Timing Parameters

| Symbol | Parameter ⁽¹⁾ | -4 | | -5 | | -7 | | Units |
|---|------------------------------------|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Buffer Delays | | | | | | | | |
| T _{IN} | Input buffer delay | - | 1.3 | - | 1.7 | - | 2.4 | ns |
| T _{FIN} | Fast data register input delay | - | 1.6 | - | 2.1 | - | 3.0 | ns |
| T _{GCK} | Global Clock buffer delay | - | 1.2 | - | 1.6 | - | 2.5 | ns |
| T _{GSR} | Global set/reset buffer delay | - | 1.9 | - | 2.4 | - | 3.5 | ns |
| T _{GTS} | Global 3-state buffer delay | - | 1.4 | - | 1.9 | - | 3.0 | ns |
| T _{OUT} | Output buffer delay | - | 1.6 | - | 1.9 | - | 2.8 | ns |
| T _{EN} | Output buffer enable/disable delay | - | 2.5 | - | 3.0 | - | 4.0 | ns |
| P-term Delays | | | | | | | | |
| T _{CT} | Control term delay | - | 0.5 | - | 0.6 | - | 0.9 | ns |
| T _{LOGI1} | Single P-term delay adder | - | 0.4 | - | 0.5 | - | 0.8 | ns |
| T _{LOGI2} | Multiple P-term delay adder | - | 0.3 | - | 0.4 | - | 0.8 | ns |
| Macrocell Delay | | | | | | | | |
| T _{PDI} | Input to output valid | - | 0.4 | - | 0.5 | - | 0.7 | ns |
| T _{SUI} | Setup before clock | 1.2 | - | 1.4 | - | 1.8 | - | ns |
| T _{HI} | Hold after clock | 0 | - | 0 | - | 0 | - | ns |
| T _{ECSU} | Enable clock setup time | 1.2 | - | 1.4 | - | 1.8 | - | ns |
| T _{ECHO} | Enable clock hold time | 0 | - | 0 | - | 0 | - | ns |
| T _{COI} | Clock to output valid | - | 0.2 | - | 0.4 | - | 0.7 | ns |
| T _{AOI} | Set/reset to output valid | - | 2.0 | - | 2.2 | - | 3.0 | ns |
| T _{CDBL} | Clock doubler delay | - | 0 | - | 0 | - | 0 | ns |
| Feedback Delays | | | | | | | | |
| T _F | Feedback delay | - | 1.6 | - | 2.0 | - | 3.0 | ns |
| T _{OEM} | Macrocell to global OE delay | - | 1.0 | - | 1.3 | - | 2.0 | ns |
| I/O Standard Time Adder Delays 1.5V I/O | | | | | | | | |
| T _{IN15} | Standard input adder | - | 0.5 | - | 0.8 | - | 1.0 | ns |
| T _{HYS15} | Hysteresis input adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| T _{OUT15} | Output adder | - | 0.5 | - | 0.8 | - | 1.0 | ns |
| T _{SLEW15} | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| I/O Standard Time Adder Delays 1.8V CMOS | | | | | | | | |
| T _{IN18} | Standard input adder | - | 0 | - | 0 | - | 0 | ns |
| T _{HYS18} | Hysteresis input adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| T _{OUT18} | Output adder | - | 0 | - | 0 | - | 0 | ns |
| T _{SLEW} | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |

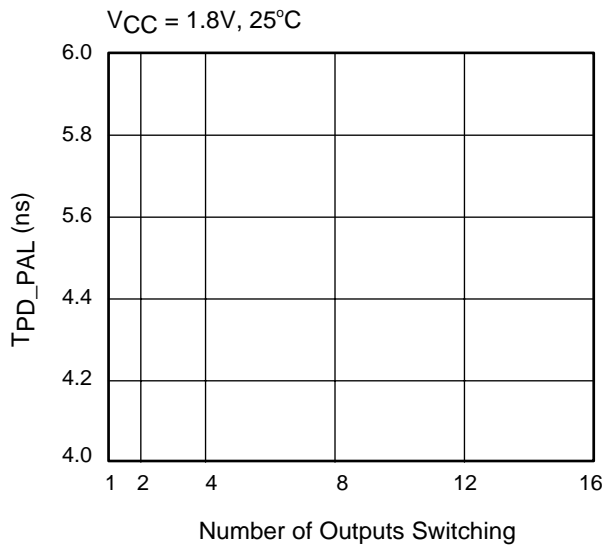
Internal Timing Parameters (Continued)

| Symbol | Parameter ⁽¹⁾ | -4 | | -5 | | -7 | | Units |
|---|--------------------------|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I/O Standard Time Adder Delays 2.5V CMOS | | | | | | | | |
| T _{IN25} | Standard input adder | - | 0.5 | - | 0.8 | - | 1.0 | ns |
| T _{HYS25} | Hysteresis input adder | - | 1.5 | - | 2.5 | - | 3.0 | ns |
| T _{OUT25} | Output adder | - | 1.5 | - | 2.5 | - | 3.0 | ns |
| T _{SLEW25} | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |
| I/O Standard Time Adder Delays 3.3V CMOS/TTL | | | | | | | | |
| T _{IN33} | Standard input adder | - | 0.7 | - | 1.0 | - | 2.0 | ns |
| T _{HYS33} | Hysteresis input adder | - | 1.0 | - | 2.0 | - | 3.0 | ns |
| T _{OUT33} | Output adder | - | 1.0 | - | 2.0 | - | 3.0 | ns |
| T _{SLEW33} | Output slew rate adder | - | 2.0 | - | 3.0 | - | 4.0 | ns |

Notes:

1. 1.5 ns input pin signal rise/fall.

Switching Characteristics



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Pin Descriptions

| Function Block | Macro-cell | PC44 | VQ44 | CP56 | VQ100 |
|----------------|------------|------|------|------|-------|
| 1 | 1 | 44 | 38 | F1 | 13 |
| 1 | 2 | 43 | 37 | E3 | 12 |
| 1 | 3 | 42 | 36 | E1 | 11 |
| 1 | 4 | - | - | - | 10 |
| 1 | 5 | - | - | - | 9 |
| 1 | 6 | - | - | - | 8 |
| 1 | 7 | - | - | - | 7 |
| 1 | 8 | - | - | - | 6 |
| 1(GTS1) | 9 | 40 | 34 | D1 | 4 |
| 1(GTS0) | 10 | 39 | 33 | C1 | 3 |
| 1(GTS3) | 11 | 38 | 32 | A3 | 2 |
| 1(GTS2) | 12 | 37 | 31 | A2 | 1 |
| 1(GSR) | 13 | 36 | 30 | B1 | 99 |
| 1 | 14 | - | - | A1 | 97 |
| 1 | 15 | - | - | C3 | 94 |
| 1 | 16 | - | - | - | 92 |
| 2 | 1 | 1 | 39 | G1 | 14 |
| 2 | 2 | 2 | 40 | F3 | 15 |
| 2 | 3 | - | - | - | 16 |
| 2 | 4 | - | - | - | 17 |
| 2 | 5 | 3 | 41 | H1 | 18 |
| 2 | 6 | 4 | 42 | G3 | 19 |
| 2(GCK0) | 7 | 5 | 43 | J1 | 22 |
| 2(GCK1) | 8 | 6 | 44 | K1 | 23 |
| 2 | 9 | - | - | K4 | 24 |
| 2(GCK2) | 10 | 7 | 1 | K2 | 27 |
| 2 | 11 | - | - | - | 28 |
| 2 | 12 | 8 | 2 | K3 | 29 |
| 2 | 13 | 9 | 3 | H3 | 30 |
| 2 | 14 | - | - | K5 | 32 |
| 2 | 15 | - | - | - | 33 |
| 2 | 16 | - | - | - | 34 |

Pin Descriptions (Continued)

| Function Block | Macro-cell | PC44 | VQ44 | CP56 | VQ100 |
|----------------|------------|------|------|------|-------|
| 3 | 1 | 35 | 29 | C4 | 91 |
| 3 | 2 | 34 | 28 | A4 | 90 |
| 3 | 3 | 33 | 27 | C5 | 89 |
| 3 | 4 | - | - | A7 | 81 |
| 3 | 5 | - | - | C8 | 79 |
| 3 | 6 | 29 | 23 | A8 | 78 |
| 3 | 7 | - | - | A9 | 77 |
| 3 | 8 | - | - | - | 76 |
| 3 | 9 | - | - | A5 | 74 |
| 3 | 10 | 28 | 22 | A10 | 72 |
| 3 | 11 | 27 | 21 | B10 | 71 |
| 3 | 12 | 26 | 20 | C10 | 70 |
| 3 | 13 | - | - | D8 | 68 |
| 3 | 14 | 25 | 19 | E8 | 67 |
| 3 | 15 | 24 | 18 | D10 | 64 |
| 3 | 16 | - | - | - | 61 |
| 4 | 1 | 11 | 5 | K6 | 35 |
| 4 | 2 | 12 | 6 | H5 | 36 |
| 4 | 3 | - | - | K7 | 37 |
| 4 | 4 | - | - | - | 39 |
| 4 | 5 | - | - | H7 | 40 |
| 4 | 6 | - | - | - | 41 |
| 4 | 7 | 14 | 8 | H8 | 42 |
| 4 | 8 | - | - | - | 43 |
| 4 | 9 | - | - | - | 49 |
| 4 | 10 | - | - | K8 | 50 |
| 4 | 11 | 18 | 12 | H10 | 52 |
| 4 | 12 | - | - | - | 53 |
| 4 | 13 | 19 | 13 | G10 | 55 |
| 4 | 14 | 20 | 14 | - | 56 |
| 4 | 15 | 22 | 16 | F10 | 58 |
| 4 | 16 | - | - | E10 | 60 |

Notes:

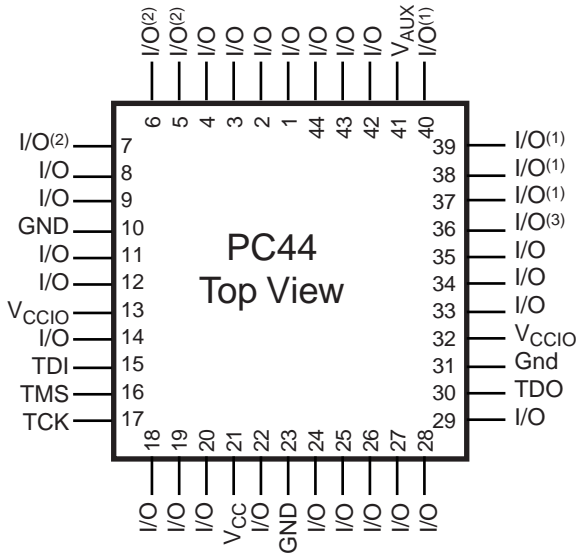
1. GTS = global output enable, GSR = global set reset, GCK = global clock x

XC2C64 Global, JTAG, Power/Ground and No Connect Pins

| Pin Type | PC44 | VQ44 | CP56 | VQ100 |
|---|----------|---------|------------|--|
| TCK | 17 | 11 | K10 | 48 |
| TDI | 15 | 9 | J10 | 45 |
| TDO | 30 | 24 | A6 | 83 |
| TMS | 16 | 10 | K9 | 47 |
| V _{AUX} (JTAG supply voltage) | 41 | 35 | D3 | 5 |
| Power internal (V _{CC}) | 21 | 15 | G8 | 26,57 |
| Power external I/O (V _{CCIO}) | 13, 32 | 7,26 | H6, C6 | 38, 51,88, 98 |
| Ground | 10,23,31 | 4,17,25 | H4, F8, C7 | 21,31,62,69,84,100 |
| No connects | | | | 20,25,44,46,54,59,63,65,66,73,75, 80,82,85,86,87,93,95,96 |
| Total user I/O | 33 | 33 | 45 | 64 |

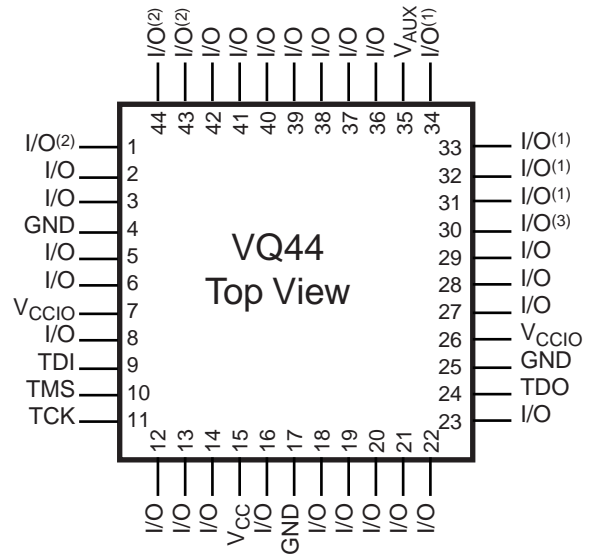
Ordering Information

| Device Ordering No. and Part Marking No. | Pin/Ball Spacing | θ_{JA} (C/Watt) | θ_{JC} (C/Watt) | Package Type | Package Dimensions | I/O | Comm. (C) Ind. (I) |
|--|------------------|------------------------|------------------------|-----------------------------|--------------------|-----|--------------------|
| XC2C64-4PC44C | 1.27mm | 53.1 | 28.7 | Plastic Leaded Chip Carrier | 17.5mm x 17.5mm | 33 | C |
| XC2C64-5PC44C | 1.27mm | 53.1 | 28.7 | Plastic Leaded Chip Carrier | 17.5mm x 17.5mm | 33 | C |
| XC2C64-7PC44C | 1.27mm | 53.1 | 28.7 | Plastic Leaded Chip Carrier | 17.5mm x 17.5mm | 33 | C |
| XC2C64-4VQ44C | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack | 12mm x 12mm | 33 | C |
| XC2C64-5VQ44C | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack | 12mm x 12mm | 33 | C |
| XC2C64-7VQ44C | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack | 12mm x 12mm | 33 | C |
| XC2C64-4CP56C | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 6mm x 6mm | 45 | C |
| XC2C64-5CP56C | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 6mm x 6mm | 45 | C |
| XC2C64-7CP56C | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 6mm x 6mm | 45 | C |
| XC2C64-4VQ100C | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack | 14mm x 14mm | 64 | C |
| XC2C64-5VQ100C | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack | 14mm x 14mm | 64 | C |
| XC2C64-7VQ100C | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack | 14mm x 14mm | 64 | C |
| XC2C64-7PC44I | 1.27mm | 53.1 | 28.7 | Plastic Leaded Chip Carrier | 17.5mm x 17.5mm | 33 | I |
| XC2C64-7VQ44I | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack | 12mm x 12mm | 33 | I |
| XC2C64-7CP56I | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 6mm x 6mm | 45 | I |
| XC2C64-7VQ100I | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack | 14mm x 14mm | 64 | I |



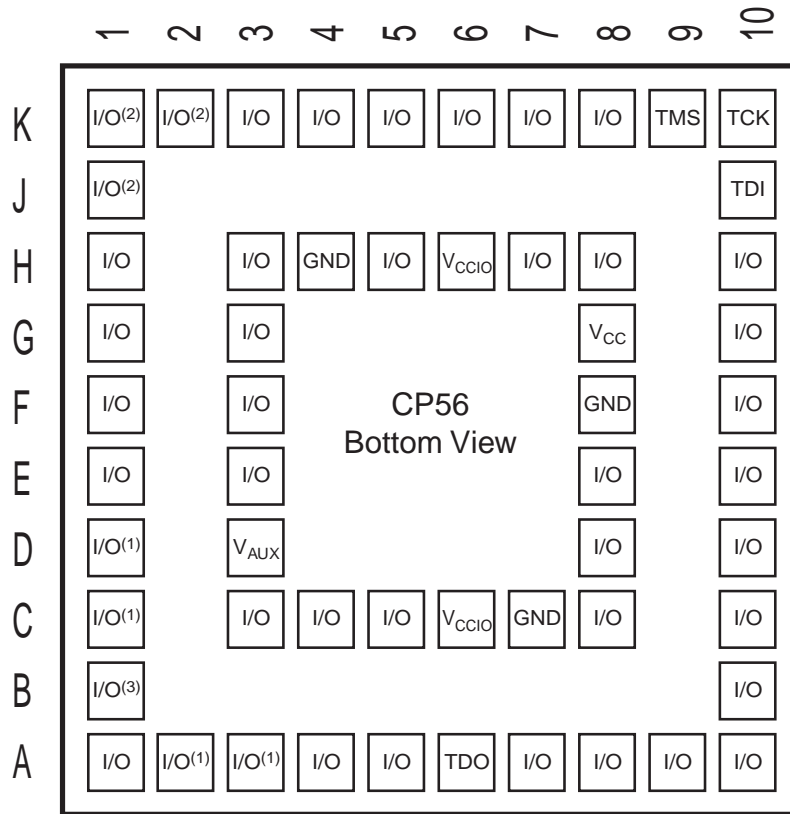
- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 2: PC44 Package



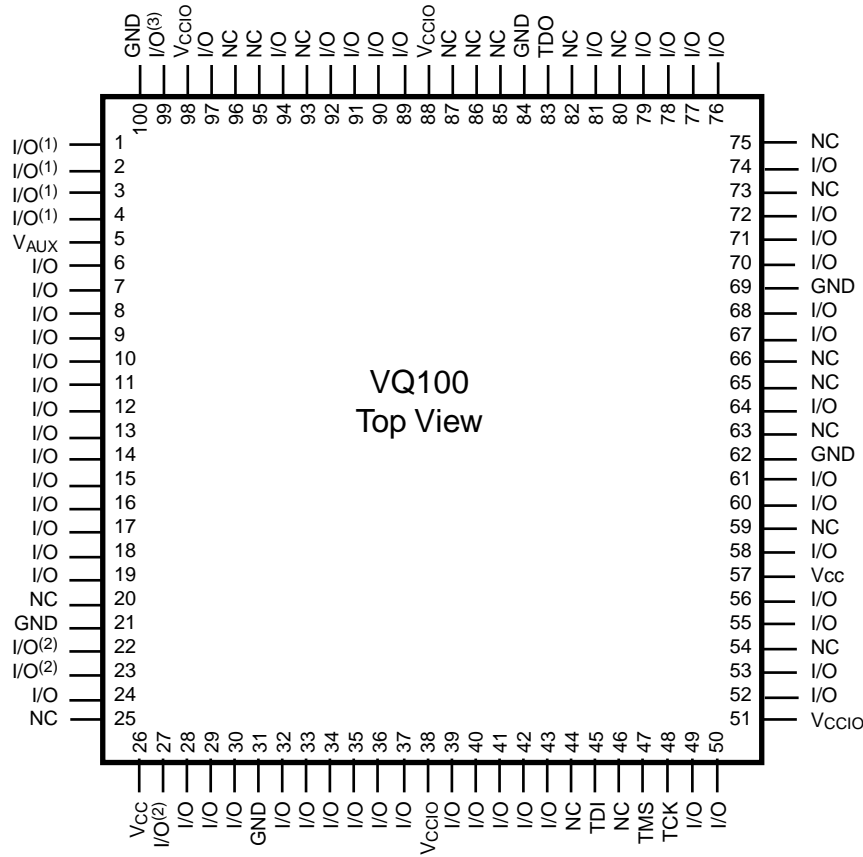
- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 3: VQ44 Package



- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 4: CP56 Package



- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset

Figure 5: VQ100 Package

Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|----------|---------|--|
| 01/03/02 | 1.0 | Initial Xilinx release. |
| 03/04/02 | 1.1 | Removed A4 from the FB1, MC16, and CP56 in the Pinout tables. Updated V _{OH} and V _{OL} for LVCMOS 2.5V, LVCMOS 1.8V, and 1.5V DC Voltage Specifications. |
| 05/13/02 | 1.2 | Removed fast Industrial speed grade. Updated 1.5 DC Voltage, V _{OH} parameter from I _{OH} = -0.8 mA to -0.4 mA. Updated AC Electrical Characteristics and added new parameters |