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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H5N2004DL, H5N2004DS

Silicon N Channel MOS FET
High Speed Power Switching

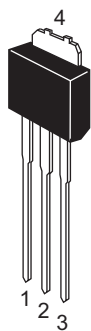
REJ03G1103-0200
(Previous: ADE-208-1372)
Rev.2.00
Sep 07, 2005

Features

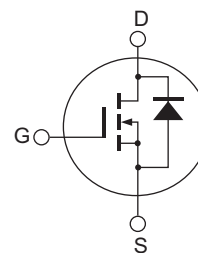
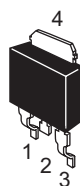
- Low on-resistance: $R_{DS(on)} = 0.38 \Omega$ typ.
- Low leakage current: $I_{DSS} = 1 \mu A$ max (at $V_{DS} = 200 V$)
- High speed switching: $t_f = 10 ns$ typ (at $V_{GS} = 10 V$, $V_{DD} = 100 V$, $I_D = 4 A$)
- Low gate charge: $Q_g = 14 nC$ typ (at $V_{DD} = 160 V$, $V_{GS} = 10 V$, $I_D = 8 A$)
- Avalanche ratings

Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))



RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	200	V
Gate to source voltage	V _{GSS}	±30	V
Drain current	I _D	8	A
Drain peak current	I _{D (pulse)} ^{Note 1}	32	A
Body-drain diode reverse drain current	I _{DR}	8	A
Body-drain diode reverse drain peak current	I _{DR (pulse)} ^{Note 1}	32	A
Avalanche current	I _{AP} ^{Note 3}	7	A
Channel dissipation	P _{ch} ^{Note 2}	30	W
Channel to case thermal impedance	θ _{ch-c}	4.17	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at T_c = 25°C3. T_{ch} ≤ 150°C

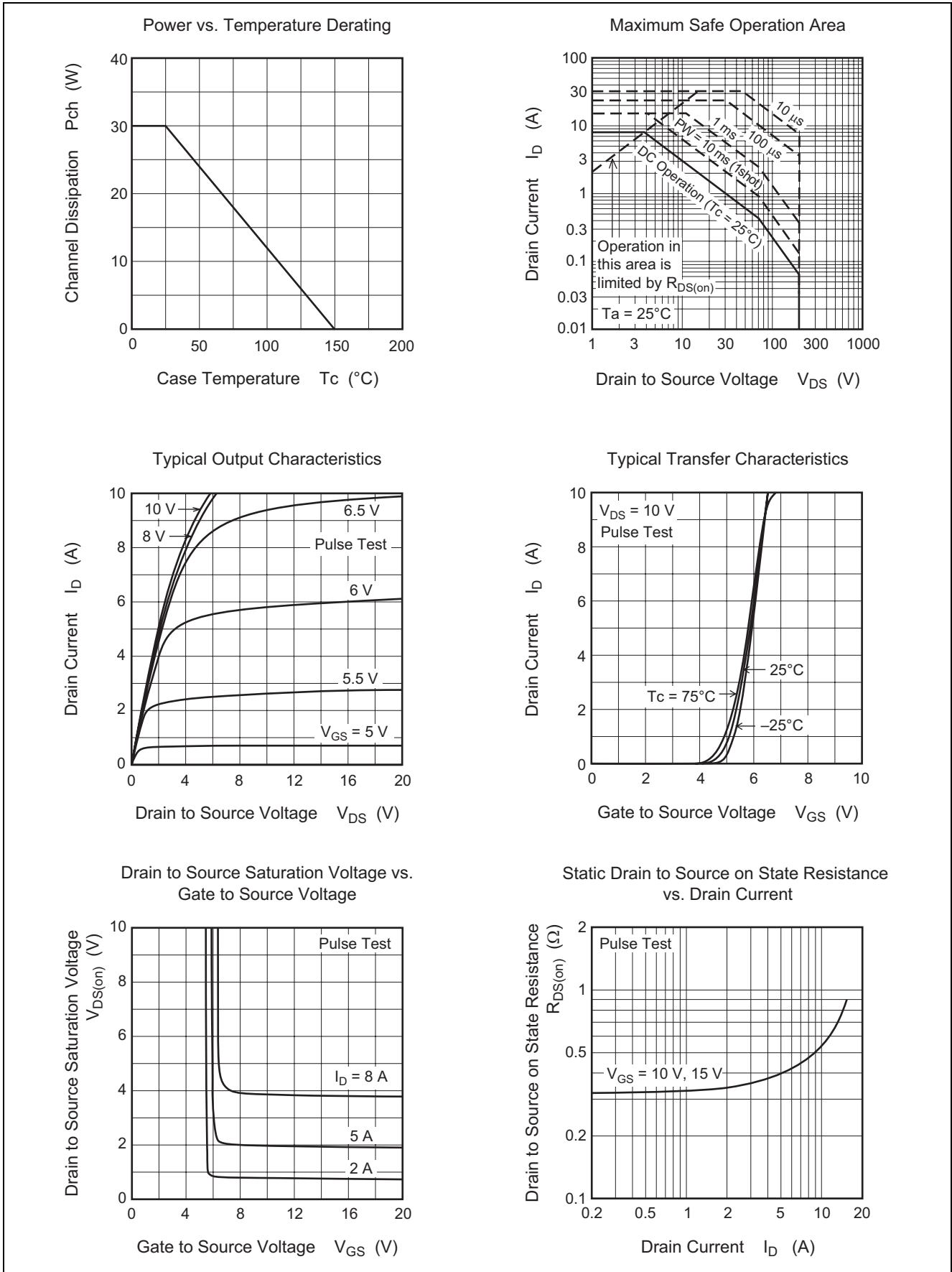
Electrical Characteristics

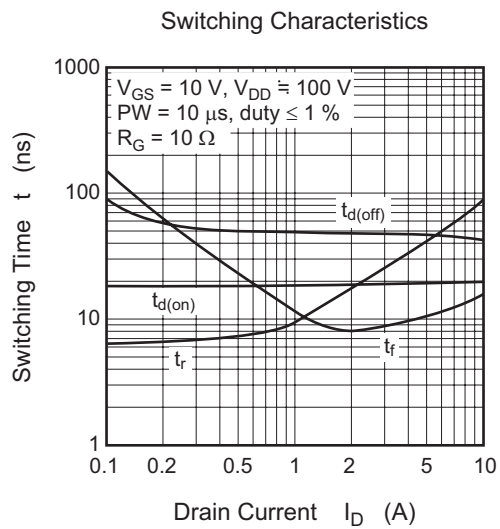
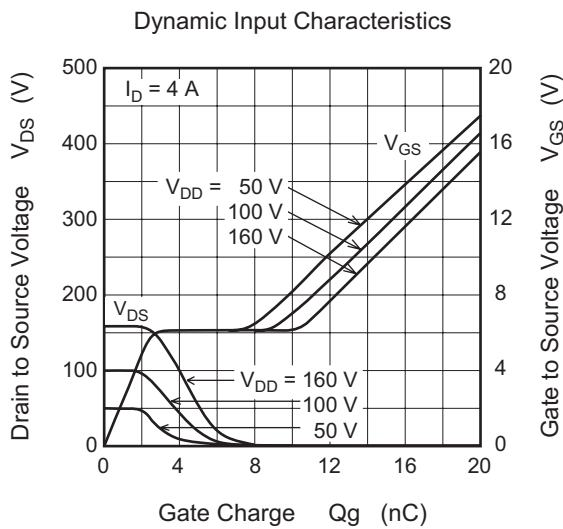
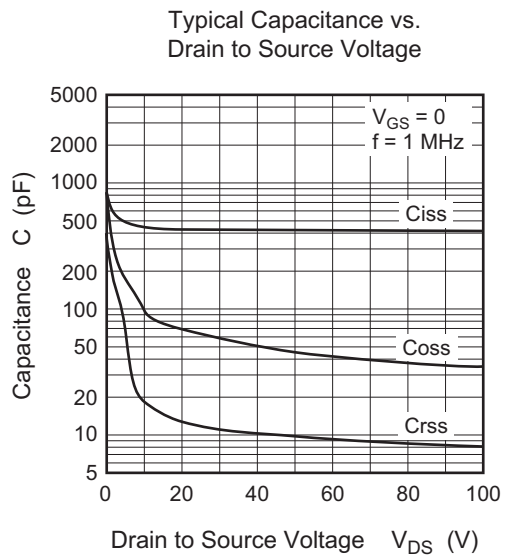
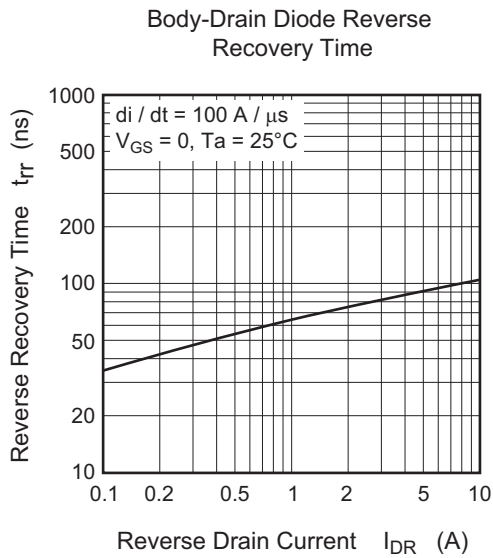
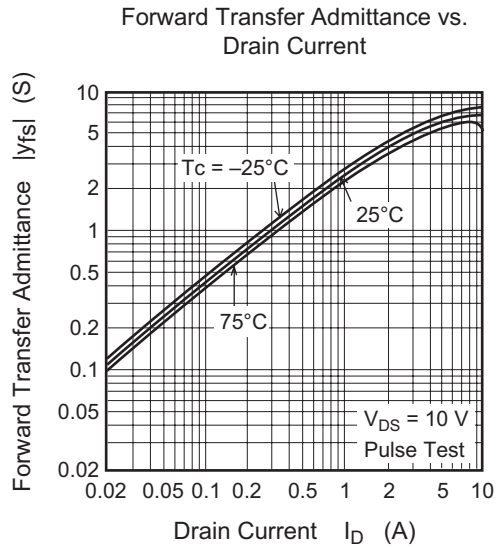
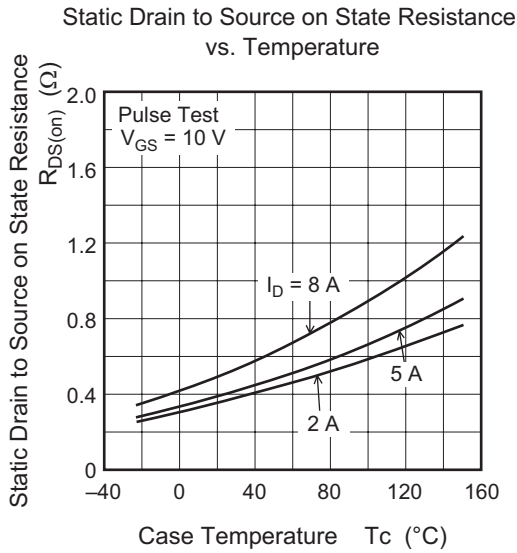
(Ta = 25°C)

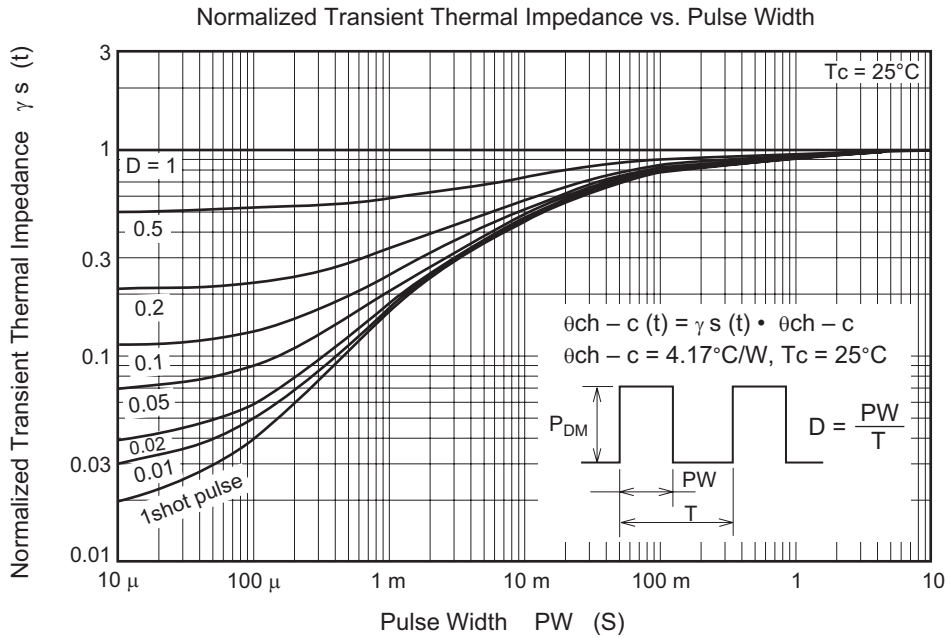
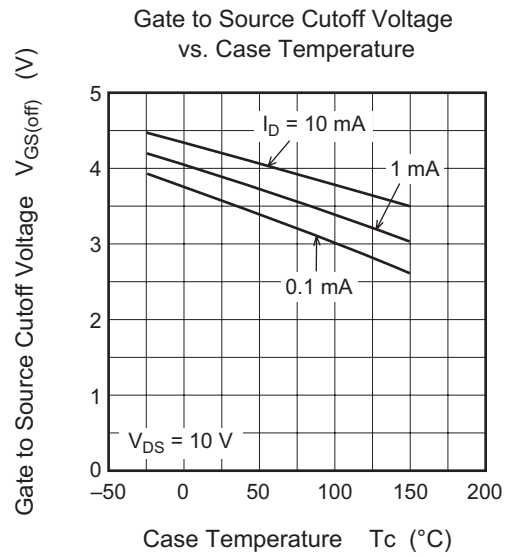
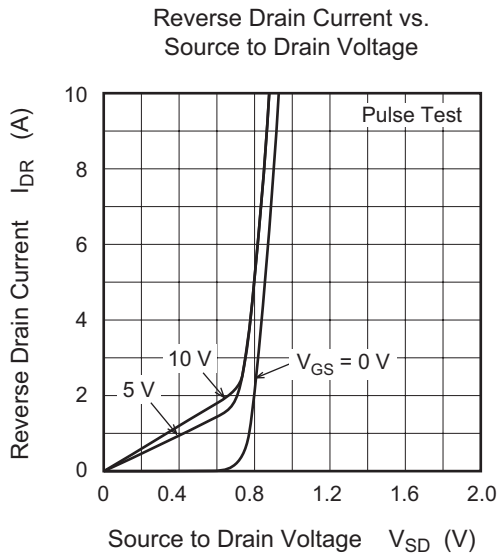
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	200	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	μA	V _{GS} = ±30 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	1	μA	V _{DS} = 200 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS (off)}	3.0	—	4.5	V	V _{DS} = 10 V, I _D = 1 mA
Static drain to source on state resistance	R _{DS (on)}	—	0.38	0.48	Ω	I _D = 4 A, V _{GS} = 10 V ^{Note 4}
Forward transfer admittance	y _{fs}	3.3	5.5	—	S	I _D = 4 A, V _{DS} = 10 V ^{Note 4}
Input capacitance	C _{iss}	—	450	—	pF	V _{DS} = 25 V
Output capacitance	C _{oss}	—	65	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	13	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	19	—	ns	I _D = 4 A
Rise time	t _r	—	32	—	ns	V _{GS} = 10 V
Turn-off delay time	t _{d (off)}	—	47	—	ns	R _L = 25 Ω
Fall time	t _f	—	10	—	ns	R _g = 10 Ω
Total gate charge	Q _g	—	14	—	nC	V _{DD} = 160 V
Gate to source charge	Q _{gs}	—	2.5	—	nC	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	7.5	—	nC	I _D = 4 A
Body-drain diode forward voltage	V _{DF}	—	0.9	1.4	V	I _F = 8 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	100	—	ns	I _F = 8 A, V _{GS} = 0
Body-drain diode reverse recovery charge	Q _{rr}	—	0.4	—	μC	di _F /dt = 50 A/μs

Note: 4. Pulse test

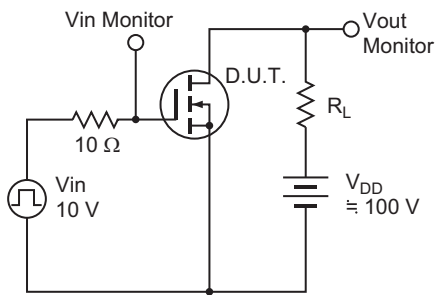
Main Characteristics



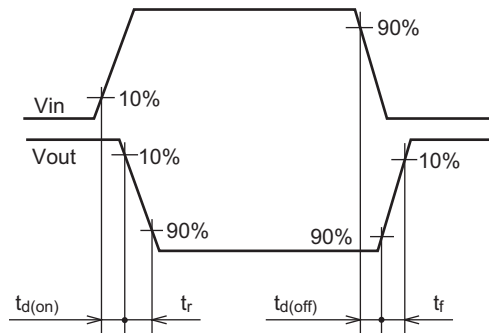




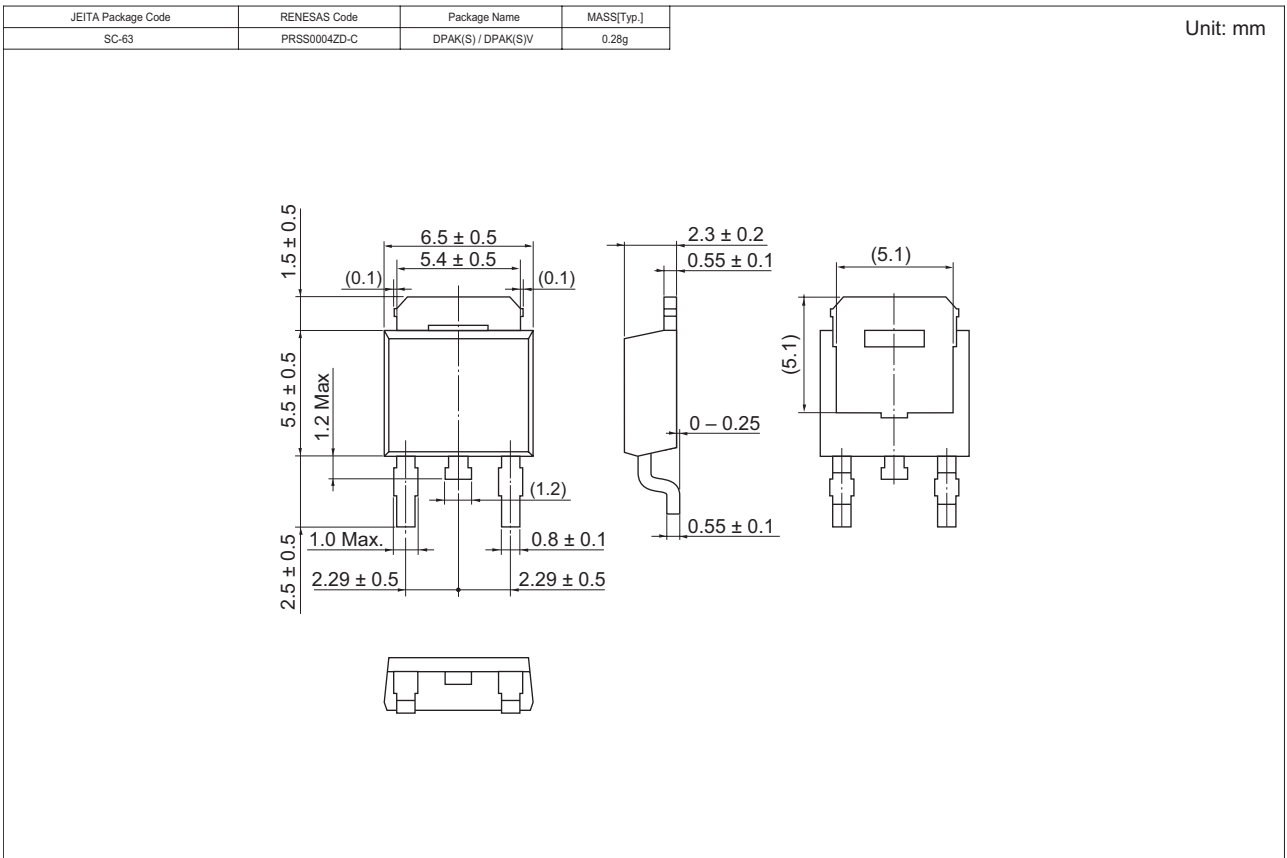
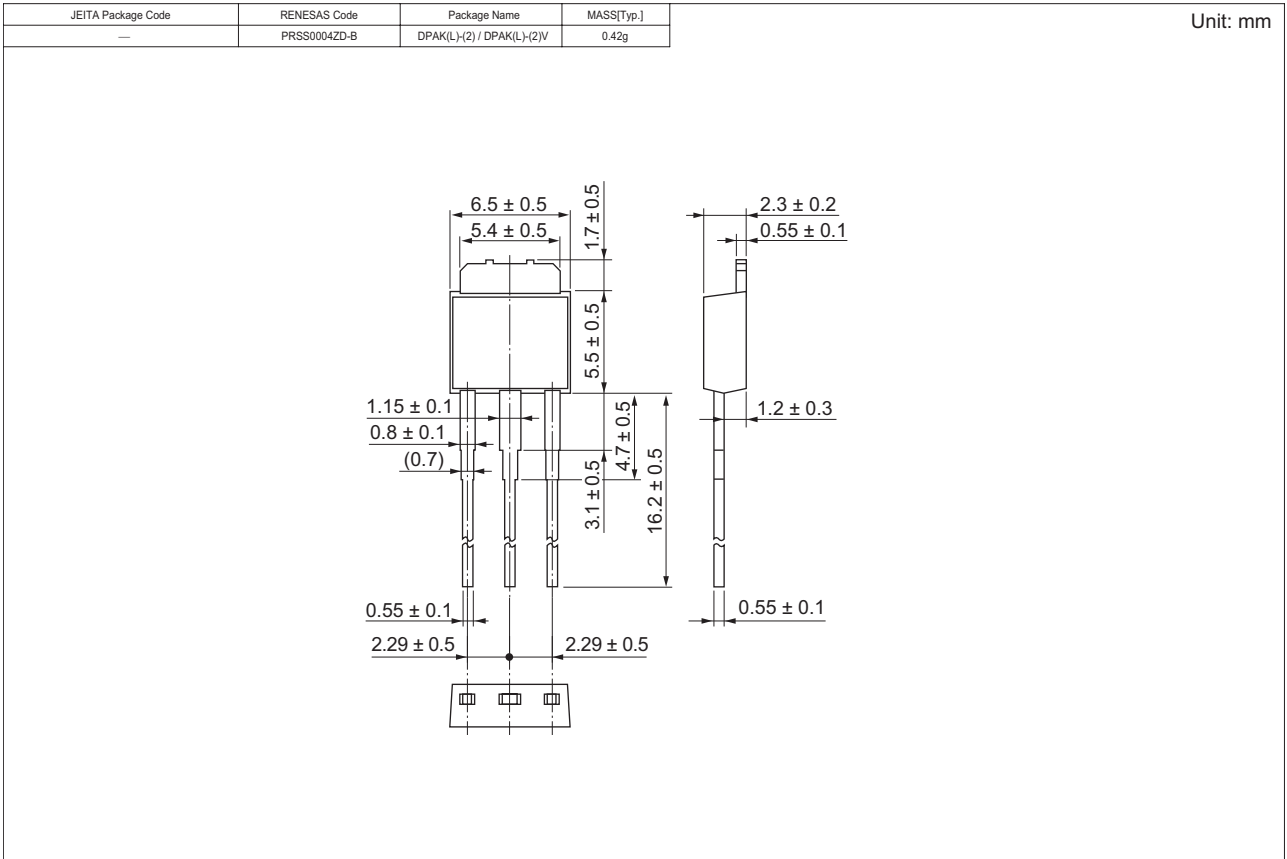
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
H5N2004DL-E	3200 pcs	Box (Sack)
H5N2004DSTL-E	3000 pcs	Taping

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