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LC717A10AJ

CMOS LSI

Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors

Overview

The LC717A10AJ is a high-performance and low-cost capacitance-digital-converter LSI for electrostatic capacitive touch sensor, especially focused on usability.

It has 16 channels capacitance-sensor input. This makes it ideal for use in the products that need many switches.

Since the calibration function and the judgment of ON/OFF are automatically performed in LSI internal, it can make development time more short. A detection result (ON/OFF) for each input can be read out by the serial interface (I²C compatible bus or SPI).

Also, measurement value of each input can be read out as 8-bit digital data. Moreover, gain and other parameters can be adjusted using serial interface.

Features

- Detection system: Differential capacitance detection (Mutual capacitance type)
- Input capacitance resolution: Can detect capacitance changes in the femto Farad order
- Measurement interval (16 differential inputs): 30ms (Typ) (at initial configuration),
6ms (Typ) (at minimum interval configuration)
- External components for measurement: Not required
- Interface: I²C * compatible bus or SPI selectable.
- Current consumption: 570μA (Typ) (V_{DD} = 2.8V), 1.3mA (Typ) (V_{DD} = 5.5V)
- Supply voltage: 2.6V to 5.5V
- Detection operations: Switch
- Packages: SSOP30

* I²C Bus is a trademark of Philips Corporation.

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Specifications

Absolute Maximum Ratings at Ta = +25°C

| Parameter | Symbol | Ratings (V _{SS} = 0V) | Unit | Remarks |
|---------------------|------------------|--------------------------------|------|---|
| Supply voltage | V _{DD} | -0.3 to +6.5 | V | |
| Input voltage | V _{IN} | -0.3 to V _{DD} +0.3 | V | *1 |
| Output voltage | V _{OUT} | -0.3 to V _{DD} +0.3 | V | *2 |
| Power dissipation | Pd max | 160 | mW | Ta = +105°C, Mounted on a substrate *3 |
| Storage temperature | Tstg | -55 to +125 | °C | |

*1) Apply to Cin0 to 15, Cref, CrefAdd, nRST, SCL, SDA, SA0, SA1, SCK, SI, nCS

*2) Apply to Cdrv, SDA, SO, INTOUT

*3) Single-layer glass epoxy board (76.1×114.3×1.6t mm)

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | Conditions | min | typ | max | Unit | Remarks |
|--------------------------|-----------------|------------|-----|-----|-----|------|---------|
| Operating supply voltage | V _{DD} | | 2.6 | | 5.5 | V | |
| Supply ripple + noise | Vpp | | | | ±20 | mV | *1 |
| Operating temperature | Topr | | -40 | 25 | 105 | °C | |

*1) We recommend connecting large and small capacitance between V_{DD} and V_{SS}.

In this case, the small capacitance is equal to or more than 0.1μF, and layout nearby LSI.

Electrical Characteristics at V_{SS} = 0V, V_{DD} = 2.6 to 5.5V, Ta = -40 to +105°C

* Unless otherwise specified, the Cdrv drive frequency is f_{CDRV} = 143kHz.

* Not tested at low temperature before shipment.

| Parameter | Symbol | Conditions | min | typ | max | Unit | Remarks |
|--|--------------------|-----------------------------|------|------|------|--------|---------|
| Capacitance detection resolution | N | | | | 8 | bit | |
| Output noise RMS | N _{RMS} | minimum gain setting | | | ±1.0 | LSB | *1 *3 |
| Input offset capacitance adjustment range | CoffRANGE | | | ±8.0 | | pF | *1 *3 |
| Input offset capacitance adjustment resolution | CoffRESO | | | 8 | | bit | |
| Cin offset drift | CinDRIFT | minimum gain setting | | | ±8 | LSB | *1 |
| Cin detection sensitivity | CinSENSE | minimum gain setting | 0.04 | | 0.12 | LSB/IF | *2 |
| Cin pin leak current | I _{Cin} | Cin = Hi-Z | | ±25 | ±500 | nA | |
| Cin allowable parasitic input capacitance | CinSUB | Cin against V _{SS} | | | 30 | pF | *1 *3 |
| Cdrv drive frequency | f _{CDRV} | | 100 | 143 | 186 | kHz | |
| Cdrv pin leak current | I _{CDRV} | Cdrv = Hi-Z | | ±25 | ±500 | nA | |
| nRST minimum pulse width | t _{NRST} | | 1 | | | μs | *1 |
| Power-on reset time | t _{POR} | | | | 20 | ms | *1 |
| Power-on reset operation condition: Hold time | t _{POROP} | | 10 | | | ms | *1 |
| Power-on reset operation condition: Input voltage | V _{POROP} | | | | 0.1 | V | *1 |
| Power-on reset operation condition: Power supply rise rate | t _{VDD} | 0V to V _{DD} | 1 | | | V/ms | *1 |

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| Parameter | Symbol | Conditions | min | typ | max | Unit | Remarks |
|------------------------|----------------------------------|---|--------------------|-----|--------------------|------|---------|
| Pin input voltage | V _{IH} | High input | 0.8V _{DD} | | | V | *1 *4 |
| | V _{IL} | Low input | | | 0.2V _{DD} | | |
| Pin output voltage | V _{OH} | High output (I _{OH} = +3mA) | 0.8V _{DD} | | | V | *5 |
| | V _{OL} | Low output (I _{OL} = -3mA) | | | 0.2V _{DD} | | |
| SDA pin output voltage | V _{OL} I ² C | SDA Low output (I _{OL} = -3mA) | | | 0.4 | V | |
| Pin leak current | I _{LEAK} | | | | ±1 | μA | *6 |
| Current consumption | I _{DD} | When initial setting and non-touch V _{DD} = 2.8V | | 570 | 700 | μA | *1 *3 |
| | | When initial setting and non-touch V _{DD} = 5.5V | | 1.3 | 1.6 | mA | *1 *3 |
| | I _{STBY} | During Sleep process | | | | 1 | μA |

*1) Design guarantee values (not tested before shipment)

*2) Measurements conducted using the test mode in the LSI

*3) T_a = +25°C

*4) Apply to nRST, SCL, SDA, SA0, SA1, SCK, SI, nCS

*5) Apply to Cdrv, SO, INTOUT

*6) Apply to nRST, SCL, SDA, SA0, SA1, SCK, SI, nCS

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I²C Compatible Bus Timing Characteristics at V_{SS} = 0, V_{DD} = 2.6 to 5.5V, Ta = -40 to +105°C

*Not tested at low temperature before shipment

| Parameter | Symbol | Pin Name | Conditions | min | typ | max | Unit | Remarks |
|-------------------------------------|---------------------------------|------------|------------|-----|-----|-----|------|---------|
| SCL clock frequency | f _{SCL} | SCL | | | | 400 | kHz | |
| START condition hold time | t _{HD;STA} | SCL SDA | | 0.6 | | | μs | |
| SCL clock low period | t _{LOW} | SCL | | 1.3 | | | μs | |
| SCL clock high period | t _{HIGH} | SCL | | 0.6 | | | μs | |
| Repeated START condition setup time | t _{SU;STA} | SCL SDA | | 0.6 | | | μs | *1 |
| Data hold time | t _{HD;DAT} | SCL SDA | | 0 | | 0.9 | μs | |
| Data setup time | t _{SU;DAT} | SCL SDA | | 100 | | | μs | *1 |
| SDA, SCL rise/fall time | t _r / t _f | SCL SDA | | | | 300 | μs | *1 |
| STOP condition setup time | t _{SU;STO} | SCL SDA | | 0.6 | | | μs | |
| STOP-to-START bus release time | t _{BUF} | SCL SDA | | 1.3 | | | μs | *1 |

*1) Design guarantee values (not tested before shipment)

SPI Bus Timing Characteristics at V_{SS} = 0, V_{DD} = 2.6 to 5.5V, Ta = -40 to +105°C

*Not tested at low temperature before shipment

| Parameter | Symbol | Pin Name | Conditions | min | typ | max | Unit | Remarks |
|--|---------------------------------|------------------|------------|-----|-----|-----|------|---------|
| SCK clock frequency | f _{SCK} | SCK | | | | 5 | MHz | |
| SCK clock Low time | t _{LOW} | SCK | | 90 | | | ns | *1 |
| SCK clock High time | t _{HIGH} | SCK | | 90 | | | ns | *1 |
| Input signal rise/fall time | t _r / t _f | nCS SCK SI | | | | 300 | ns | *1 |
| nCS setup time | t _{SU;nCS} | nCS SCK | | 90 | | | ns | *1 |
| SCK clock setup time | t _{SU;SCK} | nCS SCK | | 90 | | | ns | *1 |
| Data setup time | t _{SU;SI} | SCK SI | | 20 | | | ns | *1 |
| Data hold time | t _{HD;SI} | SCK SI | | 30 | | | ns | *1 |
| nCS hold time | t _{HD;nCS} | nCS SCK | | 90 | | | ns | *1 |
| SCK clock hold time | t _{HD;SCK} | nCS SCK | | 90 | | | ns | *1 |
| nCS standby pulse width | t _{CPH} | nCS | | 90 | | | ns | *1 |
| Output high impedance time from nCS | t _{CHZ} | nCS SO | | | | 80 | ns | *1 |
| Output data determination time | t _v | SCK SO | | | | 80 | ns | *1 |
| Output data hold time | t _{HD;SO} | SCK SO | | 0 | | | ns | *1 |
| Output low impedance time from SCK clock | t _{CLZ} | SCK SO | | 0 | | | ns | *1 |

*1) Design guarantee values (not tested before shipment)

Power-on Reset (POR)

When power is turned on, power-on reset is enabled inside the LSI and its state is released after a certain power-on reset time, t_{POR} . Power-on Reset operation condition; Power supply rise rate t_{VDD} must be at least 1V/ms.

Since INTOUT pin changes from “High” to “Low” at the same time as the released of power-on reset, it is possible to verify the timing of release of power-on reset externally.

During power-on reset, C_{in} , C_{ref} and C_{refAdd} are unknown.

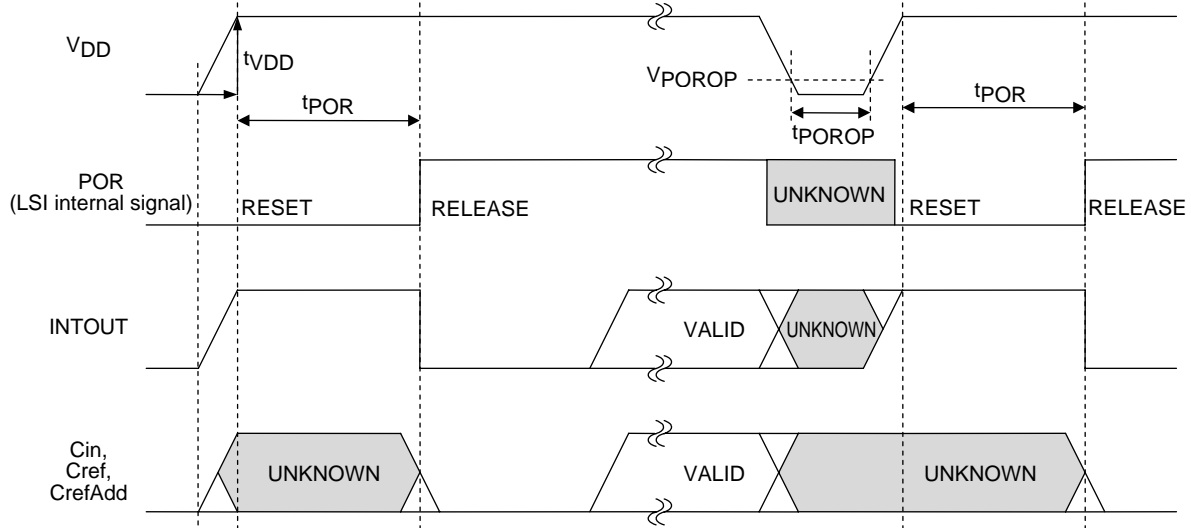


fig.1

I²C Compatible Bus Data Timing

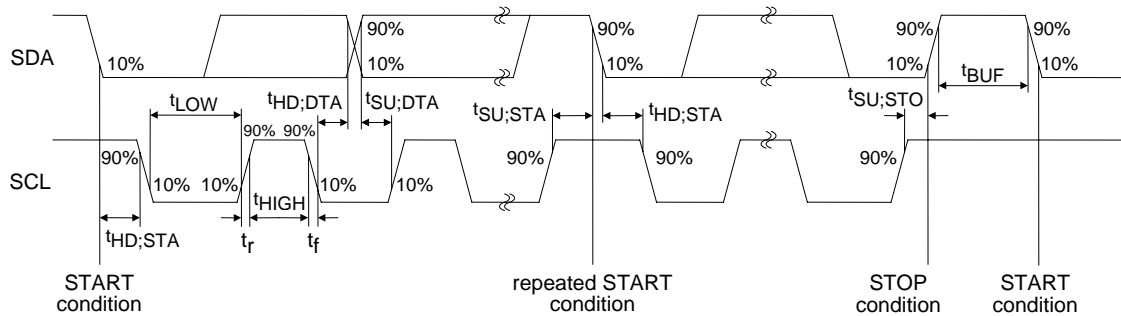


fig.2

I²C Compatible Bus Communication Formats

- Write format (data can be written into sequentially incremented addresses)



fig.3

- Read format (data can be read from sequentially incremented addresses)

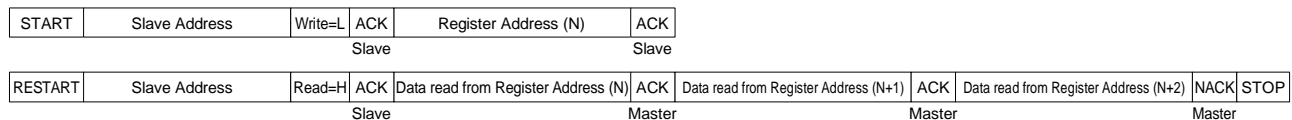


fig.4

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I²C Compatible Bus Slave Address

Selection of two kinds of addresses is possible through the SA0 and SA1 terminals.

| SA1 input | SA0 input | 7bit slave address | Binary notation | 8bit slave address |
|-----------|-----------|--------------------|-------------------|--------------------|
| Low | Low | 0x16 | 00101100b (Write) | 0x2C |
| | | | 00101101b (Read) | 0x2D |
| Low | High | 0x17 | 00101110b (Write) | 0x2E |
| | | | 00101111b (Read) | 0x2F |
| High | Low | 0x18 | 00110000b (Write) | 0x30 |
| | | | 00110001b (Read) | 0x31 |
| High | High | 0x19 | 00110010b (Write) | 0x32 |
| | | | 00110011b (Read) | 0x33 |

SPI Data Timing (SPI Mode 0 / Mode 3)

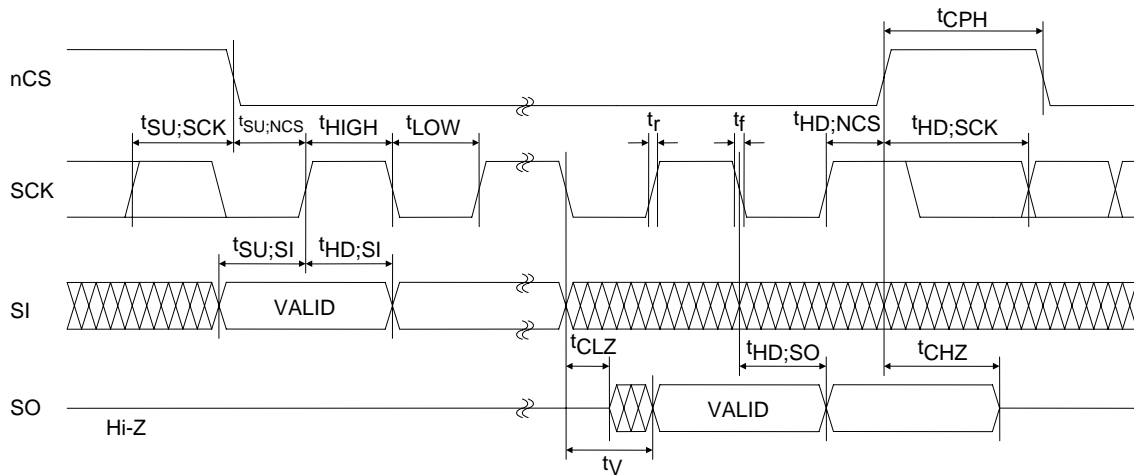


fig.5

SPI Communication Formats (Example of Mode 0)

- Write format (data can be written into sequentially incremented addresses with preserving nCS = L)

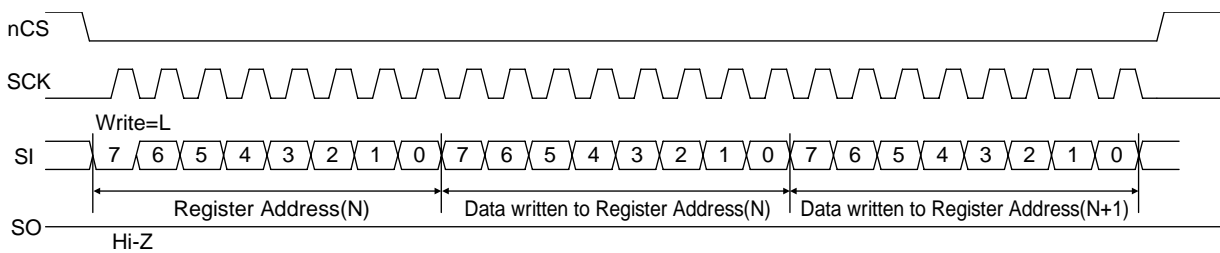


fig.6

- Read format (data can be read from sequentially incremented addresses with preserving nCS = L)

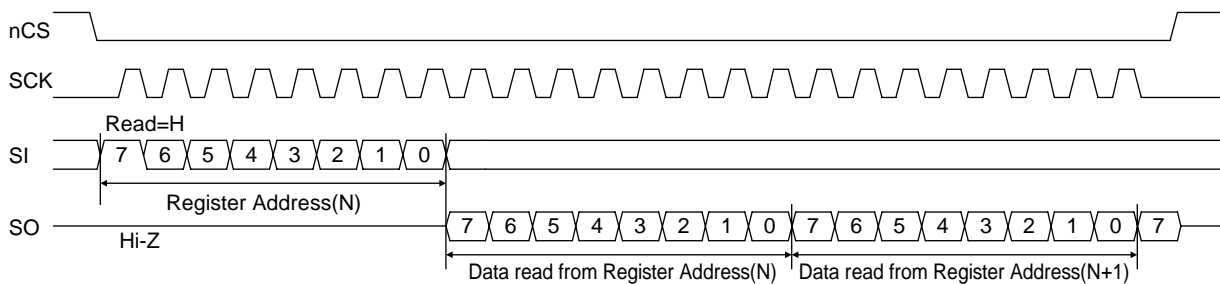


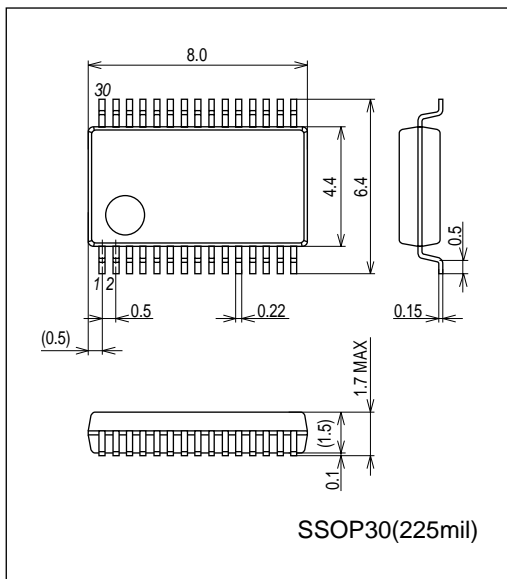
fig.7

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Package Dimensions [LC717A10AJ]

unit : mm (typ)

3421



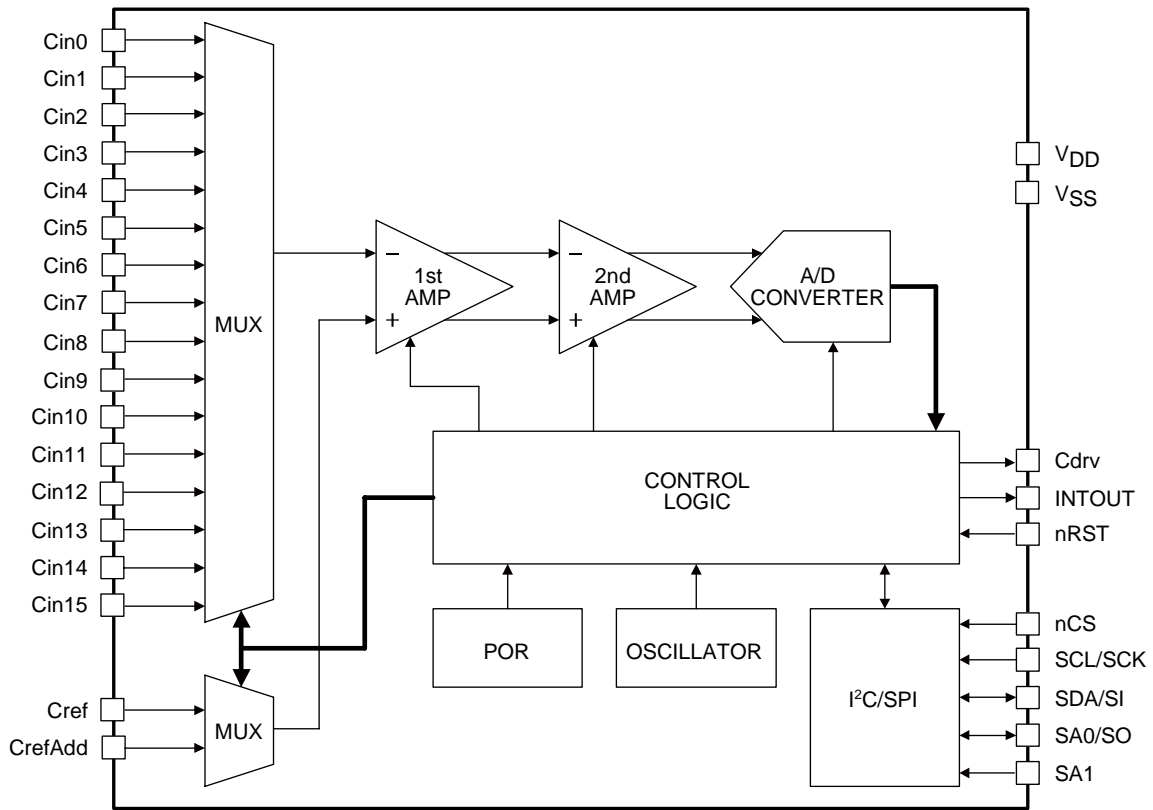
Pin Assignment

| Pin No. | Pin Name | Pin No. | Pin Name |
|---------|-----------------|---------|----------------|
| 1 | V _{DD} | 16 | Cref |
| 2 | V _{SS} | 17 | CrefAdd |
| 3 | Non Connect *1 | 18 | Cdrv |
| 4 | Cin4 | 19 | INTOUT |
| 5 | Cin5 | 20 | SA1 |
| 6 | Cin6 | 21 | SCL/SCK |
| 7 | Cin7 | 22 | SDA/SI |
| 8 | Cin8 | 23 | SA0/SO |
| 9 | Cin9 | 24 | nCS |
| 10 | Cin10 | 25 | nRST |
| 11 | Cin11 | 26 | Non Connect *1 |
| 12 | Cin12 | 27 | Cin0 |
| 13 | Cin13 | 28 | Cin1 |
| 14 | Cin14 | 29 | Cin2 |
| 15 | Cin15 | 30 | Cin3 |

*1) connect to GND when mounted

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Block Diagram



LC717A10AJ is capacitance-digital-converter LSI capable of detecting changes in capacitance in the order of femto Farads. It consists of an oscillation circuit that generates the system clock, a power-on reset circuit that resets the system when the power is turned on, a multiplexer that selects the input channels, a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values, a A/D converter that converts the analog-amplitude values into digital data, an I²C compatible bus or a SPI that enables serial communication with external devices and a control logic that controls the entire chip.

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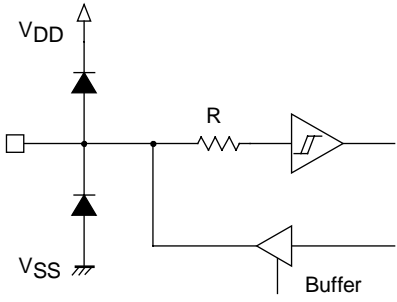
Pin Functions

| Pin Name | I/O | Pin Functions | Pin Type |
|----------|-----|--|----------|
| Cin0 | I/O | Capacitance sensor input | |
| Cin1 | I/O | Capacitance sensor input | |
| Cin2 | I/O | Capacitance sensor input | |
| Cin3 | I/O | Capacitance sensor input | |
| Cin4 | I/O | Capacitance sensor input | |
| Cin5 | I/O | Capacitance sensor input | |
| Cin6 | I/O | Capacitance sensor input | |
| Cin7 | I/O | Capacitance sensor input | |
| Cin8 | I/O | Capacitance sensor input | |
| Cin9 | I/O | Capacitance sensor input | |
| Cin10 | I/O | Capacitance sensor input | |
| Cin11 | I/O | Capacitance sensor input | |
| Cin12 | I/O | Capacitance sensor input | |
| Cin13 | I/O | Capacitance sensor input | |
| Cin14 | I/O | Capacitance sensor input | |
| Cin15 | I/O | Capacitance sensor input | |
| Cref | I/O | Reference capacitance input | |
| CrefAdd | I/O | Reference capacitance input for addition | |
| Cdrv | O | Output for capacitance sensors drive | |
| INTOUT | O | Interrupt output | |
| SCL/SCK | I | Clock input (I ² C) / Clock input (SPI) | |
| nCS | I | Interface selection / Chip select inverting input (SPI) | |
| nRST | I | External reset signal inverting input | |
| SA1 | I | Slave address selection (I ² C) | |
| SDA/SI | I/O | Data input and output (I ² C) / Data input (SPI) | |

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| Pin Name | I/O | Pin Functions | Pin Type |
|-----------------|-----|---|--|
| SA0/SO | I/O | Slave address selection (I ² C) / Data output (SPI) |  |
| V _{DD} | | Power supply (2.6V to 5.5V) *1 | |
| V _{SS} | | Ground (Earth) *1 *2 | |

*1) Inserting a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} is recommended. In this case, the small-valued capacitor should be at least 0.1μF, and is mounted near the LSI.

*2) When V_{SS} terminal is not grounded in battery-powered mobile equipment, detection sensitivity may be degraded.

Details of Pin Functions

●Cin0 to Cin15

These are the capacitance-sensor-input pins. These pins are used by connecting them to the touch switch pattern.

Cin and the Cdrv wire patterns should be close to each other. By doing so, Cdrv and Cin patterns are capacitively coupled. Therefore, LSI can detect capacitance change near each pattern as 8bit digital data.

However, if the shape of each pattern or the capacitively coupled value of Cdrv is not appropriate, it may not be able to detect the capacitance change correctly.

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cin0 to Cin15 are connected to the inverting input of the 1st amplifier.

During measurement process, channels other than the one being measured are all in “Low” condition.

Leave the unused terminals open.

●Cref, CrefAdd

These are the reference-capacitance-input pins. These are used by connecting to the wire pattern like Cin pins or are used by connecting any capacitance between this pin and Cdrv pin.

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cref is connected to the non-inverting input of the 1st amplifier.

Due to the parasitic capacitance generated in the wire connections of Cin pins and their patterns, as well as the one generated between the wire patterns of Cin and Cdrv pins, Cref may not detect capacitance change of each Cin pin accurately. In this case, connect an appropriate capacitance between Cref and Cdrv to detect capacitance change accurately.

However, if the difference between the parasitic capacitance of each Cin pin is extremely large, it may not detect capacitance change of each Cin pin correctly.

CrefAdd can be used as additional terminal for Cref. Leave the CrefAdd open if not in used.

●Cdrv

It is the output pin for capacitance sensors drive. It outputs the pulse voltage which is needed to detect capacitance at Cin0 to Cin15.

Cdrv and Cin wire patterns should be close to each other so that they are capacitively coupled.

●INTOUT

It is the interrupt-output pin.

It is used by connecting to a main microcomputer if necessary, and use as interrupt signal. (High Active)

Leave the terminal open if not in used.

●SCL/SCK

Clock input (I²C) / Clock input (SPI)

It is the clock input pin of the I²C compatible bus or the SPI depending on the mode of operation.

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- nCS

Interface selection / Chip-select-inverting input (SPI)

Selection of I²C compatible bus mode or SPI mode is through this terminal. After initialization, the LSI is automatically in I²C compatible bus mode. To continually use I²C compatible bus mode, fix nCS pin to “High”. To switch to SPI mode after LSI initialization, change the nCS input “High” → “Low”. The nCS pin is used as the chip-select-inverting input pin of SPI, and SPI mode is kept until LSI is again initialized.

- nRST

It is the external-reset-signal-inverting-input pin. When nRST pin is “Low”, LSI is in reset state.

Each pin (Cin0 to 15, Cref, CrefAdd) is “Hi-Z” during reset state.

- SDA/SI

Data input and output (I²C) / Data input (SPI)

It is the data input and output pin of the I²C compatible bus or the data input pin of the SPI depending on the mode of operation.

- SA0/SO

Slave address selection (I²C) / Data output (SPI)

It is the slave address selection pin of the I²C compatible bus or the data output pin of the SPI depending on the mode of operation.

- SA1

Slave address selection (I²C)

It is the slave address selection pin of the I²C compatible bus.

When SPI mode, connect to the SA1 pin to GND.

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