MN103SJ7/N0/N1/N2/N4/N5/N6 Series

32-bit Single-chip Microcontroller

■ Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, DMA controller, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multifunctional system on LSI for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Pins	Timer (8bit/ 16bit)	PWM	Serial I/F	A/D	VGA	Package
MN103SFJ7A	32 KB	2 KB	TQFP48	8/1	1	2	2	—	TQFP48-P-0707B
MN103SFN0D	64 KB	4KB	QFP44 TQFP48	8/2	1	2	2	—	QFP044-P-1010F TQFP48-P-0707B
MN103SFN0X		8 KB							
MN103SFN0G	128 KB	6 KB							
MN103SFN0Y		8 KB							
MN103SFN1D	64 KB	4 KB	TQFP64	12/3	2	3	2	—	TQFP064-P-1010C
MN103SFN1X		8 KB							
MN103SFN1G	128 KB	6 KB							
MN103SFN1Y		8 KB							
MN103SFN2D	64 KB	4 KB	TQFP80	12/5	2	3	2	—	TQFP080-P-1212D
MN103SFN2X		8 KB							
MN103SFN2G	128 KB	6 KB							
MN103SFN2Y		8 KB							
MN103SFN4D	64 KB	4 KB	QFP44 TQFP48	8/2	1	2	2	1	QFP044-P-1010F TQFP48-P-0707B
MN103SFN4X		8 KB							
MN103SFN4G	128 KB	6 KB							
MN103SFN4Y		8 KB							
MN103SFN5D	64 KB	4 KB	TQFP64	12/3	2	3	2	2	TQFP064-P-1010C
MN103SFN5X		8 KB							
MN103SFN5G	128 KB	6 KB							
MN103SFN5Y		8 KB							
MN103SFN6D	64 KB	4 KB	TQFP80	12/5	2	3	2	2	TQFP080-P-1212D
MN103SFN6X		8 KB							
MN103SFN6G	128 KB	6 KB							
MN103SFN6Y		8 KB							

■ Features

• CPU core

MN103S core

4 GB of address space (for instructions / data)

LOAD/STORE architecture with 5-stage pipeline

46 basic instructions + 8 extension instructions

6 addressing modes

Instruction set of 1 byte in word length

Extension arithmetic unit incorporated (high-speed multiply instruction, high-speed division instruction etc.)

Machine cycle: 16.7 ns (oscillation frequency: 10 MHz, 6 multiplying)

Operation mode: NORMAL mode, SELLP mode, HALT mode, STOP mode

• Oscillation Circuit

External oscillation (crystal/ ceramic)

Clock multiply circuit Oscillation clock can be multiplied by from 3 to 12

• Internal memory

ROM: 32 K/64 K/128 K bytes   RAM: 2 K/4 K/6 K/8 K bytes

The ROM/RAM size is different in each product.

Please refer to [■ Product Summary] for details.

• DMA Controller

Number of channels: 1 channel

Startup sources:	15 sources (MN103SFN0/N4 series)
	20 sources (MN103SFN1/N5 series)
	22 sources (MN103SFN2/N6 series)
	(External interrupts: Max 12 sources, Serial Interface: Max 9 sources, Software start: 1 source)
Transfer modes:	3 modes (One word transfer, Burst transfer, Intermittent transfer)

*: There is not the function in the MN103SFJ7A.

• Interrupts

Non-maskable interrupts

Watchdog timer overflow interrupts

System error interrupts

Fail safe function interrupts

Internal interrupts (Level interrupt)

MN103SFJ7A   : 23 interrupts

MN103SFN0/N4 series: 29 interrupts

MN103SFN1/N5 series: 42 interrupts

MN103SFN2/N6 series: 48 interrupts

<Timer Interrupts>

Timer 0 underflow interrupt

Timer 1 underflow interrupt

Timer 2 underflow interrupt

Timer 3 underflow interrupt

Timer 4 underflow interrupt

Timer 5 underflow interrupt

Timer 6 underflow interrupt

Timer 7 underflow interrupt

Timer 8 underflow interrupt

Timer 9 underflow interrupt

Timer 10 underflow interrupt

Timer 11 underflow interrupt

Timer 16 overflow/underflow interrupt

Timer 16 compare/capture A interrupt

■ Features (continued)

<Timer Interrupts> (continued)
Timer 16 compare/capture B interrupt
Timer 17 overflow/underflow interrupt
Timer 17 compare/capture A interrupt
Timer 17 compare/capture B interrupt
Timer 18 overflow/underflow interrupt
Timer 18 compare/capture A interrupt
Timer 18 compare/capture B interrupt
Timer 19 overflow/underflow interrupt
Timer 19 compare/capture A interrupt
Timer 19 compare/capture B interrupt
Timer 20 overflow/underflow interrupt
Timer 20 compare/capture A interrupt
Timer 20 compare/capture B interrupt

<Serial Interface>
Serial 0 reception end interrupts
Serial 0 communication/transmission end interrupts
Serial 1 reception end interrupts
Serial 1 communication/transmission end interrupts
Serial 2 reception end interrupts
Serial 2 communication/transmission end interrupts

<PWM>
PWM0 overflow interrupts
PWM0 underflow interrupts
PWM0 synchronous A/D start A
PWM0 synchronous A/D start B
PWM1 overflow interrupts
PWM1 underflow interrupts
PWM1 synchronous A/D start A
PWM1 synchronous A/D start B

<A/D>
A /D 0 conversion end interrupt
A /D 0 conversion end B interrupt
A /D 1 conversion end interrupt
A /D 1 conversion end B interrupt

<DMA>
DMA transfer end interrupt
DMA request after DMA transfer end interrupt
DMA transfer request overflow interrupt

External interrupts:
MN103SFJ7A   : 4 interrupts
MN103SFN0/N4 series : 8 interrupts
MN103SFN1/N5 series : 10 interrupts
MN103SFN2/N6 series : 12 interrupts

External interrupt pins   : From IRQ00 to IRQ11
Interrupt detection condition : Each edge, both edges, high-level and low-level detection
Each interrupt detection condition is able

■ Features (continued)

● Timer counter

8-bit timer	8 sets (MN103SFJ7A, MN103SFN0/N4 series)
	12 sets (MN103SFN1/N5, MN103SFN2/N6 series)
16-bit timer	1 sets (MN103SFJ7A)
	2 sets (MN103SFN0/N4 series)
	3 sets (MN103SFN1/N5 series)
	5 sets (MN103SFN2/N6 series)

Timer 0 (8-bit timer)
  Interval timer, Timer pulse output, Event count, Baud rate timer
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM0IO pin input,
                Timer 1 underflow, Timer 2 underflow

Timer 1 (8-bit timer)
  Interval timer, Timer pulse output, Event count, Baud rate timer, Cascade connection (connected to Timer 0)
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM1IO pin input,
                Timer 0 underflow, Timer 2 underflow

Timer 2 (8-bit timer)
  Interval timer, Timer pulse output [*1], Event count [*1], Baud rate timer, Cascade connection (connected to Timer 1)
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM2IO pin input [*1],
                Timer 0 underflow, Timer 1 underflow

Timer 3 (8-bit timer)
  Interval timer, Timer pulse output [*1], Event count [*1], Baud rate timer, Cascade connection (connected to Timer 2)
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM3IO pin input [*1],
                Timer 0 underflow, Timer 1 underflow, Timer 2 und

Timer 4 (8-bit timer)
  Interval timer, Timer pulse output, Event count
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM4IO pin input,
                Timer 5 underflow, Timer 6 underflow

Timer 5 (8-bit timer)
  Interval timer, Timer pulse output, Event count, Cascade connection (connected to Timer 4)
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM5IO pin input,
                Timer 4 underflow, Timer 6 underflow

Timer 6 (8-bit timer)
  Interval timer, Timer pulse output, Event count, Cascade connection (connected to Timer 5)
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM6IO pin input,
                Timer 4 underflow, Timer 5 underflow

Timer 7 (8-bit timer)
  Interval timer, Timer pulse output, Event count, Cascade connection (connected to Timer 6)
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM7IO pin input,
                Timer 4 underflow, Timer 5 underflow, Timer 6 und

Timer 8 (8-bit Timer) [*2]
  Interval timer, Timer pulse output [*3], Event count [*3]
  Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM8IO pin input [*3],
                Timer 9 underflow, Timer 10 underflow

■ Features (continued)

• Timer counter (continued)

Timer 9 (8-bit timer) [2]

Interval timer, Timer pulse output [3], Event count [3], Cascade connection (Connected to Timer 8)

Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM9IO pin input [3],

Timer 8 underflow, Timer 10 underflow

Timer 10 (8-bit timer) [2]

Interval timer, Timer pulse output, Event count, Cascade connection (Connected to Timer 9)

Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM10IO pin input,

Timer 8 underflow, Timer 9 underflow

Timer 11 (8-bit timer) [2]

Interval timer, Timer pulse output, Event count, Cascade connection (Connected to Timer 10)

Count clock source : IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM11IO pin input,

Timer 8 underflow, Timer 9 underflow, Timer 10 un

Timer 16 (16-bit timer)

Interval timer, Event count, Up/down count, Timer output, PWM output, Input capture, one-shot output, External trigger start

Start by PWMn overflow interrupt, PMWn underflow interr

Count clock source : IOCLK, IOCLK/8, Timer 6 underflo

Timer 17 (16-bit timer) [2],[4]

Interval timer, Event count, Up/down count, Timer output, PWM output, Input capture, one-shot output, External trigger start

Count clock source : IOCLK, IOCLK/8, IOCLK/64, Timer

Timer 18 (16-bit timer) [5]

Interval timer, Event count, Up/down count, Timer output, PWM output (output to 6 ports all at once is possible),

Input capture, one-shot output, External trigger start

Count clock source : IOCLK, IOCLK/8, IOCLK/64, Timer

Timer 19 (16-bit timer) [2]

Interval timer, Event count, Up/down count, Timer output, PWM output, Input capture, one-shot output, External trigger start

Start by PWMn overflow interrupt, PWMn underflow interr

Count clock source : IOCLK, IOCLK/8, Timer 10 underflo

Timer 20 (16-bit timer) [2],[4]

Interval timer, Event count, Up/down count, Timer output, PWM output, Input capture, one-shot output, External trigger start,

Count clock source : IOCLK, IOCLK/8, Timer 6 underflow

Note) [1]: The function using the TMnIO pin (n = 2, 3) cannot be used by the MN103SFN0/N4 series.

[2]: There is not the function in the MN103SFN0/N4 series.

[3]: The function using the TMnIO pin (n = 8, 9) cannot be used by the MN103SFN1/N5 series.

[4]: There is not the function in the MN103SFN1/N5 series.

[5]: There is not the function in the MN103SJ7A.

■ Features (continued)

• Watchdog Timer

Detection time   6.55 ms to 1677.72 ms (oscillation frequency 10 MHz)

Generates non-maskable interrupt at detection

Generates hard-reset at second consective overflow

• A /D Converter

A/D0

Resolution   10 bits

Minimum conversion time   0.5 ms

Analog input 5 channels (AD0IN00 to AD0IN04)

A/D conversion start trigger is in synchronization with complementary 3-phase PWM cycle and 16-bit timer

A/D1

Resolution   10 bits

Minimum conversion time   0.5 ms

Analog input

MN103SFJ7A   : 3 channels (AD1IN00 to AD1IN02)

MN103SFN0/N4 series: 3 channels (AD1IN00 to AD1IN02)

MN103SFN1/N5 series: 7 channels (AD1IN00 to AD1IN06)

MN103SFN2/N6 series: 11 channels (AD1IN00 to AD1IN10)

A/D conversion start trigger is in synchronization with complementary 3-phase PWM cycle and 16-bit timer

• Complementary 3-phase PWM output

Min. resolution: 16.7 ns

Triangular and saw-tooth waves output

Incorporates a dead time insertion circuit

Can overwrite registers by double buffer during PWM operation

PWM output protection circuit supporting external interrupts and non-maskable interrupt

Output timing varying function

A/D conversion start trigger, 16-bit timer start trigger

• VGA

VGA

MN103SFN4 series   1 sets

MN103SFN5/N6 series   2 sets

The gain of eight stages can be set (2.05, 3.03, 4.00, 4.98, 5.96, 7.90, 9.83, and 19.40times)

Offset voltage cancel cansel function(short-circuit or switching)

■ Features (continued)

• Serial Interface   3 channels

    Serial 0 (Full duplex UART / Synchronous serial interface)

        Synchronous serial interface

         Overrun error detection

         Transfer clock source:

                    1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,

                    1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,

                    1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,

                    1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,

            IOCLK/2, IOCLK/4, SBT0 pin

              Can be selected as the first bit to be transferred, An

        Can be continuously transmitted, received or transmitted and received.

        Maximum transfer rate: 5.0 Mbps

        Full duplex UART

              Parity check, Overrun and flaming error detection

         Transfer clock source:

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

            IOCLK/16, IOCLK/32, IOCLK/64

              Can be selected as the first bit to be transferred, An

        Continuous transmission, reception, and transmission/reception

        Maximum transfer rate: 300 kbps

    Serial 1 (Full duplex UART / Synchronous serial interface)

        Synchronous serial interface

         Overrun error detection

         Transfer clock source:

                    1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,

                    1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,

                    1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,

                    1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,

            IOCLK/2, IOCLK/4, SBT1 pin

              Can be selected as the first bit to be transferred, An

        Continuous transmission, reception, and transmission/reception

        Maximum transfer rate: 5.0 Mbps

        Full duplex UART

              Parity check, Overrun and flaming error detection

         Transfer clock source:

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 o

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

                    1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

            IOCLK/16, IOCLK/32, IOCLK/64

              Can be selected as the first bit to be transferred, An

        Continuous transmission, reception, and transmission/reception

        Maximum transfer rate: 300 kbps

■ Features (continued)

Serial 2 (Full duplex UART / Synchronous serial interface)

    Synchronous serial interface

      Overrun error detection

      Transfer clock source

```
1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,
```

        IOCLK/2, IOCLK/4, SBT2 pin

```
Can be selected as the first bit to be transferred, An
```

      Continuous transmission, reception and transmission / reception

      Maximum transfer rate: 5.0 Mbps

      Corresponding to the 4 channel system communication and the SPI communication

    Full duplex UART

```
Parity check, Overrun and flaming error detection
```

      Transfer clock source

```
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of
```

        IOCLK/16, IOCLK/32, IOCLK/64

```
Can be selected as the first bit to be transferred, An
```

      Continuous transmission, reception and transmission / reception

      Maximum transfer rate: 300 kbps

● Regulator

    Incorporates regulator, and use of 5 V power supply is possible

● Power Supply Detection

    Detection level   3.6 V to 4.3 V

    When power supply voltage is under detection level, reset is generated.

■ Features (continued)

Serial 2 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Overrun error detection

Transfer clock source

1 / 2, 1 / 4, 1 / 16 and 1 / 64 of timer 0 underflow,
1 / 2, 1 / 4, 1 / 16 and 1 / 64 of timer 1 underflow,
1 / 2, 1 / 4, 1 / 16 and 1 / 64 of timer 2 underflow,
1 / 2, 1 / 4, 1 / 16 and 1 / 64 of timer 3 underflow,

IOCLK/2, IOCLK/4, SBT2 pin

Can be selected as the first bit to be transferred, An

Continuous transmission, reception and transmission / reception

Maximum transfer rate: 5.0 Mbps

Corresponding to the 4 channel system communication and the SPI communication

Full duplex UART

Parity check, Overrun and flaming error detection

Transfer clock source

1 / 16, 1 / 32, 1 / 64, 1 / 128, 1 / 256, 1 / 512 and 1 / 1024 of
1 / 16, 1 / 32, 1 / 64, 1 / 128, 1 / 256, 1 / 512 and 1 / 1024 of
1 / 16, 1 / 32, 1 / 64, 1 / 128, 1 / 256, 1 / 512 and 1 / 1024 of
1 / 16, 1 / 32, 1 / 64, 1 / 128, 1 / 256, 1 / 512 and 1 / 1024 of

IOCLK/16, IOCLK/32, IOCLK/64

Can be selected as the first bit to be transferred, An

Continuous transmission, reception and transmission / reception

Maximum transfer rate: 300 kbps

- Regulator

Incorporates regulator, and use of 5 V power supply is possible

- Power Supply Detection

Detection level   3.6 V to 4.3 V

When power supply voltage is under detection level, reset is generated.

■ Features (continued)

Serial 2 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Overrun error detection

Transfer clock source

1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,

IOCLK/2, IOCLK/4, SBT2 pin

Can be selected as the first bit to be transferred, An

Continuous transmission, reception and transmission / reception

Maximum transfer rate: 5.0 Mbps

Corresponding to the 4 channel system communication and the SPI communication

Full duplex UART

Parity check, Overrun and flaming error detection

Transfer clock source

1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of

IOCLK/16, IOCLK/32, IOCLK/64

Can be selected as the first bit to be transferred, An

Continuous transmission, reception and transmission / reception

Maximum transfer rate: 300 kbps

- Regulator

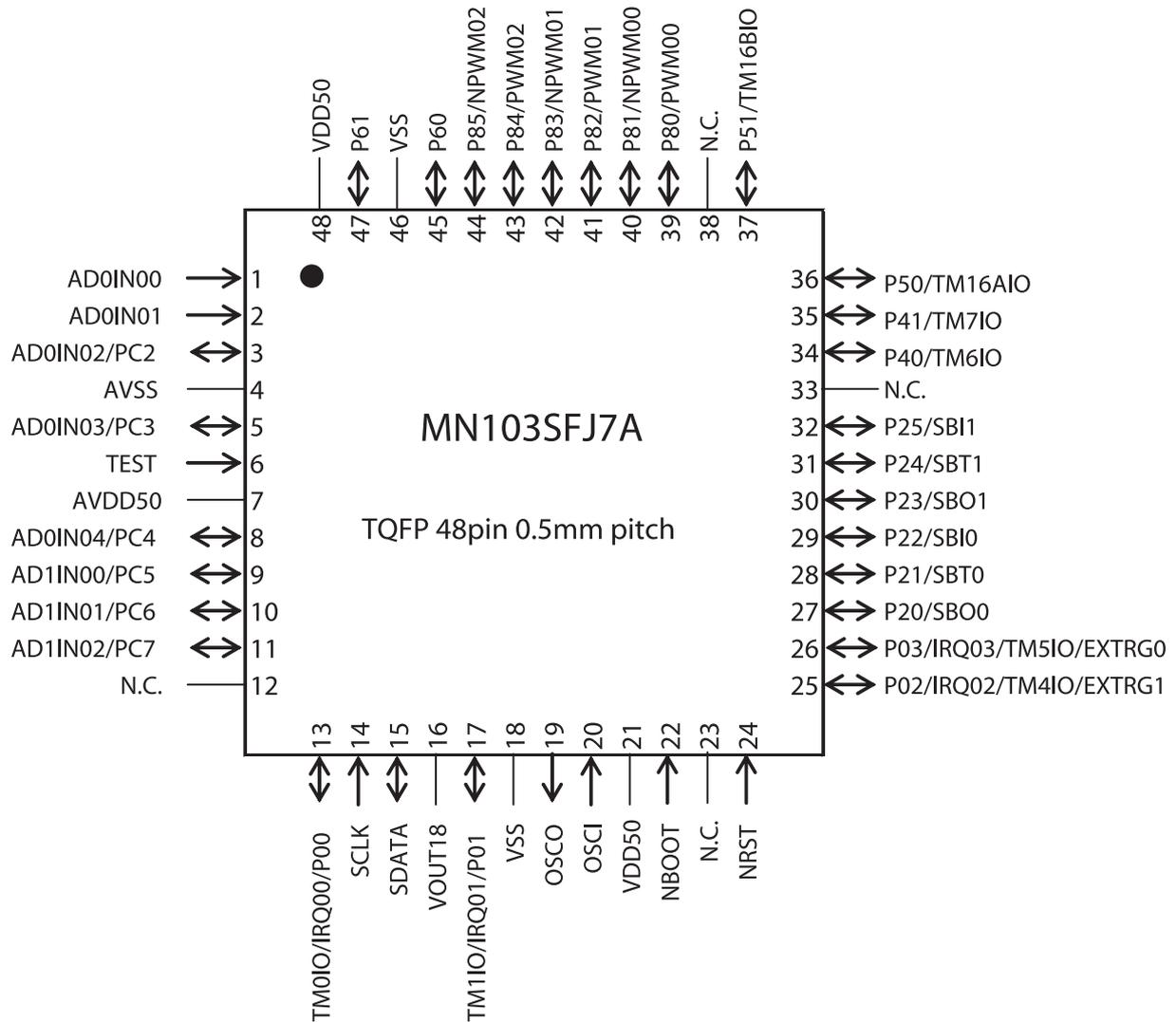Incorporates regulator, and use of 5 V power supply is possible

- Power Supply Detection

Detection level   3.6 V to 4.3 V

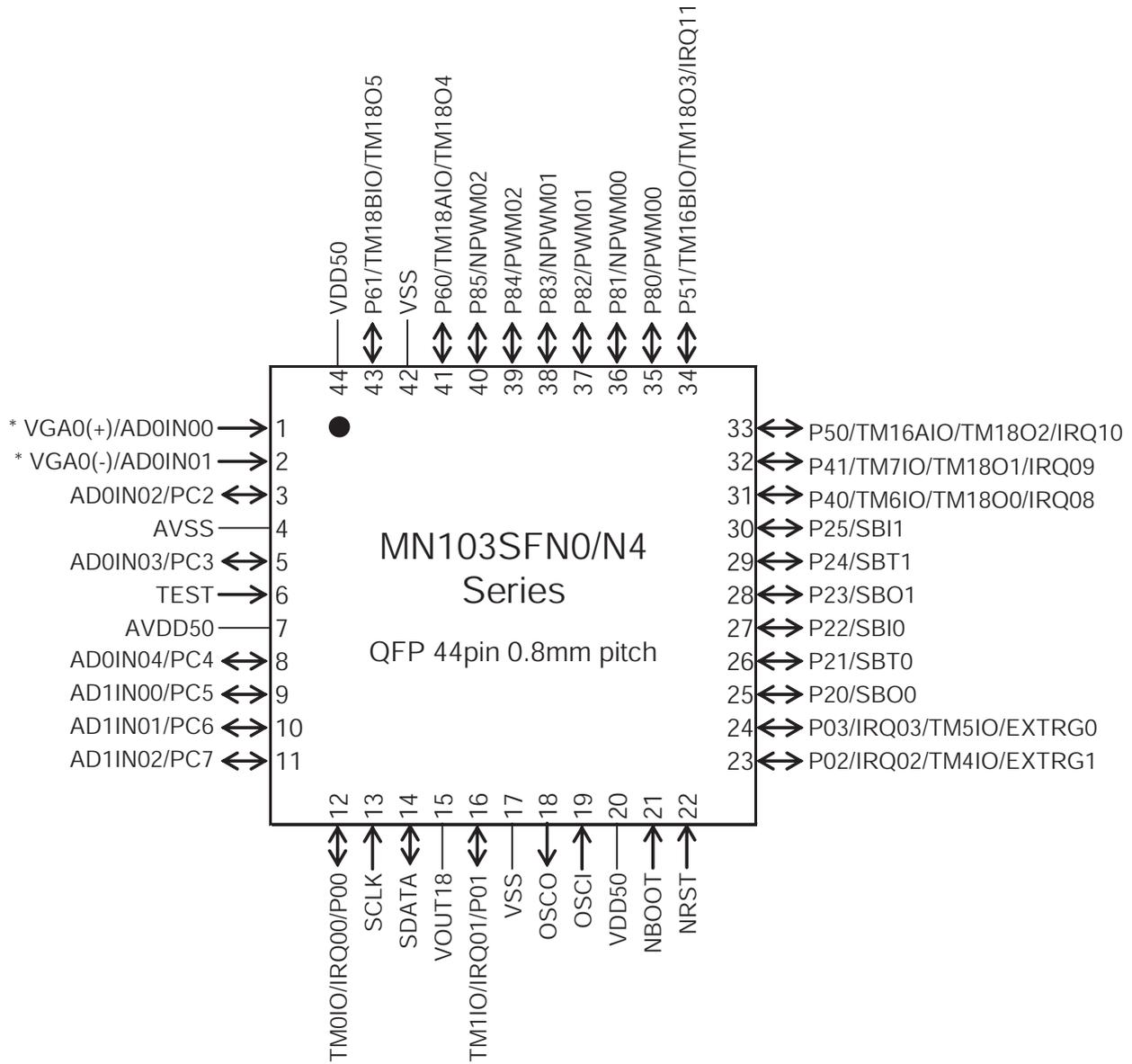When power supply voltage is under detection level, reset is generated.

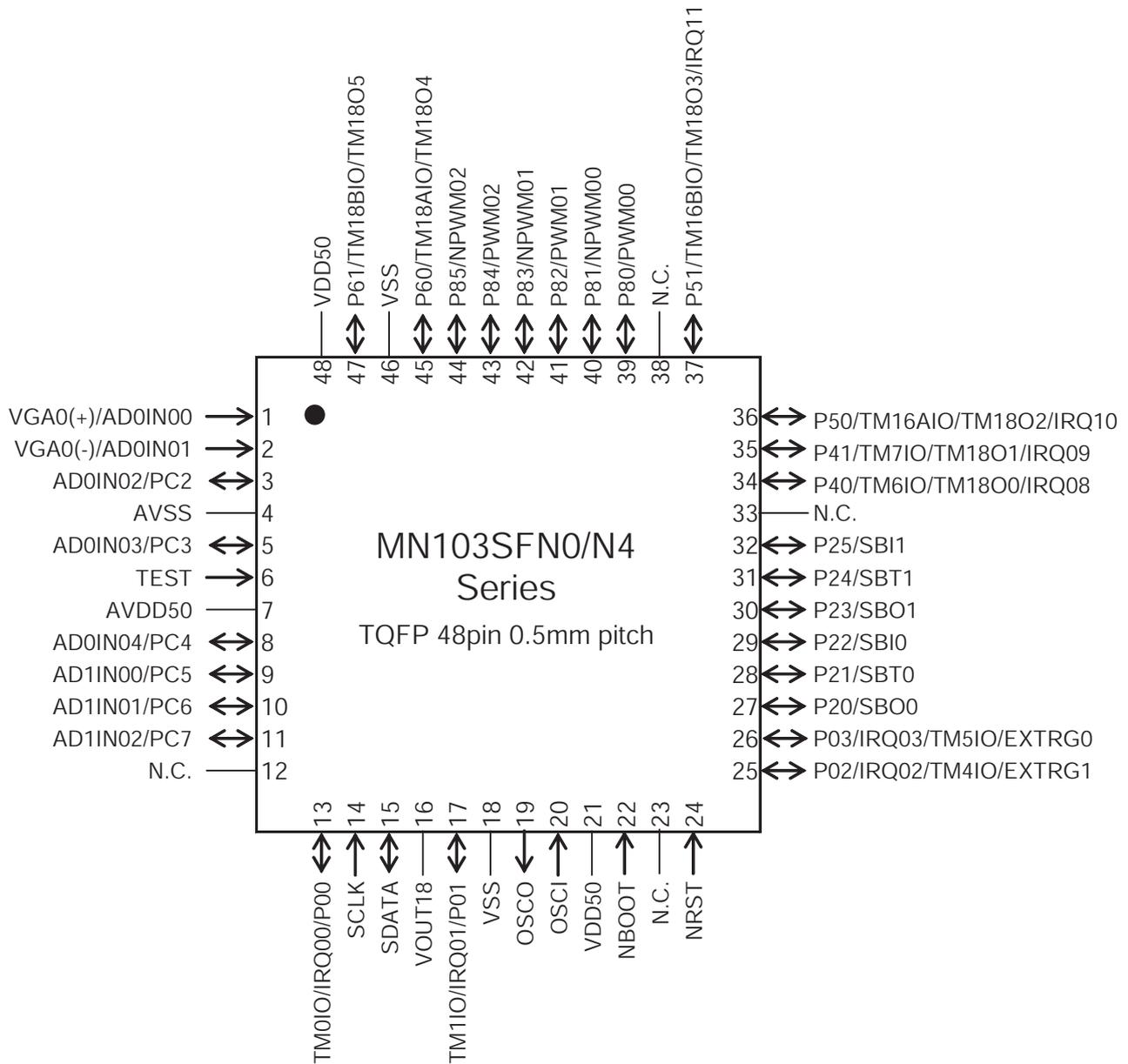■ Pin Description

• MN103SFJ7A (TQFP048-P-0707B)

Top pins (left to right, 48–37):
VDD50 (48), P61 (47), VSS (46), P60 (45), P85/NPWMO2 (44), P84/PWMO2 (43), P83/NPWMO1 (42), P82/PWMO1 (41), P81/NPWMO0 (40), P80/PWMO0 (39), N.C. (38), P51/TM16BIO (37)

Left pins (1–12):
AD0IN00 → 1
AD0IN01 → 2
AD0IN02/PC2 ↔ 3
AVSS — 4
AD0IN03/PC3 ↔ 5
TEST → 6
AVDD50 — 7
AD0IN04/PC4 ↔ 8
AD1IN00/PC5 ↔ 9
AD1IN01/PC6 ↔ 10
AD1IN02/PC7 ↔ 11
N.C. — 12

Center:
MN103SFJ7A
TQFP 48pin 0.5mm pitch

Right pins (36–25):
36 ↔ P50/TM16AIO
35 ↔ P41/TM7IO
34 ↔ P40/TM6IO
33 — N.C.
32 ↔ P25/SBI1
31 ↔ P24/SBT1
30 ↔ P23/SBO1
29 ↔ P22/SBI0
28 ↔ P21/SBT0
27 ↔ P20/SBO0
26 ↔ P03/IRQ03/TM5IO/EXTRG0
25 ↔ P02/IRQ02/TM4IO/EXTRG1

Bottom pins (13–24):
TM0IO/IRQ00/P00 (13), SCLK (14), SDATA (15), VOUT18 (16), TM1IO/IRQ01/P01 (17), VSS (18), OSCO (19), OSCI (20), VDD50 (21), NBOOT (22), N.C. (23), NRST (24)

■ Pin Description (continued)
  • MN103SFN0/N4 Series (QFP044-P-1010F)

* VGA is not in the MN103SFN0 series.
  1,2 pin of MN103SFN0 series are the dedicated input pin for A/D converter.

■ Pin Description (continued)
• MN103SFN0/N4 Series (TQFP048-P-0707B)

Top side pins (left to right, pins 48–37):
- 48 VDD50
- 47 P61/TM18BIO/TM18O5
- 46 VSS
- 45 P60/TM18AIO/TM18O4
- 44 P85/NPWM02
- 43 P84/PWM02
- 42 P83/NPWM01
- 41 P82/PWM01
- 40 P81/NPWM00
- 39 P80/PWM00
- 38 N.C.
- 37 P51/TM16BIO/TM18O3/IRQ11

Left side pins (top to bottom, pins 1–12):
- 1 VGA0(+)/AD0IN00
- 2 VGA0(-)/AD0IN01
- 3 AD0IN02/PC2
- 4 AVSS
- 5 AD0IN03/PC3
- 6 TEST
- 7 AVDD50
- 8 AD0IN04/PC4
- 9 AD1IN00/PC5
- 10 AD1IN01/PC6
- 11 AD1IN02/PC7
- 12 N.C.

Center label: MN103SFN0/N4 Series — TQFP 48pin 0.5mm pitch

Right side pins (top to bottom, pins 36–25):
- 36 P50/TM16AIO/TM18O2/IRQ10
- 35 P41/TM7IO/TM18O1/IRQ09
- 34 P40/TM6IO/TM18O0/IRQ08
- 33 N.C.
- 32 P25/SBI1
- 31 P24/SBT1
- 30 P23/SBO1
- 29 P22/SBI0
- 28 P21/SBT0
- 27 P20/SBO0
- 26 P03/IRQ03/TM5IO/EXTRG0
- 25 P02/IRQ02/TM4IO/EXTRG1

Bottom side pins (left to right, pins 13–24):
- 13 TM0IO/IRQ00/P00
- 14 SCLK
- 15 SDATA
- 16 VOUT18
- 17 TM1IO/IRQ01/P01
- 18 VSS
- 19 OSCO
- 20 OSCI
- 21 VDD50
- 22 NBOOT
- 23 N.C.
- 24 NRST

* VGA is not in the MN103SFN0 series.
  1,2 pin of MN103SFN0 series are the dedicated input pin for A/D converter.

■ Pin Description (continued)

• MN103SFN1/N5 Series (TQFP064-P-1010C)

MN103SFN1/N5 Series

TQFP 64pin 0.5mm pitch

Top pins (64–49):
- 64 VDD50
- 63 P61/TM18BIO/TM18O5
- 62 VSS
- 61 P60/TM18AIO/TM18O4
- 60 P95/NPWM12
- 59 P94/PWM12
- 58 P93/NPWM11
- 57 P92/PWM11
- 56 P91/NPWM10
- 55 P90/PWM10
- 54 P85/NPWM02
- 53 P84/PWM02
- 52 P83/NPWM01
- 51 P82/PWM01
- 50 P81/NPWM00
- 49 P80/PWM00

Left pins (1–16):
- TM19AIO/P64 ←→ 1
- TM19BIO/P65 ←→ 2
- * VGA0(+)/AD0IN00 → 3
- * VGA0(-)/AD0IN01 → 4
- AD0IN02/PC2 ←→ 5
- AVSS — 6
- AD0IN03/PC3 ←→ 7
- AVDD50 — 8
- AD0IN04/PC4 ←→ 9
- AD1IN00/PC5 ←→ 10
- AD1IN01/PC6 ←→ 11
- AD1IN02/PC7 ←→ 12
- * VGA1(+)/AD1IN03 → 13
- * VGA1(-)/AD1IN04 → 14
- AD1IN05/PD2 ←→ 15
- AD1IN06/PD3 ←→ 16

Right pins (48–33):
- 48 ←→ P51/TM16BIO/TM18O3
- 47 ←→ P50/TM16AIO/TM18O2
- 46 ←→ P47/TM11IO/IRQ05
- 45 ←→ P46/TM10IO/IRQ04
- 44 ←→ P43/TM3IO/IRQ11
- 43 ←→ P42/TM2IO/IRQ10
- 42 ←→ P41/TM7IO/TM18O1/IRQ09
- 41 ←→ P40/TM6IO/TM18O0/IRQ08
- 40 ←→ P33/SBCS2
- 39 ←→ P32/SBI2
- 38 ←→ P31/SBT2
- 37 ←→ P30/SBO2
- 36 ←→ P25/SBI1
- 35 ←→ P24/SBT1
- 34 ←→ P23/SBO1
- 33 ←→ P22/SBI0

Bottom pins (17–32):
- 17 TM0IO/IRQ00/P00
- 18 TM1IO/IRQ01/P01
- 19 EXTRG1/TM4IO/IRQ02/P02
- 20 EXTRG0/TM5IO/IRQ03/P03
- 21 SCLK
- 22 SDATA
- 23 VOUT18
- 24 TEST
- 25 VSS
- 26 OSCO
- 27 OSCI
- 28 VDD50
- 29 NBOOT
- 30 NRST
- 31 SBO0/P20
- 32 SBT0/P21

* VGA is not in the MN103SFN1 series.
  3,4,13,14 pin of MN103SFN1 series are the dedicated input pin for A/D converter.

■ Pin Description (continued)

• MN103SFN2/N6 Series (TQFP080-P-1212D)

MN103SFN2/N6 Series

TQFP 80pin 0.5mm pitch
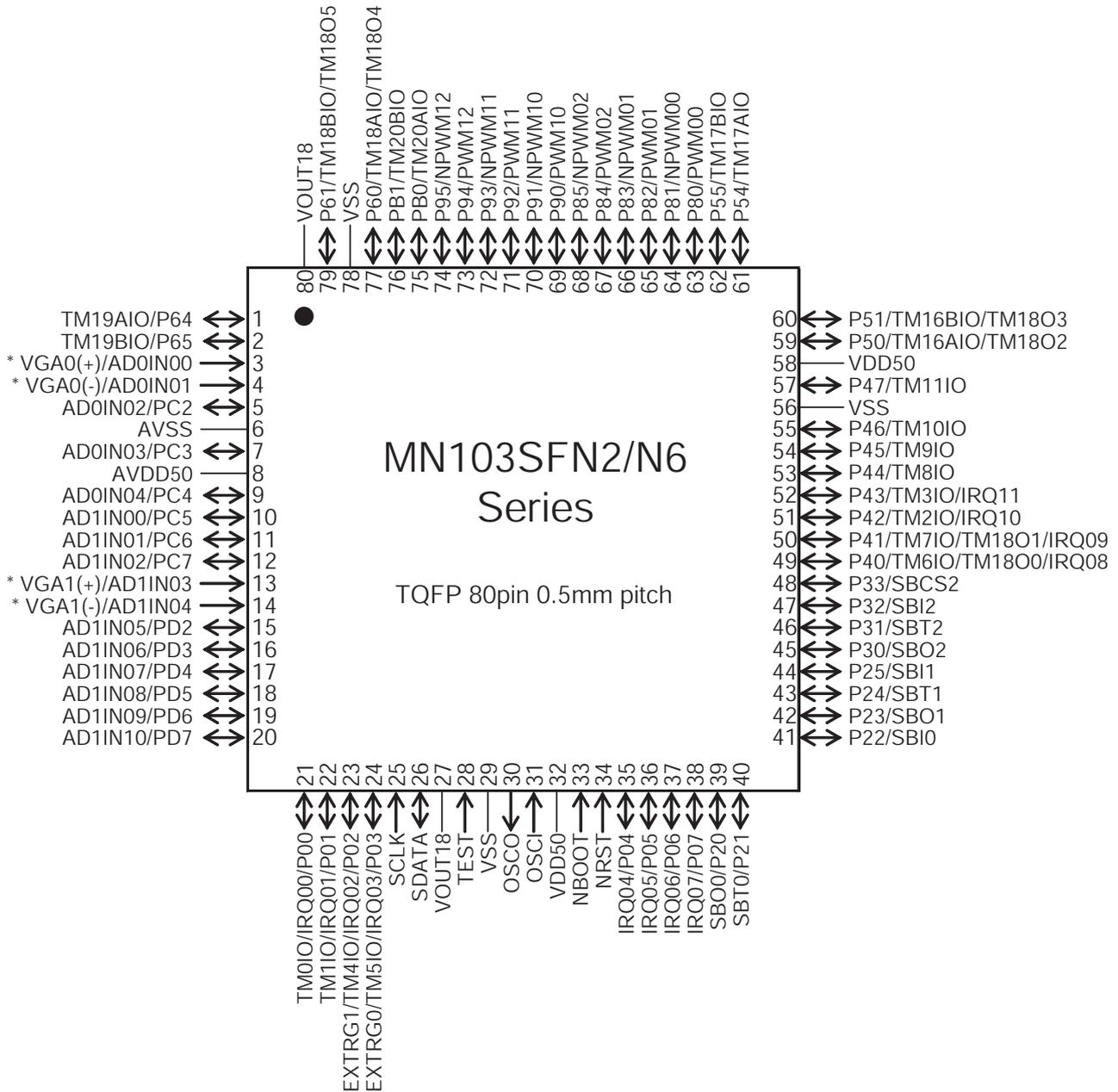
* VGA is not in the MN103SFN2 series.
3,4,13,14 pin of MN103SFN2 series are the dedicated input pin for A/D converter.