# MN103SL7 Series

# 32-bit Single-chip Microcontroller

#### Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.

This LSI series is well suited for in-vehicle electrical compressor control, in-vehicle body control, air conditioner, electrical power control and other applications.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, DMA controller, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors, arithmetic unit for speed-up of inverter control and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multifunctional system on LSI for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

# **Product Summary**

This datasheet describes the following model.

| Model      | ROM Size | RAM Size | Classification       | Package         |  |
|------------|----------|----------|----------------------|-----------------|--|
| MN103SFL7G | 128 KB   | 12 KB    | Flash EEPROM version | TQFP048-P-0707F |  |
| MN103SFL7K | 256 KB   | 12 KD    |                      |                 |  |

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#### Features

#### CPU core

MN103S core

4 GB of memory space (for instructions / data)

LOAD/STORE architecture with 5-stage pipeline

46 basic instructions + 23 extended arithmetic instructions

6 addressing modes

Instruction set of 1 byte in word length

Extended arithmetic unit incorporated (high-speed multiply/divide instructions)

Machine cycle: 16.7 ns (oscillation frequency: 10 MHz, 6 multiplying)

Operation mode: NORMAL mode, SLEEP mode, HALT mode, STOP mode

#### Oscillation Circuit

External high-speed oscillation (crystal/ceramic)

Internal high-speed oscillation (10 MHz)

Internal low-speed oscillation for Watchdog timer 2 (35 kHz)

#### Clock Multiplication Circuit

PLL output clock (IOCLK): High-speed oscillation is multiplied by 3 to 15

# Internal Memory

ROM 128 KB (MN103SFL7G), ROM 256 KB (MN103SFL7K)

RAM 12 KB

#### **DMA Controller**

Channel : 2 ch Transfer requests : 46 types

(External interrupts: 8, Timer: 17, Serial: 6, IIC: 3, A/D converter: 4, CAN: 1, LIN: 1, PWM: 4,

Power Voltage Detection: 1, Software: 1)

Transfer mode : 3 modes (One word transfer / Burst transfer / Intermittent transfer)

#### Features (continued)

#### Interrupts

Internal interrupts 48 interrupts :DWFKGRWLPHURHURZLQWHUUSWV

System error interrupts

Fail safe function interrupts

:DWFKGRWLPHURHURZORFNHUURUGHWHFWLRQ5HLVWHUSURWHFW

Power voltage detection interrupts

#### <Timer Interrupts>

7LPHUQGHURZLQWHUUSW

7LPHUQGHURZLQWHUUSW

7LPHQQGHURZLQWHUUSW

7LPHQGHURZLQWHUUSW

7LPHUQGHURZLQWHUUSW

7LPHUQGHURZLQWHUUSW

7LPHUQGHURZLQWHUUSW

7LPHUQGHURZLQWHUUSW

7LPHURHURZQGHURZLQWHUUSW

Timer 16 compare/capture A interrupt

Timer 16 compare/capture B interrupt

#### 7LPHURHURZQGHURZLQWHUUSW

Timer 18 compare/capture A interrupt

Timer 18 compare/capture B interrupt

# 7LPHURHURZQGHURZLQWHUUSW

Timer 19 compare/capture A interrupt

Timer 19 compare/capture B interrupt

#### <Serial interface>

Serial 0 UART reception completion interrupt

Serial 0 clock synchronous communication completion /UART transmission completion interrupt

Serial 0 transmission data buffer empty interrupt

Serial 1 UART reception completion interrupt

Serial 1 clock synchronous communication completion /UART transmission completion interrupt

Serial 1 transmission data buffer empty interrupt

IIC stop condition detection interrupt

IIC communication end interrupt

IIC transmission data buffer empty interrupt

LIN interrupt

CAN interrupt

#### <PWM>

#### 3:0RHURZLQWHUUSW

#### 3:0QGHURZLQWHUUSW

PWM0 synchronous A/D conversion start A interrupt

PWM0 synchronous A/D conversion start B interrupt

# <A/D>

A/D 0 conversion end interrupt

A/D 0 conversion end B interrupt

A/D 1 conversion end interrupt

A/D 1 conversion end B interrupt

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#### Features (continued)

Interrupts (continued)

<DMA>

DMA0 transfer end interrupt

DMA0 request after DMA transfer end interrupt

0WUDQVIHUUHTHVWRHURZLQWHUUSW

DMA1 transfer end interrupt

DMA1 request after DMA transfer end interrupt 0WUDQVIHUUHTHVWRHURZLQWHUUSW

External interrupts : 8 interrupts

External interrupt pins : From IRQ00 to IRQ07

Interrupt detection condition : Each edge, both edges, high-level and low-level detection

(DFKLQWHUUSWGHWHFWLRQFRQGLWLRQLVDEOHWROWHULQZLWKWKHQRLVHOWHU

**Timer Counter** 

8-bit timer 8 sets 16-bit timer 3 sets

Timer 0 (8-bit timer)

Interval timer, Timer pulse output, Event count, Baud rate timer RQWFORFNVRUFH \_2/\_2/\_2/70,2SLQLQSW7LPHUQGHURZ7LPHUQGHURZ

Timer 1 (8-bit timer)

Interval timer, Timer pulse output, Event count, Baud rate timer, Cascade connection RQWFORFNVRUFH \_2/\_2/\_2/\_20\_2SLQLQSW7LPHQQGHURZ7LPHQQGHURZ

Timer 2 (8-bit timer)

Interval timer, Baud rate timer, Cascade connection

RQWFORFNVRUFH \_2/\_2/\_2/TLPHUQGHURZ/LPHUQGHURZ

Timer 3 (8-bit timer)

Interval timer, Baud rate timer, Cascade connection

RQWFORFNVRUFH ,2/,2/,2/7LPHLQGHURZ/LPHLQGHURZ/LPHLQGHURZ

Timer 4 (8-bit timer)

Interval timer, Timer pulse output, Event count RQWFORFNVRUFH \_2/\_2/\_2/\_270,2SLQLQSW7LPHUQGHURZ7LPHUQGHURZ

Timer 5 (8-bit timer)

Interval timer, Timer pulse output, Event count, Cascade connection RQWFORFNVRUFH \_2/\_2/\_2/\_270,2SLQLQSW7LPHUQGHURZ7LPHUQGHURZ

Timer 6 (8-bit timer)

Interval timer, Timer pulse output, Event count, Cascade connection RQWFORFNVRUFH \_2/\_2/\_2/70,2SLQLQSW7LPHUQGHURZ/LPHUQGHURZ

Timer 7 (8-bit timer)

Interval timer, Timer pulse output, Event count, Cascade connection RQWFORFNVRUFH ,2/,2/,2/,2/70,2SLQLQSW7LPHUQGHURZ 7LPHUQGHURZ/LPHUQGHURZ

#### Features (continued)

#### Serial Interface

Serial 1 (Multi master IIC / Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Overrun error detection

7UDQVIHUFORFNVRUFHDQCRIWLPHUQGHURZ

DQCRIWLPHUQGHURZ DQCRIWLPHUQGHURZ DQCRIWLPHUQGHURZ

IOCLK/2, IOCLK/4, SBT1 pin

Transfer clock division value selection: Divided by 8, 16

#### DQEHVHOHFWHGDVWKHUVWELWWREHWUDQVIHUUHGWWUDQVIHUVLHIURPWRELWVFDQEHVHOHFWHG

Can be continuously transmitted, received or transmitted and received.

Maximum transfer rate: 5.0 Mbps

Full duplex UART

Parity check, Overrun and framing error detection

7UDQVIHUFORFNVRUFHDQCRIWLPHUQGHURZ

DQQRIWLPHQQGHURZ DQQRIWLPHQQGHURZ DQQRIWLPHQQGHURZ IOCLK/2, IOCLK/4

Transfer clock division value selection: Divided by 8, 16

#### DQEHVHOHFWHGDVWKHUVWELWWREHWUDQVIHUUHQWUDQVIHUVLHIURPWRELWVFDQEHVHOHFWHG

Continuous transmission, reception, and transmission/reception

Maximum transfer rate: 300 kbps

Multi master IIC

7, 10-bit slave address is settable

General call communication mode is supported

7UDQVIHUFORFNVRUFHDQQRIWLPHUQGHURZ

DQCRIWLPHLQGHURZ DQCRIWLPHLQGHURZ DQCRIWLPHLQGHURZ IOCLK/2, IOCLK/4

Transfer clock division value selection: Divided by 8

#### Power Supply Voltage Detection

Detection level 4.15 V r 0.25 V (At falling voltage)

4.25 V r 0.25 V (At rising voltage)

When power supply voltage become equal to detection level, interrupt is generated.

Auto Reset Circuit

Detection level 3.50 V r 0.20 V (At falling voltage)

3.65 V r 0.35 V (At rising voltage)

When power supply voltage is under detection level, reset is generated.

# **Clock Monitoring Function**

Frequency error of the external high-speed oscillation (include PLL output) can detect.

When the error is detected, reset is generated.

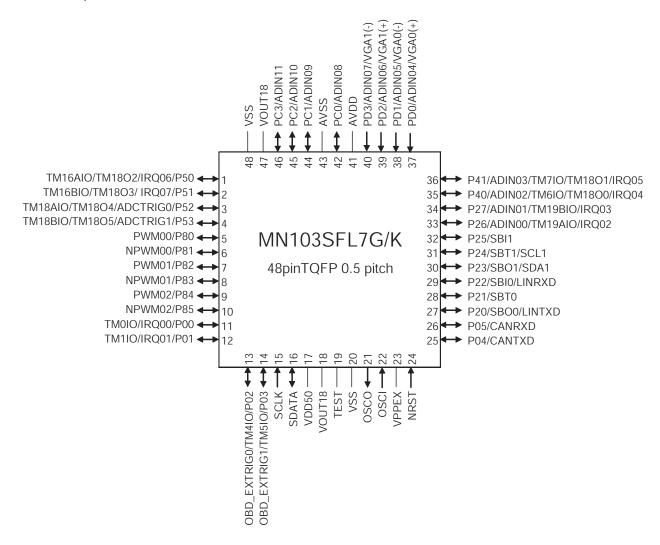
# Features (continued)

| ,                     |    |      |
|-----------------------|----|------|
| Port / pins           |    |      |
| I/O ports             | 30 | pins |
| Motor control output  | 6  | pins |
| External interrupt    | 8  | pins |
| A/D input             | 8  | pins |
| Input ports           | 4  | pins |
| VGA, A/D input        | 4  | pins |
| Special pins          | 14 | pins |
| Reset input pin       | 1  | pin  |
| Oscillation pin       | 2  | pins |
| Test mode input pin   | 2  | pins |
| Power pin             | 7  | pins |
| On-board debugger pin | 2  | pins |

#### Package Code name

TQFP48 (7 mm square, 0.5 mm pitch, halogen free) TQFP048-P-0707F

# Pin Description



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