

DATA SHEET

SKY13345-368LF: 0.1 to 3.5 GHz SP3T Switch

Applications

- 802.11 b/g WLANs
- Bluetooth®

Features

- Broadband frequency range: 0.1 to 3.5 GHz
- Low insertion loss: 0.5 dB @ 2.45 GHz
- High isolation: 32 dB up to 2.45 GHz
- No external DC blocking capacitors required
- Positive low voltage control: $V_{CTL} = 1.6$ to 3.3 V, $V_{DD} = 2.5$ to 5.5 V
- Small, QFN (12-pin, 2 x 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

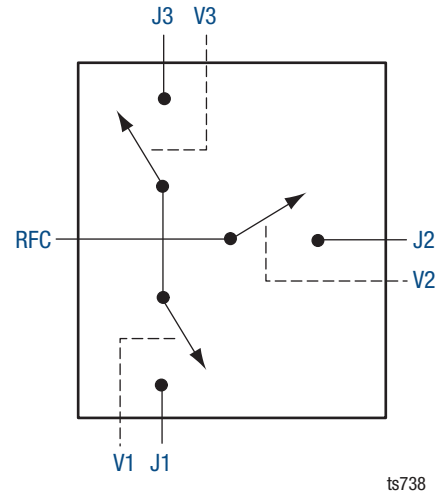


Figure 1. SKY13345-368LF Block Diagram



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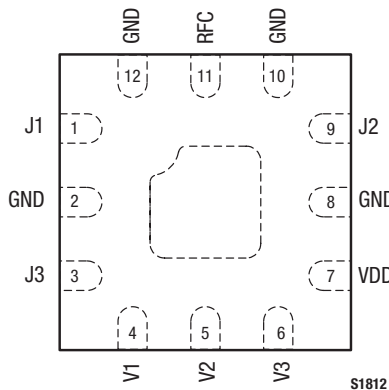


Figure 2. SKY13345-368LF Pinout – 12-Pin QFN (Top View)

Description

The SKY13345-368LF is a CMOS silicon-on-insulation (SOI), single-pole, triple-throw (SP3T) switch. The high linearity performance and low insertion loss makes the device an ideal choice for WLAN (802.11 b/g) and Bluetooth® applications in the 2.4 to 2.5 GHz frequency range.

The SKY13345-368LF SP3T switch is provided in a compact Quad Flat No-Lead (QFN) 2 x 2 mm package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Table 1. SKY13345-368LF Signal Descriptions (Note 1)

Pin	Name	Description	Pin	Name	Description
1	J1	RF port 1	7	VDD	DC power supply
2	GND	Ground	8	GND	Ground
3	J3	RF port 3	9	J2	RF port 2
4	V1	DC control voltage 1 (see Table 4)	10	GND	Ground
5	V2	DC control voltage 2 (see Table 4)	11	RFC	RF common (antenna) port
6	V3	DC control voltage 3 (see Table 4)	12	N/C	No connection (pin may be grounded)

Note 1: Exposed pad must be grounded.

Functional Description

The SKY13345-368LF includes an internal negative voltage generator and decoder that eliminate the need for external DC blocking capacitors on the RF ports. No external components are required for proper operation. DC decoupling capacitors may be added on the VDD and control lines if necessary.

Switching is controlled by three control voltage inputs: V1, V2, and V3. Depending on the logic voltage level applied to the control pins, the RFC (RF common) pin is connected to one of three switched RF outputs (J1, J2, or J3) through a low insertion path, while the path between the RFC pin and the other RF pins is in a high isolation state. There is a fourth switching state that enables J2 and J3 at the same time. The output power measured at J2 and J3 in this state is 3 dB less than the insertion loss.

For proper switching operation, the SKY13345-368LF must be set to a state for a minimum of 10 μs before changing to a different state. A typical switching diagram is shown in Figure 3.

Shutdown mode is enabled by connecting all control pins to logic low. This mode reduces the overall current consumption of the

device to 5 μA, typical. To prevent the switch from accidentally entering shutdown mode during switching, caution must be taken to avoid having all three control signals (V1, V2, and V3) set to logic low for more than 500 ns. When exiting shutdown mode, the switch has a 25 μs startup time before switching occurs.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13345-368LF are provided in Table 2. Electrical specifications are provided in Table 3.

The state of the SKY13345-368LF is determined by the logic provided in Table 4.

Typical performance characteristics of the SKY13345-368LF are illustrated in Figures 4 through 7.

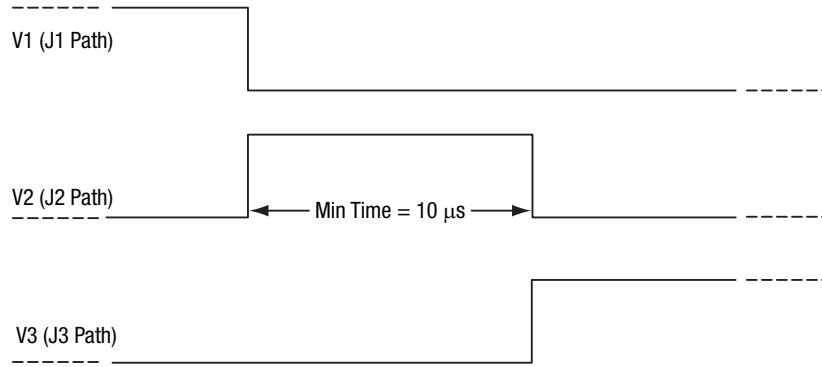
Table 2. SKY13345-368LF Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage (VDD)	V _{DD}	2.5	5.5	V
Control voltage (V1, V2, V3) (Note 2)	V _{CTL}	1.6	3.3	V
Input power	P _{IN}		+35	dBm
Storage temperature	T _{STG}	-40	+125	°C
Operating temperature	T _{OP}	-40	+85	°C

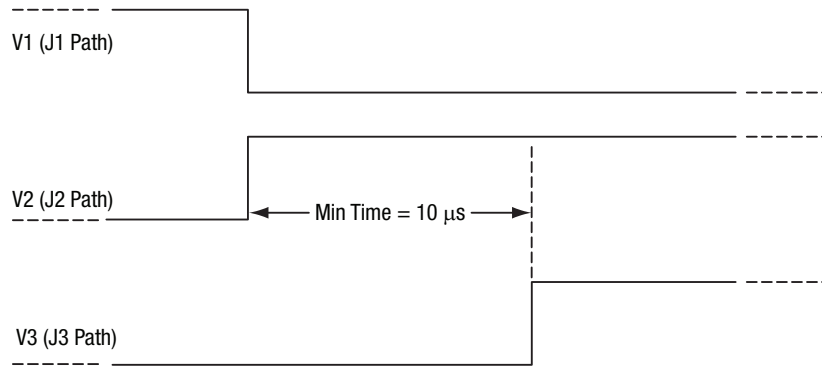
Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Note 2: Any bias voltage applied to the V1, V2, or V3 pins may damage the device if there is no bias voltage also present on the VDD pin.

CAUTION: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

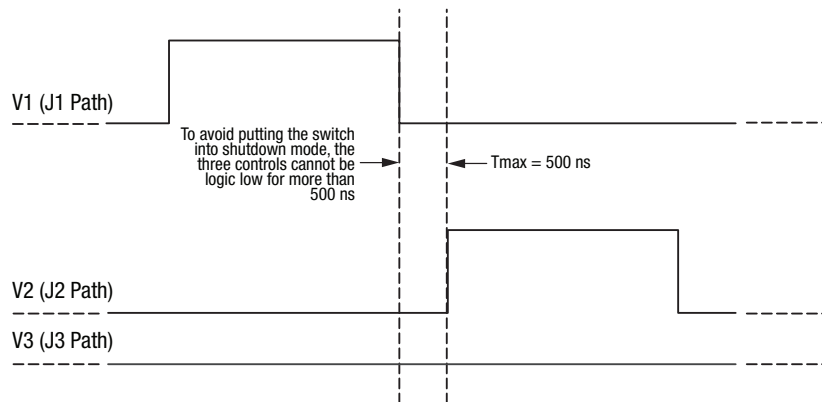


One Arm "On"



Two Arms "On"

To Avoid Shutdown
 $V1 = V2 = V3 = 0 < 500 \text{ ns}$



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Figure 3. Typical Switching Diagram

Table 3. SKY13345-368LF Electrical Specifications (1 of 2) (Note 1)

(V_{DD} = 2.5 V to 5.5 V, V_{CTL} = 0 V (Low), V_{CTL} = 1.8 V (High), T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z₀] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Insertion loss	IL	f = 1 GHz, RFC-J1, RFC-J2		0.40	0.50	dB
		f = 1 GHz, RFC-J3		0.45	0.50	dB
Insertion loss	IL	f = 2 GHz, RFC-J1, RFC-J2		0.40	0.50	dB
		f = 2 GHz, RFC-J3		0.50	0.55	dB
Insertion loss	IL	f = 2.4 to 2.5 GHz, RFC-J1, RFC-J2		0.40	0.55	dB
		f = 2.4 to 2.5 GHz, RFC-J3		0.55	0.65	dB
Isolation	Iso	f = 1 GHz, RFC-J1, RFC-J2, RFC-J3	40	43		dB
Isolation	Iso	f = 2 GHz, RFC-J1, RFC-J2, RFC-J3	34	37		dB
Isolation	Iso	f = 2.4 to 2.5 GHz, RFC-J1, RFC-J2, RFC-J3	32	35		dB
Return loss	IS11I	f = 2.45 GHz	18	20		dB
Third order input intercept point	IIP3	f = 2.45 GHz, ΔF = 1 MHz, P _{IN} = +20 dBm/tone	+55	+57		dBm
Input 0.1 dB compression point	P0.1dB	f = 2.45 GHz				
		RFC to J1 and J2 RFC to J3		+34 +27		dBm dBm
2 nd harmonic	2fo	f = 2.45 GHz, P _{IN} = +20 dBm		+75		dBc
3 rd harmonic	3fo	f = 2.45 GHz, P _{IN} = +20 dBm		+75		dBc
Error vector magnitude, WLAN	EVM _{WLAN}	P _{IN} for 2.5% error, WLAN 2.45 GHz, 802.11g, OFDM, 54 Mbps, 64 QAM		+27		dBm
Switching rise time		10/90% RF		180	200	ns
Switching fall time		90/10% RF		110	130	ns
Switching on time		50% V _{CTL} to 10/90% RF		220	250	ns
Switching off time		50% V _{CTL} to 90/10% RF		190	210	ns
Logic dwell time (Note 2)		T _{OP} = -40 °C to +85 °C	10	12		μs
Startup time (Note 3)		Shutdown state to any RF switch state		20	25	μs

Table 3. SKY13345-368LF Electrical Specifications (2 of 2) (Note 1)

($V_{DD} = 2.5\text{ V to }5.5\text{ V}$, $V_{CTL} = 0\text{ V (Low)}$, $V_{CTL} = 1.8\text{ V (High)}$, $T_{OP} = +25\text{ }^{\circ}\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\ \Omega$, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
DC Specifications						
Control voltage:						
High	V_{CTL_HIGH}		1.6		3.3	V
Low	V_{CTL_LOW}		0	1.8	0.4	V
Supply voltage	V_{DD}		2.5		5.5	V
Supply current	I_{DD}	$V_{DD} = 3.5\text{ V}$		30		μA
Control current	I_{ctl}	$V1 = V2 = V3 = 1.8\text{ V}$		2		μA
Shutdown mode supply current	I_{off}	$V_{DD} = 3.5\text{ V}$, $V1 = V2 = V3 = 0\text{ V}$		5		μA

Note 1: Performance is guaranteed only under the conditions listed in this table.

Note 2: Dwell time refers to the amount of time the switch is required to stay in any one state before switching to another state. Refer to the Functional Description section for more information.

Note 3: Startup time refers to the amount of time it takes for the switch to be fully operational when coming out of shutdown mode ($V1 = V2 = V3 = \text{logic } 0$).

Table 4. SKY13345-368LF Truth Table

V1 (Pin 4)	V2 (Pin 5)	V3 (Pin 6)	State
0	0	0	Shutdown
1	0	0	RFC to J1
0	1	0	RFC to J2
0	0	1	RFC to J3
0	1	1	RFC to J2 and J3

Note: 1 = 1.6 to 3.3 V

0 = 0 to 0.4 V

Any state other than described in this table places the switch into an undefined state.

Typical Performance Characteristics

($V_{DD} = 2.5\text{ V to }5.5\text{ V}$, $V_{CTL} = 0\text{ V (Low)}$, $V_{CTL} = 1.8\text{ V (High)}$, $T_{OP} = +25\text{ }^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\ \Omega$, Unless Otherwise Noted)

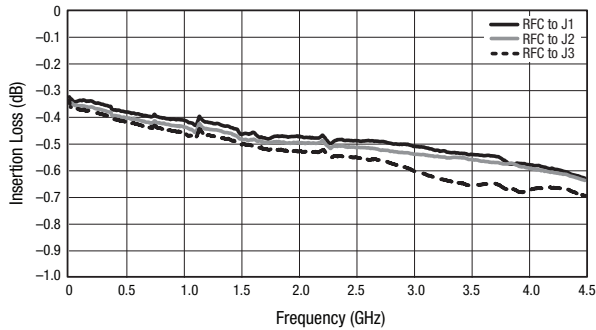


Figure 4. Typical Insertion Loss vs Frequency

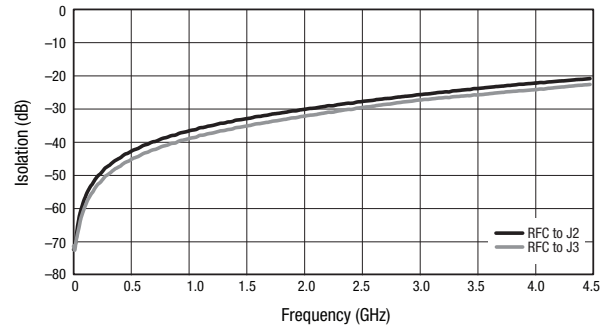


Figure 5. Typical Isolation vs Frequency (RFC to J1 Insertion Loss State)

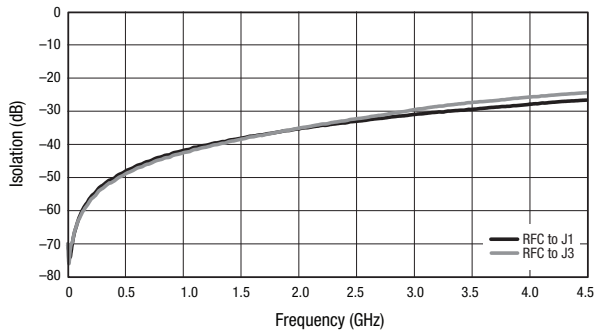


Figure 6. Typical Isolation vs Frequency (RFC to J2 Insertion Loss State)

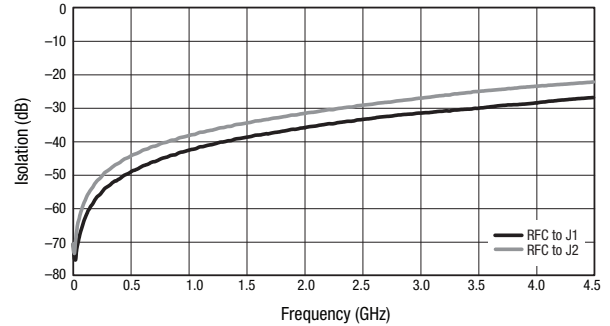


Figure 7. Typical Isolation vs Frequency (RFC to J3 Insertion Loss State)

Evaluation Board Description

The SKY13345-368LF Evaluation Board is used to test the performance of the SKY13345-368LF SP3T Switch. The board is made from a two-layer construction with ½ oz. copper cladding on top and bottom. The first layer material is 12-mil Rogers 4003C. The second layer material is 49-mil of FR4 for a total board thickness of about 62 mils. The impedance of all RF traces is 50 Ω.

An Evaluation Board schematic diagram is provided in Figure 8. An assembly drawing for the Evaluation Board is shown in Figure 9.

Package Dimensions

The PCB layout footprint for the SKY13345-368LF is provided in Figure 10. Typical part markings are shown in Figure 11. Package dimensions for the 12-pin QFN are shown in Figure 12, and tape and reel dimensions are provided in Figure 13.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13345-368LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

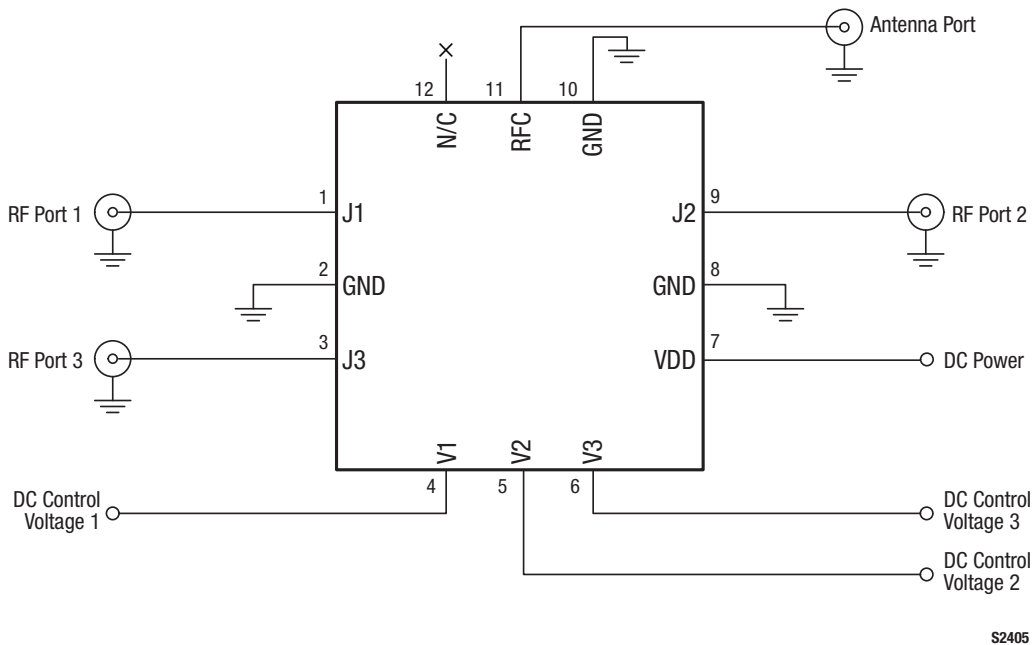
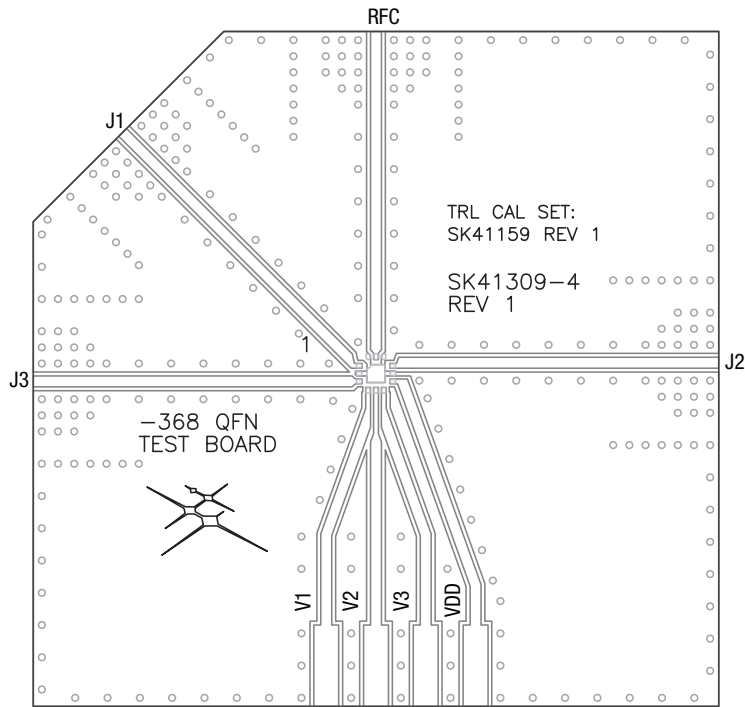
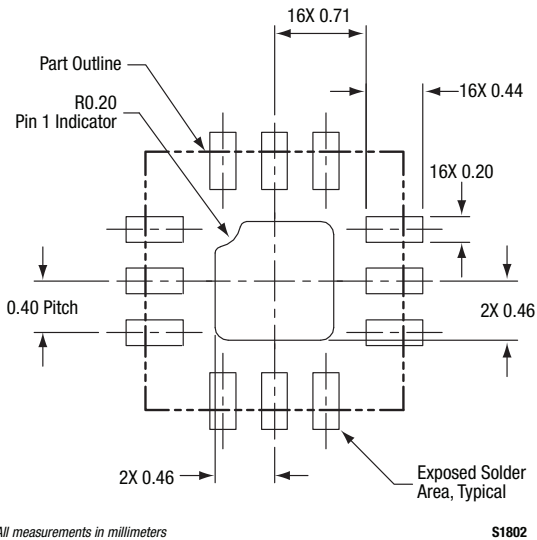


Figure 8. SKY13345-368LF Evaluation Board Schematic



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Figure 9. SKY13345-368LF Evaluation Board Assembly Diagram



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Figure 10. SKY13345-368LF PCB Layout Footprint (Top View)

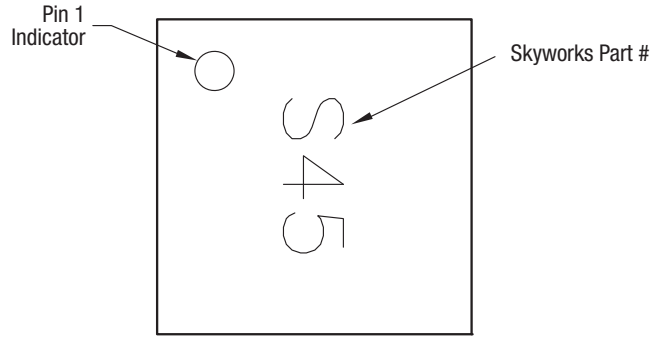
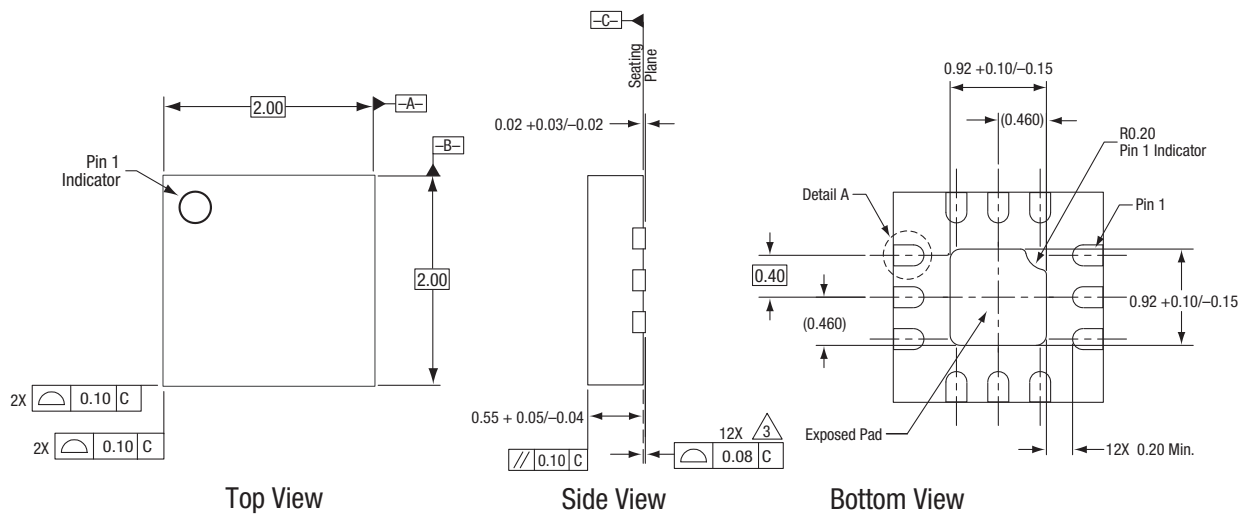
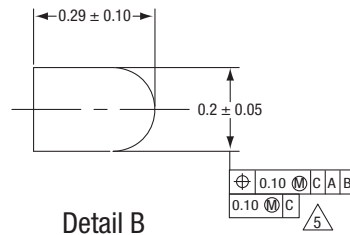


Figure 11. Typical Part Markings (Top View)



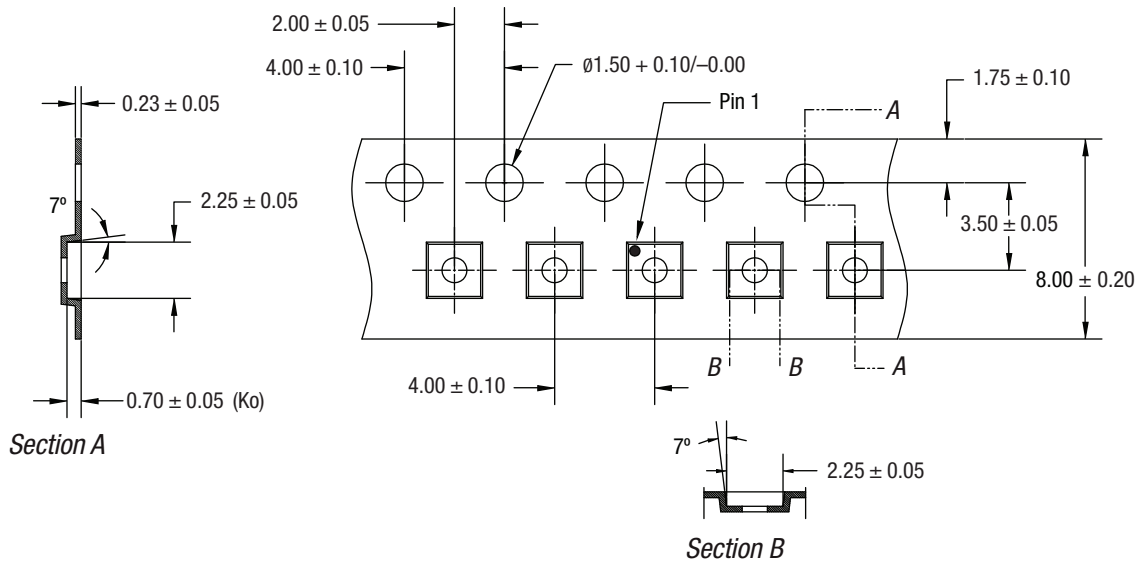
Notes:

1. All measurements are in millimeters.
2. Dimensions and tolerances according to ASME Y14.5M-1994.
3. Coplanarity applies to the terminals and all other bottom surface metallization.
4. Plating requirement per source control drawing (SCD) 2504.
5. Dimension applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.



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Figure 12. SKY13345-368LF 12-Pin QFN Package Dimensions



Notes:

1. Carrier tape must meet all requirements of Skyworks GP01-D232 procurement spec for tape and reel shipping.
2. Carrier tape shall be black conductive polycarbonate bakeable material at 125 °C temperature.
3. Cover tape shall be transparent conductive with 5.40 mm width.
4. ESD-surface resistivity must meet all ESD requirements of Skyworks specified on GP01-D232.
5. All measurements are in millimeters.

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Figure 13. SKY13345-368LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13345-368LF SP3T Switch	SKY13345-368LF	SKY13345-368LF-EVB

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