NAND Flash Drive

--- THNIDxxxxBx Series ---

Outline

The THNIDxxxxBx NAND Flash Drive series from Toshiba features an IDE interface, a flash disk controller chip, and NAND-type flash memory devices. There are two form factors, 2.5 inch-type and 3.5 inch-type, available in the series. The THNIDxxxxBx is available in 16 MB, 32 MB, 64 MB, 128 MB, 192 MB, 256 MB, 320 MB, 384 MB, 512 MB, 640 MB, 1024 MB, 1536 MB and 2048 MB capacities in each type. The drives operate with a 5-volts power supply and support Mode 4 PIO data transfer.

The NAND Flash Drive is geared specifically to the industrial market for use in ATM, factory automation machine, POS terminal, measuring product, ticket-vending machine, parking system and other industrial products that require high tolerance to environmental condition.

Features

- Capacity
  16MB up to 2GB
- Form factor
  2.5 inch-type, 3.5 inch-type, (HDD compatible)
- IDE interface
  Mode4 PIO
  ATA command set compatible
- Power supply
  V_{CC} = 5.0 V ± 10%
- Operating temperature
  –40°C~85°C (Industrial grade : THNIDxxxxBxI)
  0°C~70°C (Commercial grade : THNIDxxxxBx)
- Performance

Burst data transfer rate (Drive-Host)	16.6 MB/sec. (max)
Sustained write speed	3.2 MB/sec. (max)
Sustained read speed	6.5 MB/sec. (max)
Shock	9800 m/s^2 (max) [Non-operating]
Vibration	147 m/s^2 peak (25~2000 Hz) [Operating]

Product Models

2.5 inch-type

Unformatted	Cylinder	Head	Sector	Model No.
16 MB	248	4	32	THNID016MBA/BAI
32 MB	496	4	32	THNID032MBA/BAI
64 MB	978	4	32	THNID064MBA/BAI
128 MB	978	8	32	THNID128MBA/BAI
192 MB	733	16	32	THNID192MBA/BAI
256 MB	978	16	32	THNID256MBA/BAI
320 MB	814	16	48	THNID320MBA/BAI
384 MB	977	16	48	THNID384MBA/BAI
512 MB	993	16	63	THNID512MBA/BAI
640 MB	1241	16	63	THNID640MBA/BAI
1024 MB	1985	16	63	THNID1G02BA/BAI
1536 MB	2966	16	63	THNID1G53BA/BAI
2048 MB	3954	16	63	THNID2G04BA/BAI

3.5 inch-type

Unformatted	Cylinder	Head	Sector	Model No.
16 MB	248	4	32	THNID016MBB/BBI
32 MB	496	4	32	THNID032MBB/BBI
64 MB	978	4	32	THNID064MBB/BBI
128 MB	978	8	32	THNID128MBB/BBI
192 MB	733	16	32	THNID192MBB/BBI
256 MB	978	16	32	THNID256MBB/BBI
320 MB	814	16	48	THNID320MBB/BBI
384 MB	977	16	48	THNID384MBB/BBI
512 MB	993	16	63	THNID512MBB/BBI
640 MB	1241	16	63	THNID640MBB/BBI
1024 MB	1985	16	63	THNID1G02BB/BBI
1536 MB	2966	16	63	THNID1G53BB/BBI
2048 MB	3954	16	63	THNID2G04BB/BBI

Product Specification

- Storage Capacities:
  16, 32, 64, 128, 192, 256, 320, 384, 512, 640, 1024, 1536, 2048 Mbytes (unformatted)
- Performance:

To/from host	16.6 Mbytes/sec. (max theoretical)
Sustained write	3.2 Mbyte/sec. (max) [ATA PIO mode 4] (≥64 MB)
	1.5 Mbyte/sec. (max) [ATA PIO mode 4] (16 MB~32 MB)
Sustained read	6.5 Mbyte/sec. (max) [ATA PIO mode 4]

- Operating Voltage:
  5V +/– 10%
- Power Consumption:

Read mode	51 mA (typ)
Write mode	43 mA (typ)
Idle mode	16 mA (typ)
Sleep mode	1 mA (typ) (≤64 MB)
	3 mA (typ) (2 GB)

- Environmental Specification:

Operating temperature	–40°C to 85°C (Industrial grade : THNIDxxxxBxI)
	0°C to 70°C (Commercial grade : THNIDxxxxBx)
Storage temperature	–40°C to 85°C (Industrial grade : THNIDxxxxBxI)
	–20°C to 85°C (Commercial grade : THNIDxxxxBx)
Humidity	95% (max) [No condensation]
Shock	9800 m/s^2 (max) (3 axis) [No-operating]
Vibration	147 m/s^2 peak (25Hz~2000Hz) [Operating]

- Reliability:

Error rate	<1 bit/10^{15} bit read
ECC	1 bit error connection

Mechanical Specification

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	−0.6 to 6.0	V
V_{IN}	Input Voltage	−0.3 to V_{CC} + 0.3	V
T_{STG}	Storage Temperature	−40 to 85 (Industrial grade) 0 to 70 (Commercial grade)	°C
T_{OPR}	Operating Temperature	−40 to 85 (Industrial grade) −20 to 85 (Commercial grade)	°C

Recommended DC Operating Conditions

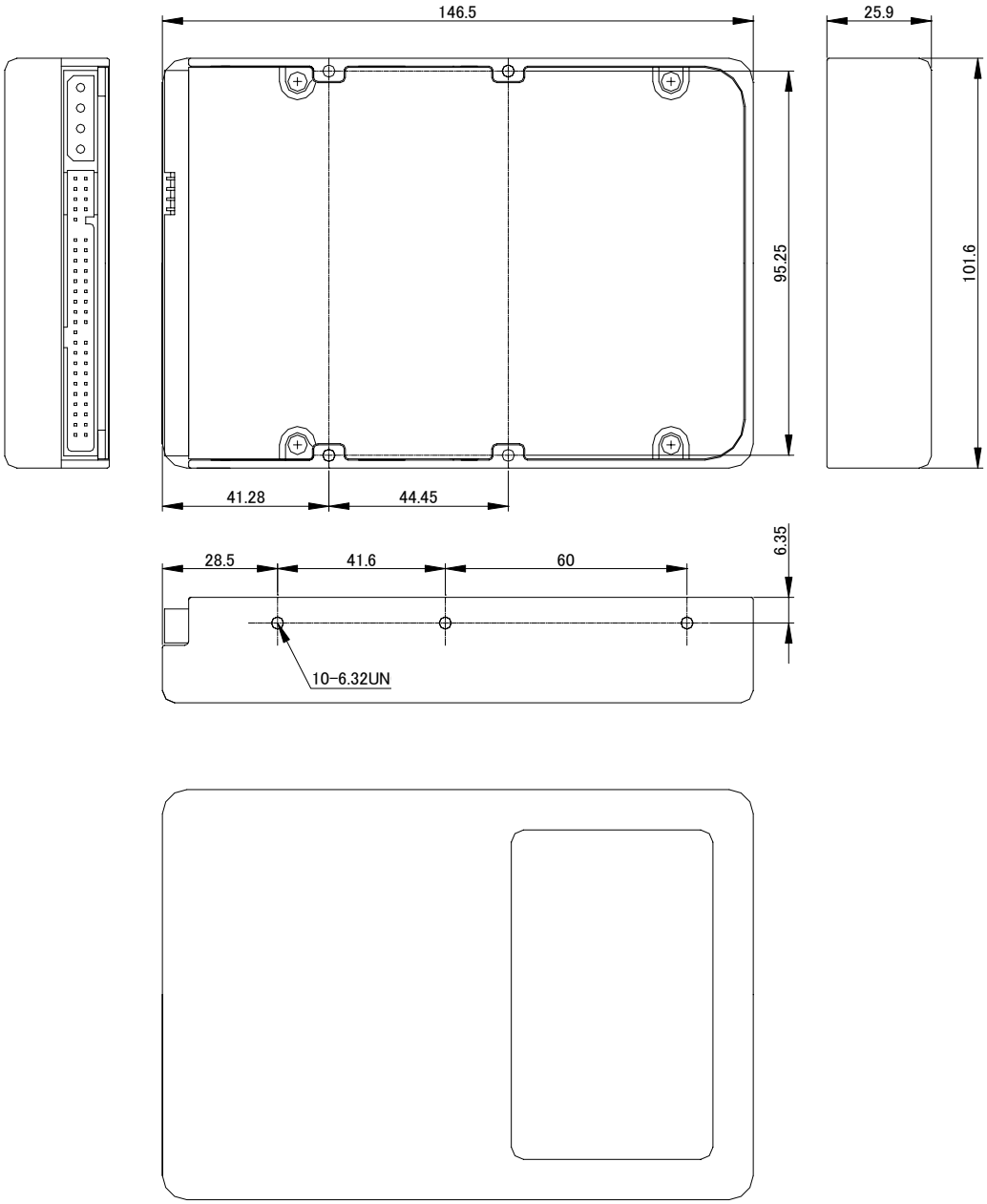
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	High Level Input Voltage	2.0	—		V
V_{IL}	Low Level Input Voltage		—	0.8	V

DC Characteristics (Ta = −40°C to 85°C, V_{CC} = 5.0 V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
I_{CCR}	Operating Current (Read)		51		mA
I_{CCW}	Operating Current (Write)		43		mA
I_{CCS}	Sleep Mode Current (≦ 64 MB)		1		mA
	Sleep Mode Current (2 GB)		3		mA
V_{OH}	High Level Output Voltage	V_{CC} −0.8	—	—	V
V_{OL}	Low Level Output Voltage	—	—	0.4	V

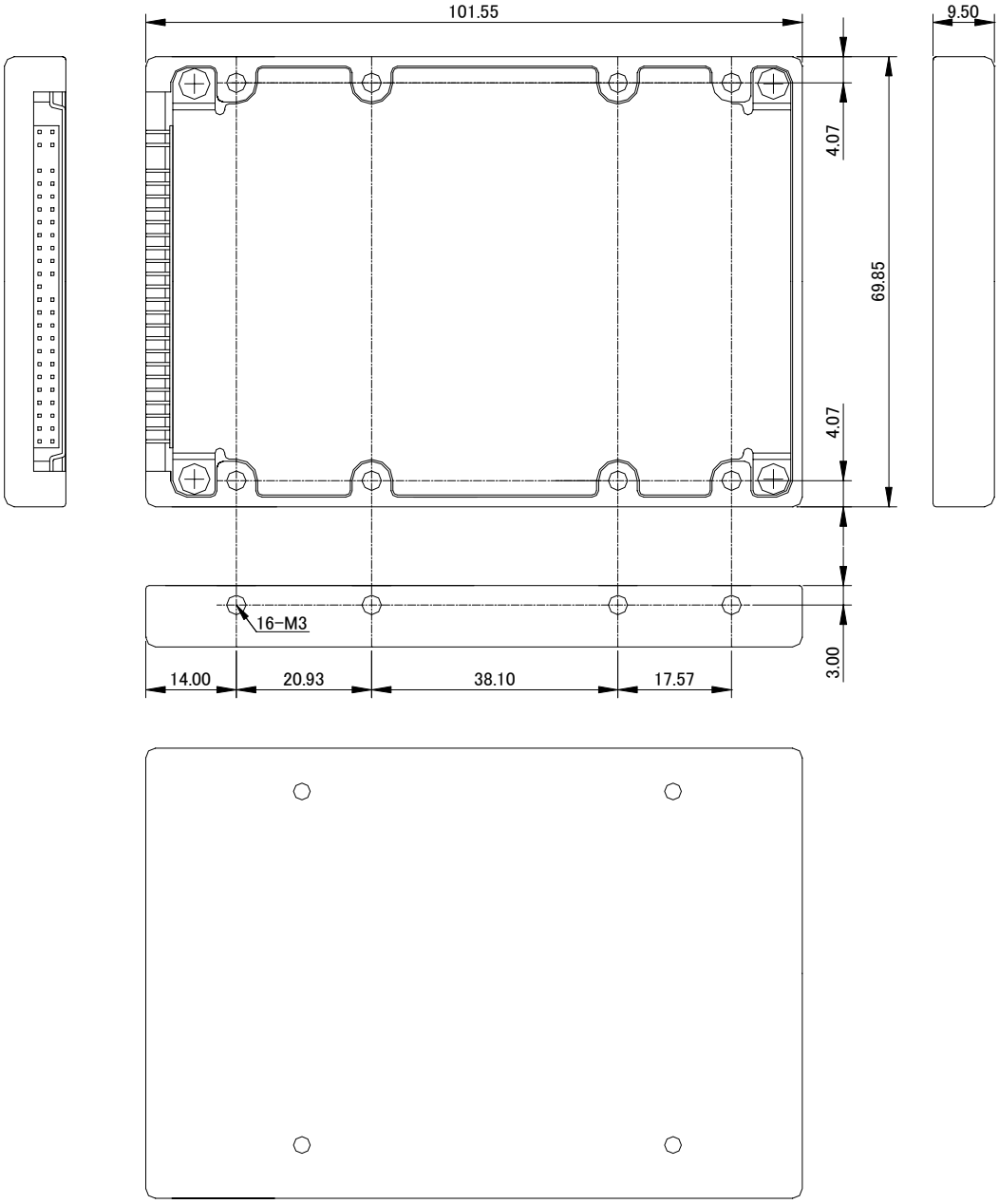
Package Dimensions

3.5 inch



3.5 inch Flash Drive Dimensions

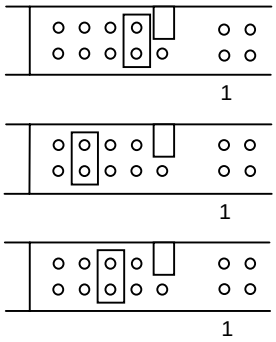
2.5 inch



2.5 Flash Drive Dimensions

Jumper Settings

3.5 inch

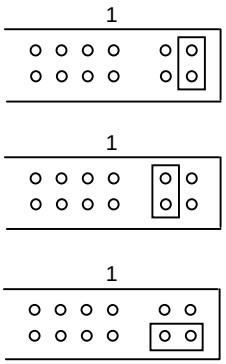


Master

Slave

Cable Select

2.5 inch



Master

Slave

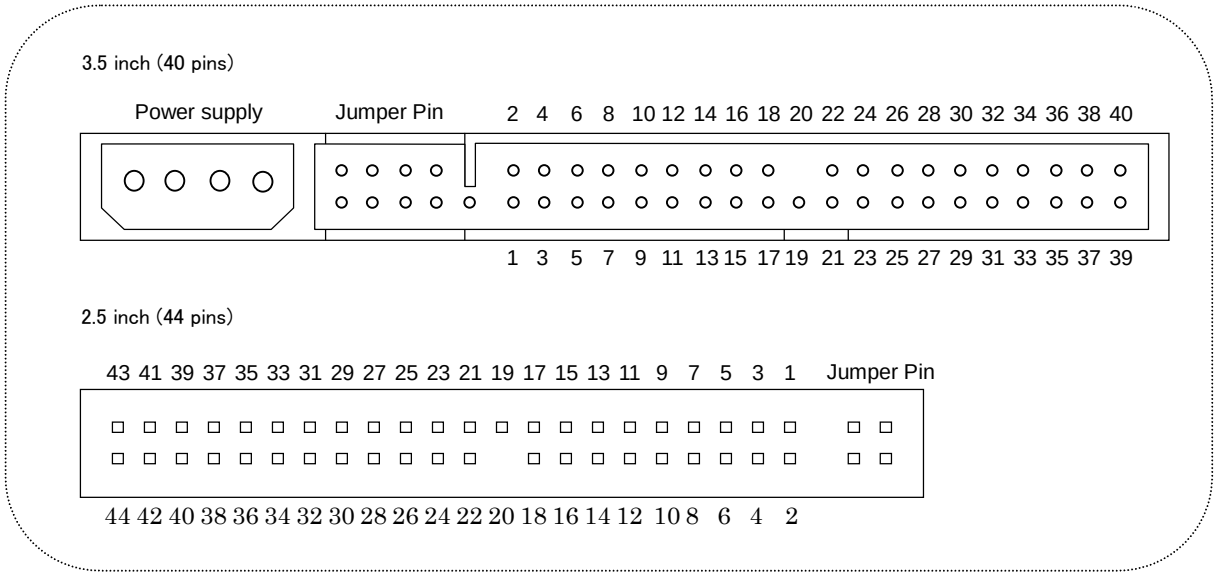
Cable Select

Pin Assignments and Pin Type

Pin Number	Signal Name	Pin Type
1	$\overline{\text{RESET}}$	I
3	DD7	I/O
5	DD6	I/O
7	DD5	I/O
9	DD4	I/O
11	DD3	I/O
13	DD2	I/O
15	DD1	I/O
17	DD0	I/O
19	GND	—
21	DMARQ(NC)	—
23	$\overline{\text{DIOW}}$	I
25	$\overline{\text{DIOR}}$	I
27	Reserved	O
29	$\overline{\text{DMACK}}$ (NC)	—
31	INTRQ	O
33	DA1	I
35	DA0	I
37	$\overline{\text{CS0}}$	I
39	$\overline{\text{DASP}}$	I/O
41	VCC	—
43	GND	—

Pin Number	Signal Name	Pin Type
2	GND	—
4	DD8	I/O
6	DD9	I/O
8	DD10	I/O
10	DD11	I/O
12	DD12	I/O
14	DD13	I/O
16	DD14	I/O
18	DD15	I/O
20	KEY(NC)	—
22	GND	—
24	GND	—
26	GND	—
28	CSEL	I
30	GND	—
32	Reserved	—
34	$\overline{\text{PDIAG}}$	I/O
36	DA2	I
38	$\overline{\text{CS1}}$	I
40	GND	—
42	VCC	—
44	—	—

Note 1: Pins #41 to 44 are for the IDE 44-pin standard (2.5 inch-type).
Note 2: To avoid damage to the drive or its pins, be sure to connect the drive to the IDE connecter properly
Note 3: "I" is defined as a direction from the host to the drive.
"O" is defined as a direction from the drive to the host.



Signal Description

Signal Name	Dir.	Pin	Description
$\overline{\text{RESET}}$	I	1	This pin is shall be used by host to reset the device. Reset signal is from the host and it is active low.
DD[0:15]	I/O	3 to 18	These lines carry Data, Commands and Status information between the host and controller. DD[0] is the LSB and DD[15] is the MSB.
$\overline{\text{DIOW}}$	I	23	DIOW is the strobe signal asserted by the host to write the device register.
$\overline{\text{DIOR}}$	I	25	DIOR is the strobe signal asserted by the host to read the device register
INTRQ	O	31	This signal is used by the selected device to interrupt the host system when interrupt pending is set. When the nIEN bit is cleared to zero and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is set to one or the device is not selected, the INTRQ signal shall be released.
DA[0: 2]	I	33, 35, 36	DA[2:0] are used to select one of eight registers
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	I	37, 38	$\overline{\text{CS0}}$ is used to select the Command Block registers while $\overline{\text{CS1}}$ is used to select the Control Block Register.
CSEL	I	28	CSEL is used to select Master/Slave mode, Low for Master, High for Slave mode.
$\overline{\text{PDIAG}}$	I/O	34	This bi-directional open drain signal is asserted by the slave after an Execute Diagnostic command to indicate to the master it has passed its diagnostics.
$\overline{\text{DASP}}$	I/O	39	This open drain output is asserted low any time the drive is active. In a Master/Slave configuration, this signal is used for the slave to inform the master that a slave drive is present.
GND		2, 19, 22, 24, 26, 30, 40, 43	Ground
VCC		41, 42	Power

I/O Register Specifications

The data is transferred between the host system and the device via I/O registers in the device.
Reads and writes to the registers are performed using the following logics.

Read I/O Register Function

Mode	$\overline{CS1}$	$\overline{CS0}$	DA0~DA2	$\overline{DIOR}$	$\overline{DIOW}$	DD8~DD15	DD0~DD7
Invalid mode	L	L	×	×	×	High-Z	High-Z
Standby mode	H	H	×	×	×	High-Z	High-Z
Data register access	H	L	0	L	H	odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	status out
Other command block register access	H	L	1~7H	L	H	High-Z	data

Note: ×: L or H

Write I/O Register Function

Mode	$\overline{CS1}$	$\overline{CS0}$	DA0~DA2	$\overline{DIOR}$	$\overline{DIOW}$	DD8~DD15	DD0~DD7
Invalid mode	L	L	×	×	×	don't care	don't care
Standby mode	H	H	×	×	×	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control in
Other command block register access	H	L	1~7H	H	L	don't care	data

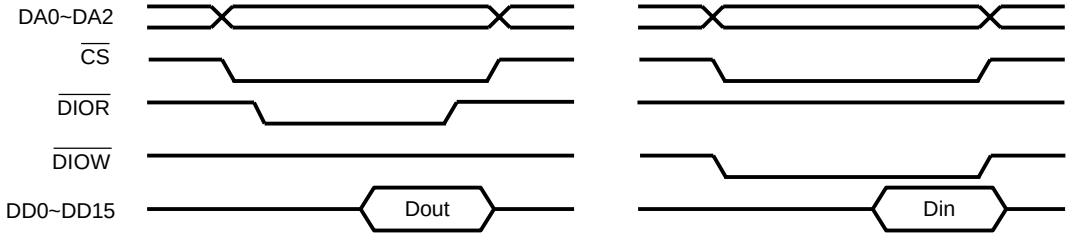
Note: x: L or H

I/O Register Address

This table summarizes the register selected by DA0~DA2.

$\overline{CS1}$	$\overline{CS0}$	DA2	DA1	DA0	$\overline{DIOR}$ = L	$\overline{DIOW}$ = L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Device/Head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

Register Access Timing Example



read cycle write cycle

1. Data register: This register is a 16-bit register that has read/write capability. is used for transferring 1 sector of data between the drive and the host.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DD0~DD15															

2. Error register: This register is read-only. It contains info on errors that occur when the drive is being accessed. This register is valid when the BSY bit in Status register and Alternate Status register are set to ”0”

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBK	UNC	“0”	IDNF	“0”	ABRT	“0”	AMNF

Bit	Name	Function
7	BBK (Bad Block detected)	This bit is set when a Bad Block is detected.
6	UNC (Data ECC error)	This bit is set when an uncorrectable error has occurred when reading the drive.
4	IDNF (ID Not Found)	This bit is set when the requested sector is in error or cannot be found.
2	ABRT (ABoRTed command)	This bit is set if the command has been aborted because of the drive status condition.（Not ready, Write fault, Invalid command）
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

3. Feature register: This register is write-only. It provides information regarding features of the drive that the host wishes to utilize.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Feature byte							

4. Sector count register: This register contains the number of sectors of data requested to be transferred via a read or write operation between the host and the drive. If the value of this register is zero, a count of 256 sectors is specified.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sector count byte							

5. Sector number register: This register contains the starting sector number, which is started by following sector transfer command.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sector number byte							

6. Cylinder low register: This register contains the low 8-bits of the starting cylinder address, which is started by following sector transfer command.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Cylinder low byte							

7. Cylinder high register: This register contains the high 8-bits of the starting cylinder address, which is started by following sector transfer command.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Cylinder high byte							

8. Device/head register: This register is used for selecting the drive number and Head number for the following command.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Obsolete	LBA	Obsolete	DRV	Head number			

Bit	Name	Function
7	Obsolete	This bit is set to “1”.
6	LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA = 0, CHS mode is selected. When LBA = 1, LBA mode is selected. In LBA mode, the Logical Block Address is interpreted as follows: LBA07-LBA00: Sector Number Register D7-D0. LBA15-LBA08: Cylinder Low Register D7-D0. LBA23-LBA16: Cylinder High Register D7-D0. LBA27-LBA24: Drive/Head Register bits HS3-HS0.
5	Obsolete	This bit is set to “1”.
4	DEV (Device select)	This bit is used for selecting the Master (Drive 0) and Slave (Drive 1) in Master/Slave organization. Cleared to zero selects the Master (Drive 0)
3	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

9. Status register: This register is read-only. It indicates the status of the command execution. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device. Reading this register when an interrupt is pending causes the pending interrupt to be cleared. The host should not read the Status register when an interrupt is expected as this may clear the pending interrupt before the INTRQ can be recognized by the host.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BSY	DRDY	DWF	DSC	DRQ	CORR	Obsolete	ERR

Bit	Name	Function
7	BSY (BuSY)	This bit is set to “1” when an internal operation is executing. When this bit is set to “1”, other bits in this register are invalid.
6	DRDY (Drive ReaDY)	This bit is set to “1” when an internal operation has been ended and the drive is capable of being accessed from the host.
5	DWF (Drive Write Fault)	This bit is set to “1” if this drive indicates a write fault status.
4	DSC (Drive Seek Complete)	This bit is set to “1” when the drive seek is complete.
3	DRQ (Data ReQuest)	This bit is set to “1” when the device is ready to transfer a word of data between the host and Data register.
2	CORR (CORRected data)	This bit is set to “1” when a correctable data error has occurred and the data has been corrected.
1	Obsolete	This bit is always set to “0”.
0	ERR (ERRor)	This bit is set to “1” when the previous command has ended in some type of error. The error information is set in the Error register. This bit is cleared by the next command.

10. Alternate status register: This register is the same as the Status register in the command block. The bit assignment is same as the prior description of the Status register. But this register is different from the Status register in that -IREQ is not negated when data is read.

11. Device control register: This register is write-only. This register allows a host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reserved			SRST	nIEN	0

Bit	Name	Function
7~3	X	Reserved bits
2	SRST (Software ReSeT)	This bit is set to “1” in order to have the drive perform Software Reset operation. The drive remains in Reset until this bit is set to “0”.
1	nIEN (Interrupt Enable)	This bit is used to enable INTRQ. When this bit is set to”0”, INTRQ is active. When this bit is set to “1”, INTRQ is high impedance.
0	0	This bit is set to “0”.

12. Drive Address register: This register is read-only. It is used for confirming the drive status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
×	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

Bit	Name	Function
7	X	This bit is unknown. It remains in tri-state, when host read.
6	nWTG (WriTing Gate)	“0”
5~2	nHS3-0 (Head Select 3~0)	These 4 bits are the negative value of Head Number in the Drive/Head register.
1	nDS1 (Idrive Select 1)	This bit is “0”, when drive 1 is selected.
0	nDS0 (Idrive Select 0)	This bit is “0”, when drive 0 is selected.

13. Command register: This register is write-only. Each command to be executed is written to this register, after setting the parameters as follows.

		Used Parameter						
Command	Command code	FR	SC	SN	CY	DR	HD	LBA
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
CFA erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	N	N	N	N	Y	N	N
CFA request extended error	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Sleep	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
CFA translate sector	87H	N	N	Y	Y	Y	Y	Y
CFA wear level	F5H	N	N	N	N	Y	N	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
CFA write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
CFA write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

Note: FR: Feature register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder Low/High register
DR: DRV bit of Drive Head register
HD: Head Number of Drive/Head register
LBA: Logical Block Address Mode Supported
Y: The register contains a valid parameter for this command
N: The register does not contain a valid parameter for this command

ATA Command Specification

1. Check Power Mode (code: E5H or 98H): This command checks the power mode.
2. Execute Drive Diagnostic (code: 90H): This command performs the internal diagnostic tests implemented by the drive.
3. CFA Erase Sector (s) (code: C0H): This command is used to erase data sectors.
4. Format Track (code: 50H): This command writes the desired head and cylinder of the selected drive. But selected sector data is not exchanged. This drive expects one sector (512 bytes) of data from the host to follow the command with the same protocol as the Write Sector Command
5. Identify Drive (code: ECH): This command enables the host to receive parameter information from the drive.

Identify Drive Information

Word address	Default value	Total bytes	Data field type information
0	040AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	XXXX	2	Number of unformatted bytes per track
5	XXXX	2	Number of unformatted bytes per sector
6	XXXX	2	Default number of sectors per track
7 to 8	XXXX	4	Reserved
9	0000H	2	Reserved
10 to 19	XXXX	20	Serial number in ASCII
20	0001H	2	Buffer type(single ported)
21	0004H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23 to 46	XXXX	48	Firmware revision in ASCII etc.
47	0001H	2	Maximum number of sectors on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT Supported (bit8), LBA supported (bit9)
50	0000H	2	Reserved
51	0400H	2	PIO data transfer cycle timing mode 4
52	0000H	2	DMA data transfer cycle timing mode not Supported
53 to 58	XXXX	12	Reserved
59	0101H	2	Multiple sector setting is valid
60 to 61	XXXX	4	Total number of sectors addressable in LBA Mode
62 to 255	0000H	388	Reserved

6. Idle (code: E3H or 97H): This command causes the drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.
7. Idle Immediate (code: E1H or 95H): This command causes the drive to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

8. Initialize Drive Parameters (code: 91H): This command enables the host to set the number of sectors per track and the number of heads per cycle.
9. Read Buffer (code: E4H): This command enables the host to read the current contents of the drive's sector buffer.
10. Read Multiple (code: C4H): This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
11. Read Long Sector (code 22H or 23H): This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
12. Read Sector(s) (code 20H, 21H): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer beings at the sector specified in the Sector Number register.
13. Read Verify Sector(s) (code: 40H or 41H): This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
14. Recalibrate (code: 1XH): This command is effectively a NOP command to the drive and is provided for compatibility purposes.
15. CFA Request Extended Error (code: 03H): This command requests an extended error code after command ends with an error.
16. Seek (code: 7XH): This command is effectively a NOP command to the drive although it does perform a range check.
17. Set Features (code: EFH): This command is used by the host to establish or select certain features.

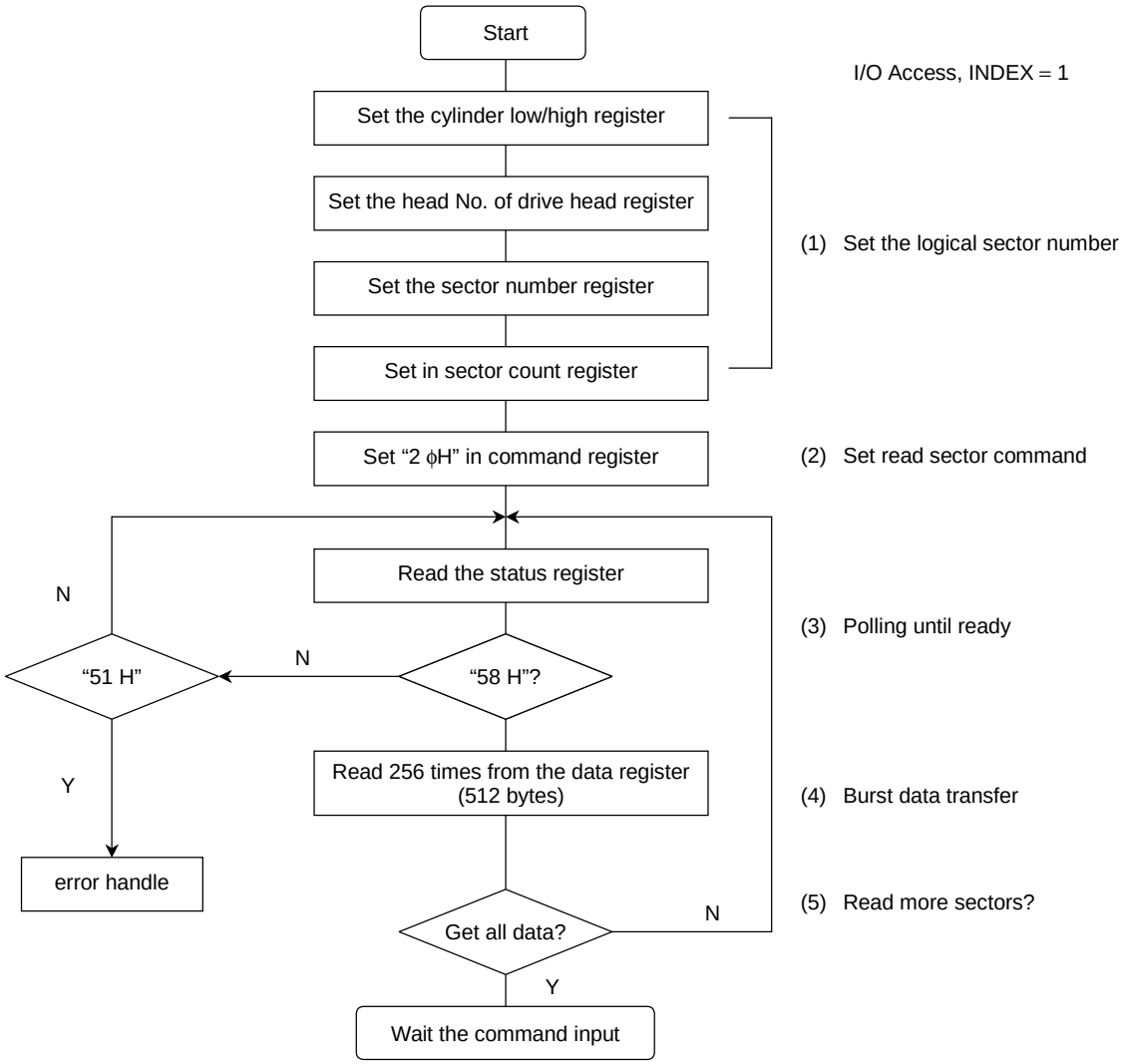
Feature	Operation
01H	Enable 8-bit data transfers.(CFA feature set only)
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
81H	Disable 8-bit data transfers. (CFA feature set only)
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

18. Set Multiple Mode (code: C6H): This command enables the drive to perform Read and Write Multiple operations and establishes the block count for these commands.
19. Sleep (code: E6H or 99H): This command causes the drive to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.
20. Stand By (code: E2H or 96H): This command causes the drive to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.
21. Stand By Immediate (code: E0H or 94H): This command causes the drive to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately
22. CFA Translate Sector (code: 87H): This command allows the host a method of determining the exact number of times a use sector has been erased and programmed
23. CFA Wear Level (code: F5H): This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00H indicating Wear Level is not needed.
24. Write Buffer (code: E8H): This command enables the host to overwrite contents of the drive's sector buffer with any data pattern desired.
25. Write Long Sector (code: 32H or 33H): This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

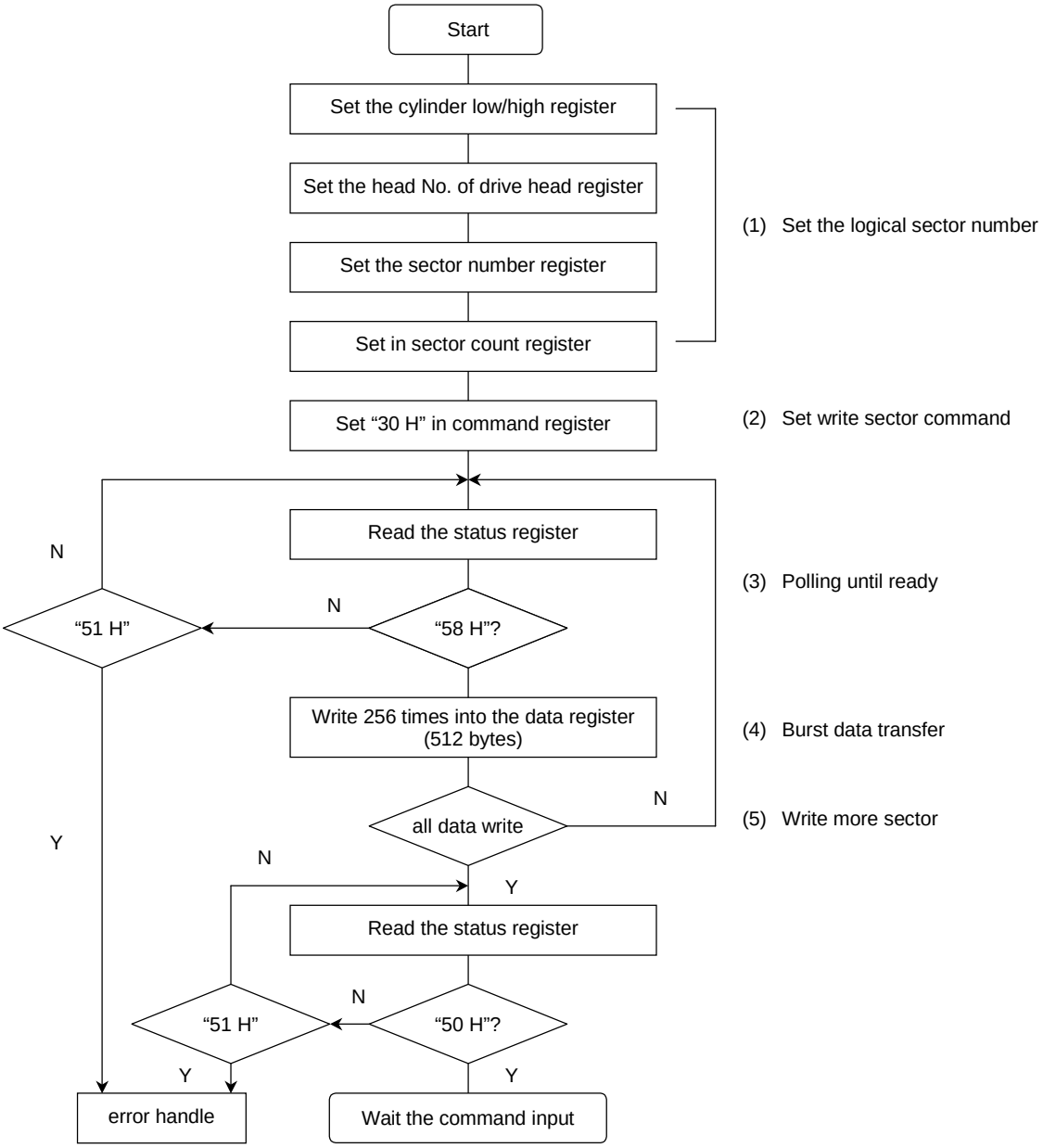
26. Write Multiple (code: C5H): This command is similar to the Write Sector(s) command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.
27. CFA Write Multiple without Erase (code: CDH): This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.
28. Write Sector(s) (code: 30H or 31H): This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
29. CFA Write Sector(s) without Erase (code: 38H): This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.
30. Write Verify(s) (code: 3CH): This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

Sector Transfer Protocol

1. Sector read: The protocol of sector(s) read is as follows.



2. Sector write: The protocol of write sector(s) is as follows.

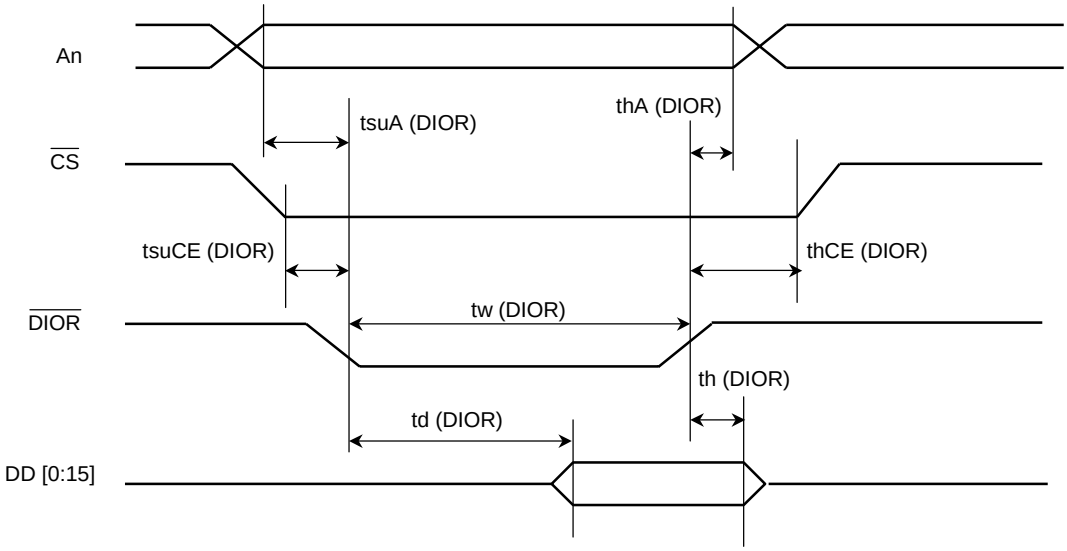


AC Characteristics (Ta = –40 ~ +85°C, V_{CC} = 5 V ± 10%)

Access Read AC Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Data delay after DIOR	td (DIOR)	—	—	50	ns
Data hold following DIOR	th (DIOR)	5	—	—	ns
DIOR width time	tw (DIOR)	70	—	—	ns
Address setup before DIOR	tsuA (DIOR)	15	—	—	ns
Address hold following DIOR	thA (DIOR)	10	—	—	ns
CS setup before DIOR	tsuCS (DIOR)	5	—	—	ns
CS hold following DIOR	thCS (DIOR)	10	—	—	ns

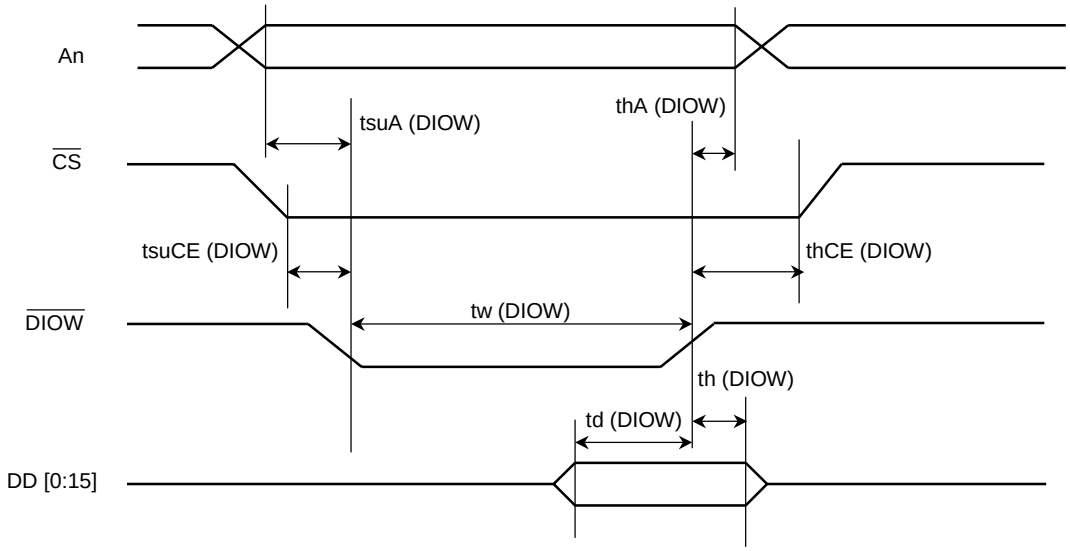
Access Read Timing



Access Write AC Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Data setup before DIOW	tsu (DIOW)	20	—	—	ns
Data hold following DIOW	th (DIOW)	10	—	—	ns
DIOW width time	tw (DIOW)	70	—	—	ns
Address setup before DIOW	tsuA (DIOW)	15	—	—	ns
Address hold following DIOW	thA (DIOW)	10	—	—	ns
CS setup before DIOW	tsuCS (DIOW)	5	—	—	ns
CS hold following DIOW	thCS (DIOW)	10	—	—	ns

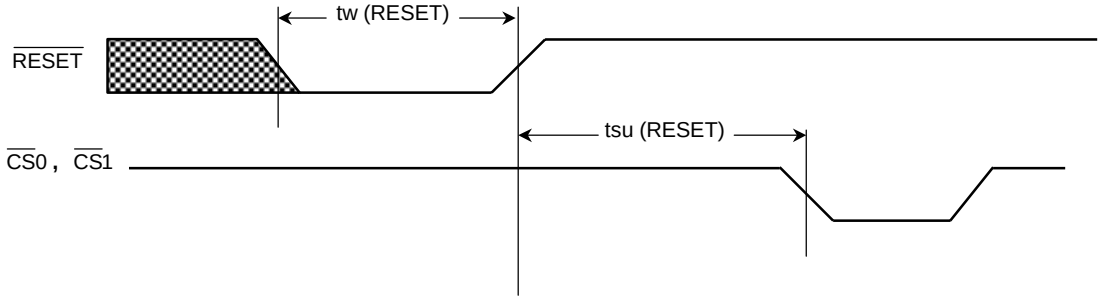
Access Write Timing



Power on Reset Characteristics

This table summarizes the power on reset sequence.

Hard Reset Timing



Hard Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Reset setup time	tsu (RESET)	2	—	—	ms	
Reset pulse width	tw (RESET)	25	—	—	µs	

Attention for Drive Use

- After performing the reset or power off operation, the information of all registers is cleared.
- Please do not insert or remove the drive while the host is active.
- After performing a hard reset, soft reset, power on reset or command input, commands cannot be applied to the drive while the bit7 (BSY) in the Status register is “high” level. Flash drive will not respond in this case.
- It is recommended that the drive should be formatted using an operating system before using it.