

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 175 \text{ mA}$  at 100 MHz
- Low CMOS standby power
  - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic Power-down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 54-pin TSOP II package

## Functional Description

The CY7C10612DV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

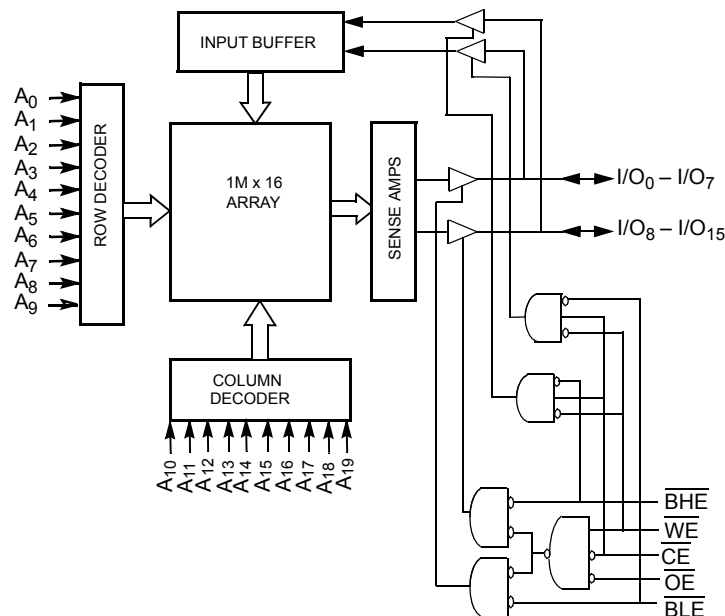
To write to the device, take Chip Enables ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, take Chip Enables ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See Truth Table on page 10 for a complete description of Read and Write modes.

The input or output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

The CY7C10612DV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



## Contents

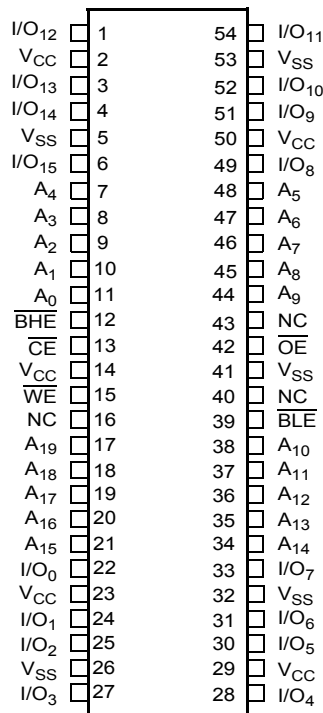
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### Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

### Pin Configuration

Figure 1. 54-pin TSOP II (Top View) [1]



**Note**

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage on V <sub>CC</sub> Relative to GND [2] .....	-0.5 V to +4.6 V
DC Voltage Applied to Outputs in High Z State [2] .....	-0.5 V to V <sub>CC</sub> + 0.5 V

DC Input Voltage [2] .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015) .....	> 2001 V
Latch Up Current .....	> 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH voltage	Min V <sub>CC</sub> , I <sub>OH</sub> = -4.0 mA	2.4	-	V
V <sub>OL</sub>	Output LOW voltage	Min V <sub>CC</sub> , I <sub>OL</sub> = 8.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage [2]		-0.3	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels	-	175	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	30	mA
I <sub>SB2</sub>	Automatic CE power-down current – CMOS Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3 V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0	-	25	mA

## Capacitance

Parameter [3]	Description	Test Conditions	54-pin TSOP II	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	6	pF
C <sub>OUT</sub>	I/O capacitance		8	pF

## Thermal Resistance

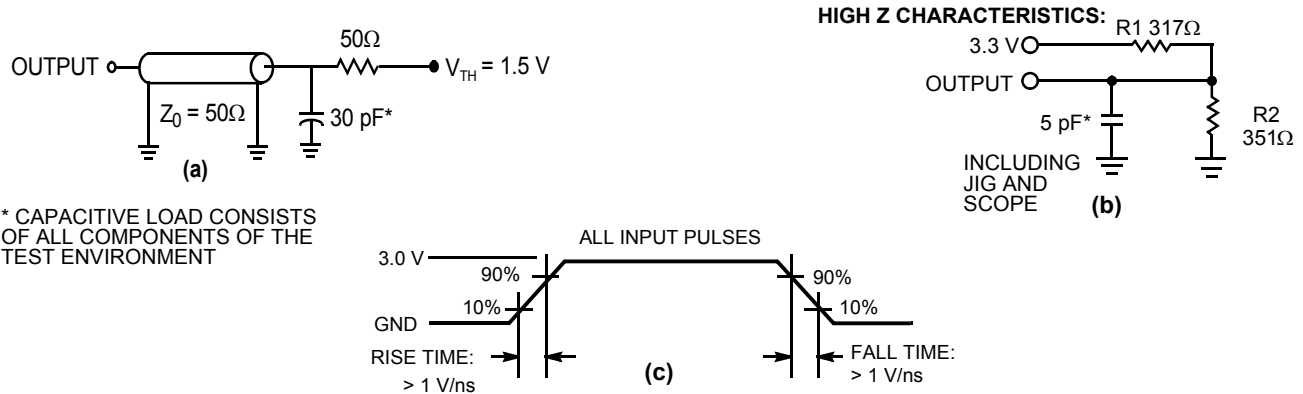
Parameter [3]	Description	Test Conditions	54-pin TSOP II	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		5.40	°C/W

### Note

- V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



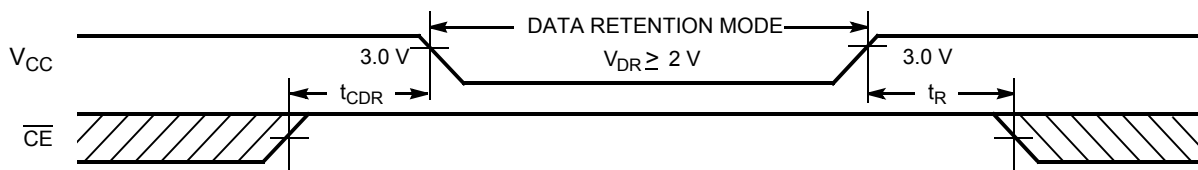
### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [5]	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2	–	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	25	mA
$t_{CDR}^{[6]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[7]}$	Operation recovery time		$t_{RC}$	–	–	ns

### Data Retention Waveform

Figure 3. Data Retention Waveform



**Notes**

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0 V). 100  $\mu\text{s}$  ( $t_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation begins including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0 V) voltage.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the Operating Range

Parameter <sup>[4]</sup>	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}$	$V_{CC}$ (typical) to the first access <sup>[5]</sup>	100	–	$\mu$ s
$t_{RC}$	Read cycle time	10	–	ns
$t_{AA}$	Address to data valid	–	10	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z	1	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[6]</sup>	–	5	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[6]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[6]</sup>	–	5	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up <sup>[7]</sup>	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down <sup>[7]</sup>	–	10	ns
$t_{DBE}$	Byte enable to data valid	–	5	ns
$t_{LZBE}$	Byte enable to low Z	1	–	ns
$t_{HZBE}$	Byte disable to high Z	–	5	ns
<b>Write Cycle <sup>[8, 9]</sup></b>				
$t_{WC}$	Write cycle time	10	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	7	–	ns
$t_{AW}$	Address setup to write end	7	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	ns
$t_{SD}$	Data setup to write end	5.5	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[6]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[6]</sup>	–	5	ns
$t_{BW}$	Byte enable to end of write	7	–	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of Figure 2 on page 5, unless specified otherwise.
- $t_{POWER}$  gives the minimum amount of time that the power supply is at typical  $V_{CC}$  values until the first memory access is performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of Figure 2 on page 5. Transition is measured  $\pm 200$  mV from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . Chip enable must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [10, 11]

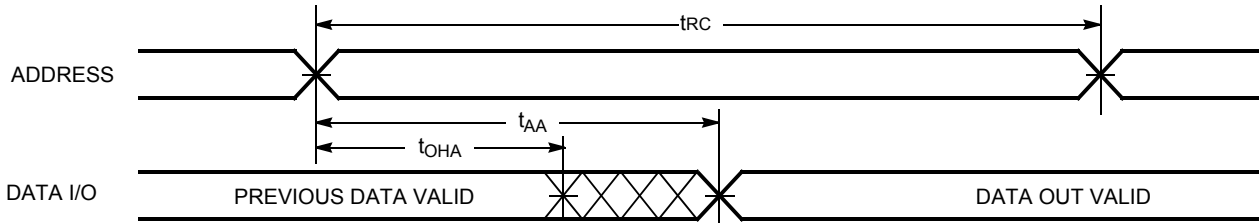
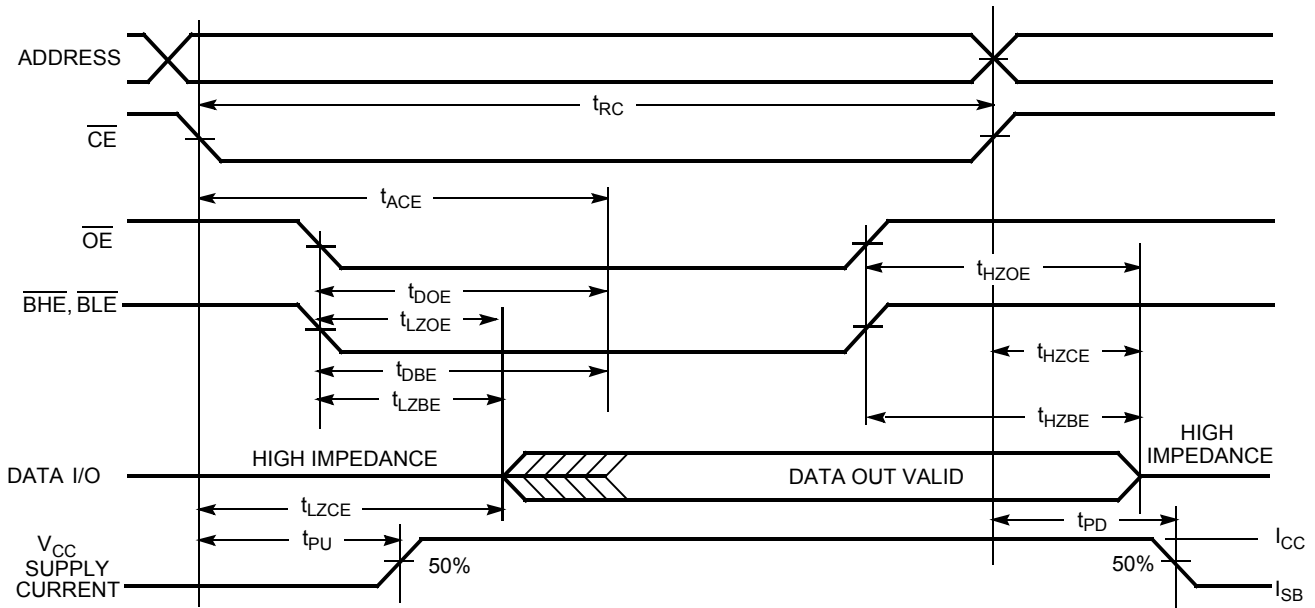


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [11, 12]



**Notes**

- 10. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ .
- 11.  $\overline{WE}$  is HIGH for read cycle.
- 12. Address valid before or similar to  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [13, 14]

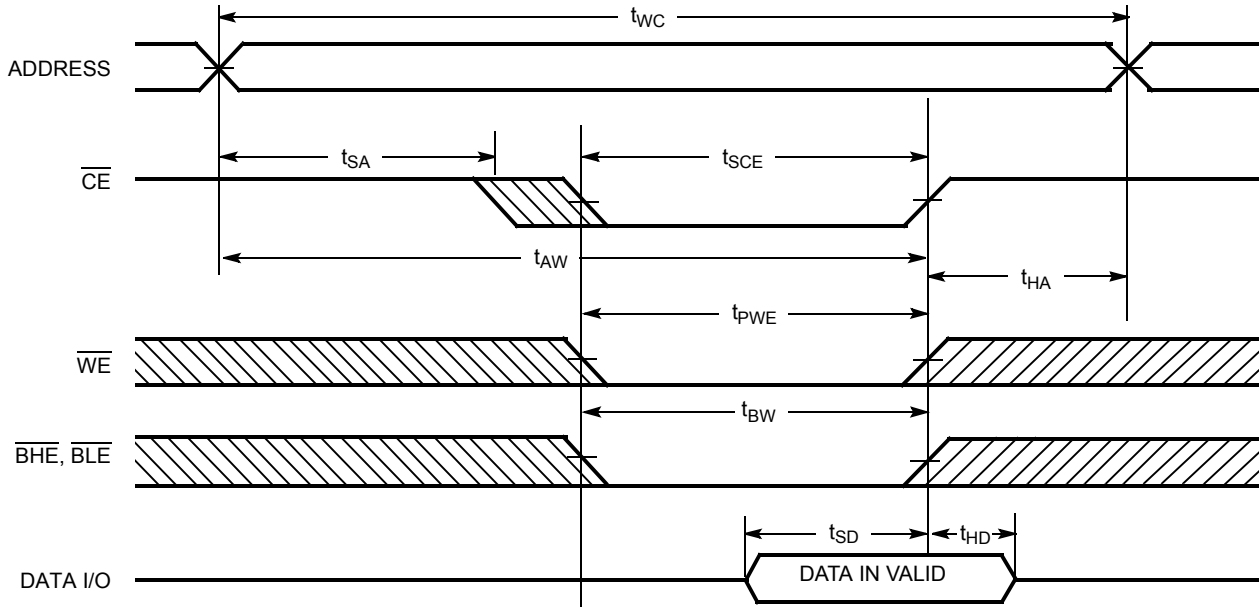
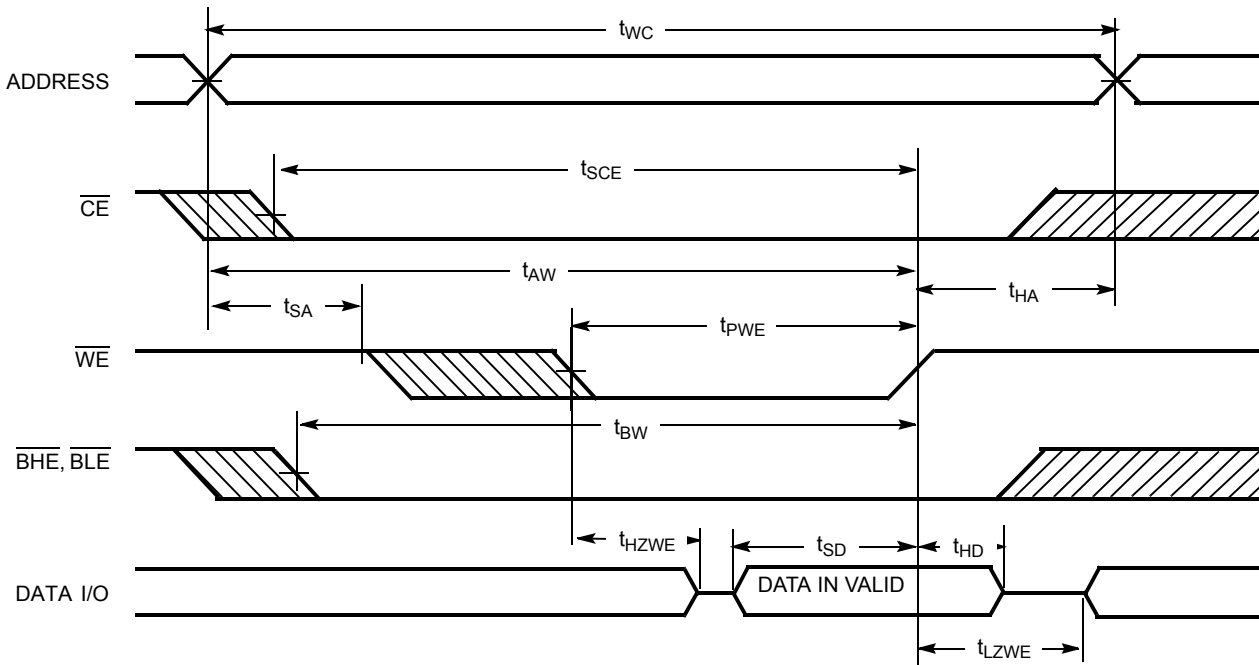


Figure 7. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [13, 14]



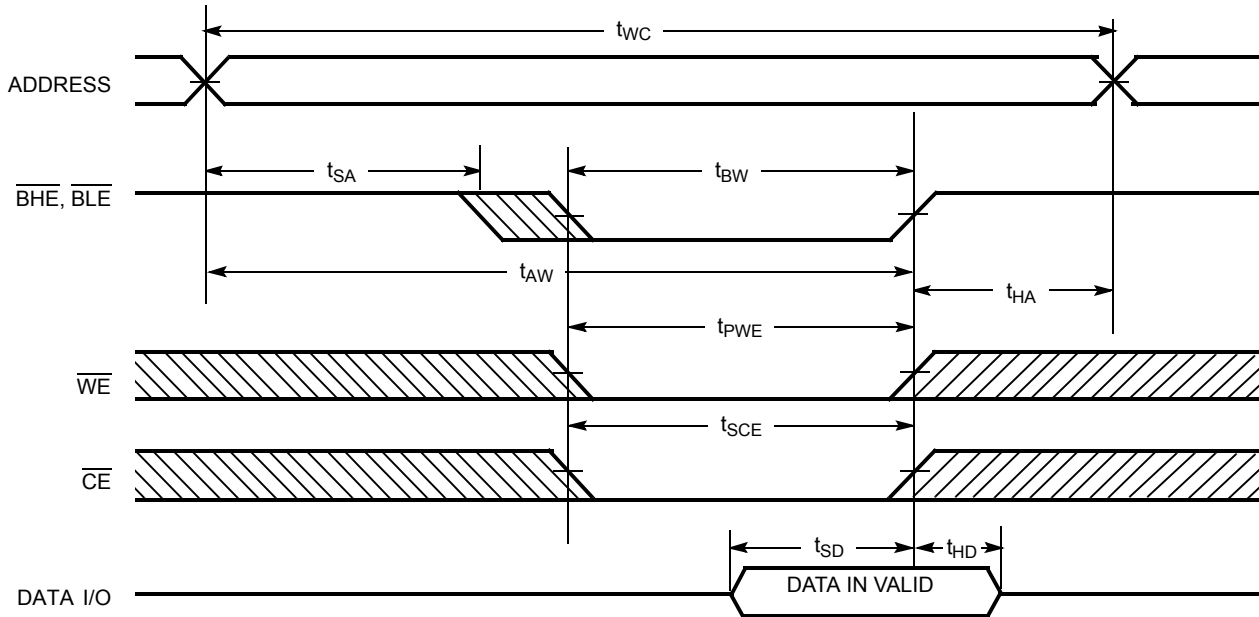
Notes

- 13. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 14. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.



Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) <sup>[15]</sup>



**Note**  
15. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

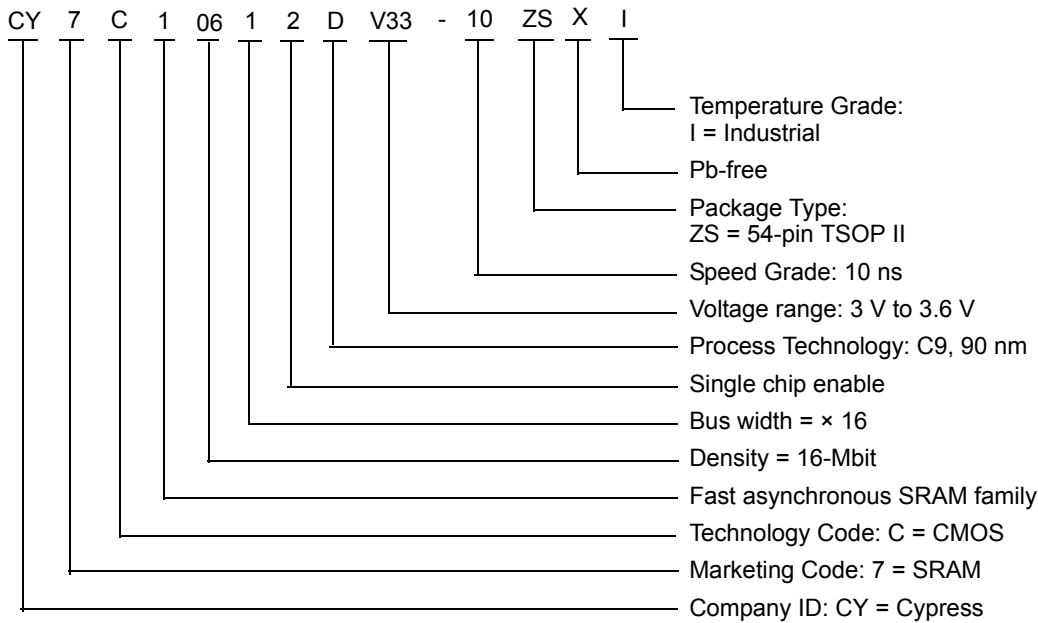
**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data Out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	High Z	Data Out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data In	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	High Z	Data In	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**Ordering Information**

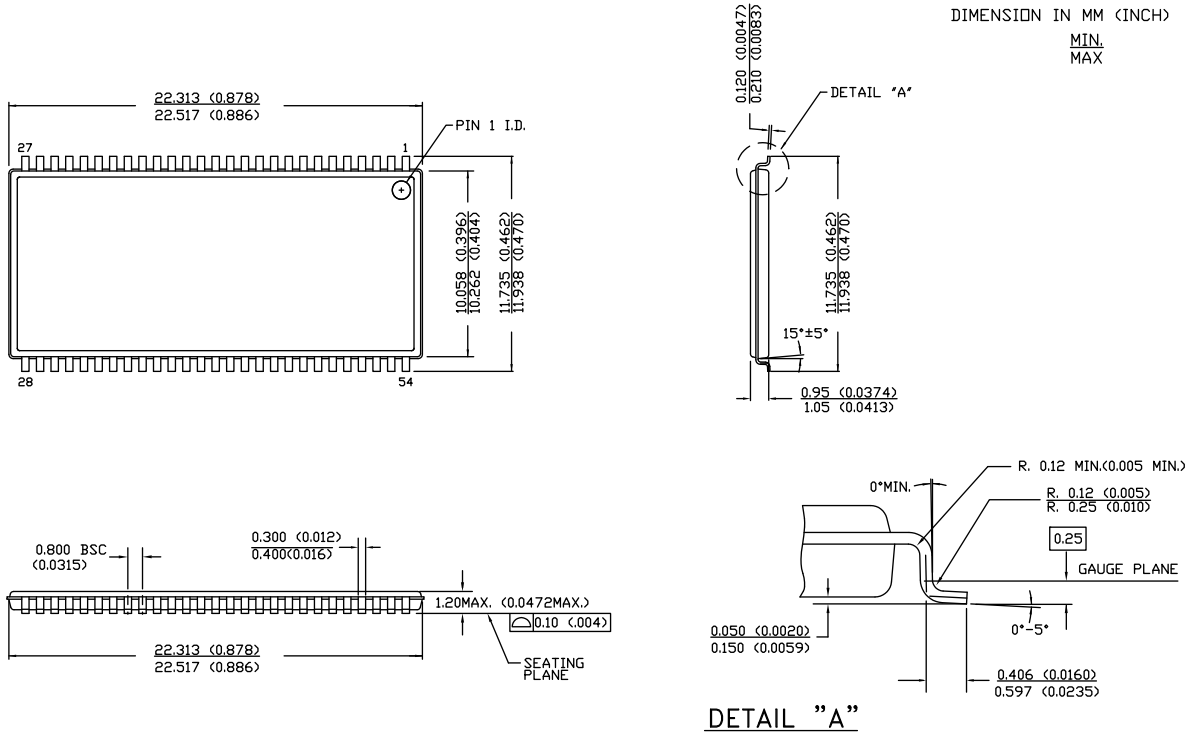
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C10612DV33-10ZSXI	51-85160	54-pin TSOP II (Pb-free)	Industrial

**Ordering Code Definitions**



Package Diagrams

Figure 9. 54-pin TSOP Type II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 \*C

## Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
WE	write enable

## Document Conventions

### Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C10612DV33, 16-Mbit (1 M × 16) Static RAM Document Number: 001-49315				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2589743	VKN / PYRS	10/15/08	New datasheet
*A	2718906	VKN	06/15/09	Post to external web
*B	3128718	PRAS	01/05/11	Template updates. Style changes. IO changed to I/O through out the document. Under Data Retention Characteristics on Page 6, "Typ" is associated with a new footnote # 10. Included ordering code definitions, Acronyms and units of measure tables. Updated package diagram from ** to *A.
*C	3412972	TAVA	10/18/2011	Updated <a href="#">Features</a> . Updated <a href="#">DC Electrical Characteristics</a> . Updated <a href="#">Switching Waveforms</a> . Updated <a href="#">Package Diagrams</a> . Updated in new template.

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