4 Channel Multi-Mode PSI5 Transceiver E521.41

PRODUCTION DATA – Apr 27, 2016

RoHS compliant

Features

- Transceiver compliant with PSI5 standard v1.3 and v2.1
- Provides four independent master channels (up to 6 sensors each)
- Supporting 125 Kbit/s and 189 Kbit/s protocols
- Supporting synchronous and asynchronous operation modes
- Various diagnostic features
- Internal sync-voltage generation
- Programmable PSI5 channel-voltage 4.6V to 11V
- Automatic threshold adaption to sensor quiescent current
- Reverse polarity protected bus outputs up to 40V
- Enables operation in powertrain and chassis control systems
- Developed according to ISO 26262, based on safety requirements rated up to ASIL C.
- Operating temperature range -40°C to +125°C

General Description

The E521.41 was developed to manage the connection and communication between a microcontroller unit and up to 24 sensor satellites.
Data transmission from the sensor to ECU is done by current modulation on the power supply lines with data rate of 125 Kbit/s or 189 Kbit/s (Manchester coded).
Data transmission from ECU to sensor is done by voltage modulation on the power supply. It supports bidirectional communication. Two methods are supported:

- tooth gap method
- pulse width method

The device is a PSI5 V1.3 and V2.1 compliant transceiver which provides four independently operating channels. The channels are able to communicate in low power-,
standard-, synchronous- and asynchronous operating mode. The communication to µC is done via the SPI or UART interface.

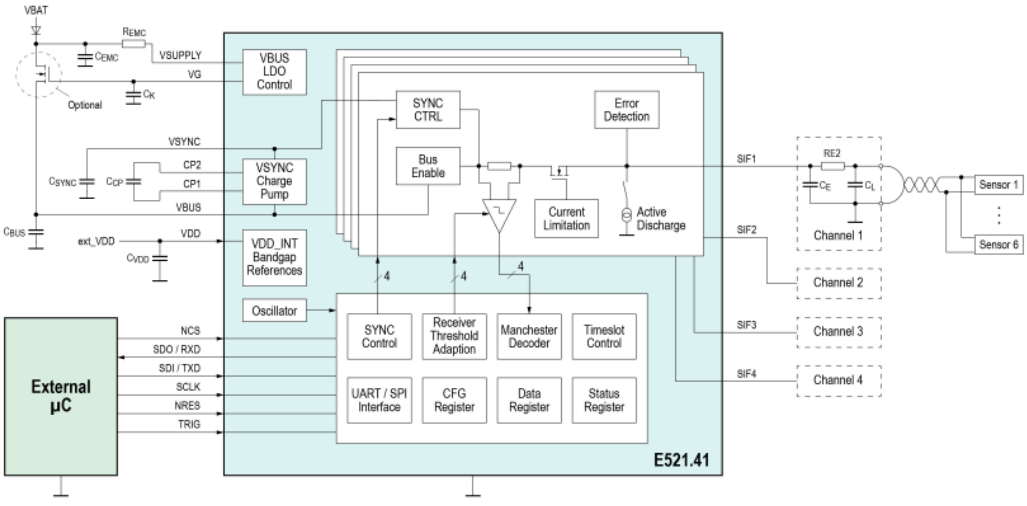
Applications

- Safety (airbag) control systems
- Powertrain control systems
- Vehicle dynamics control system

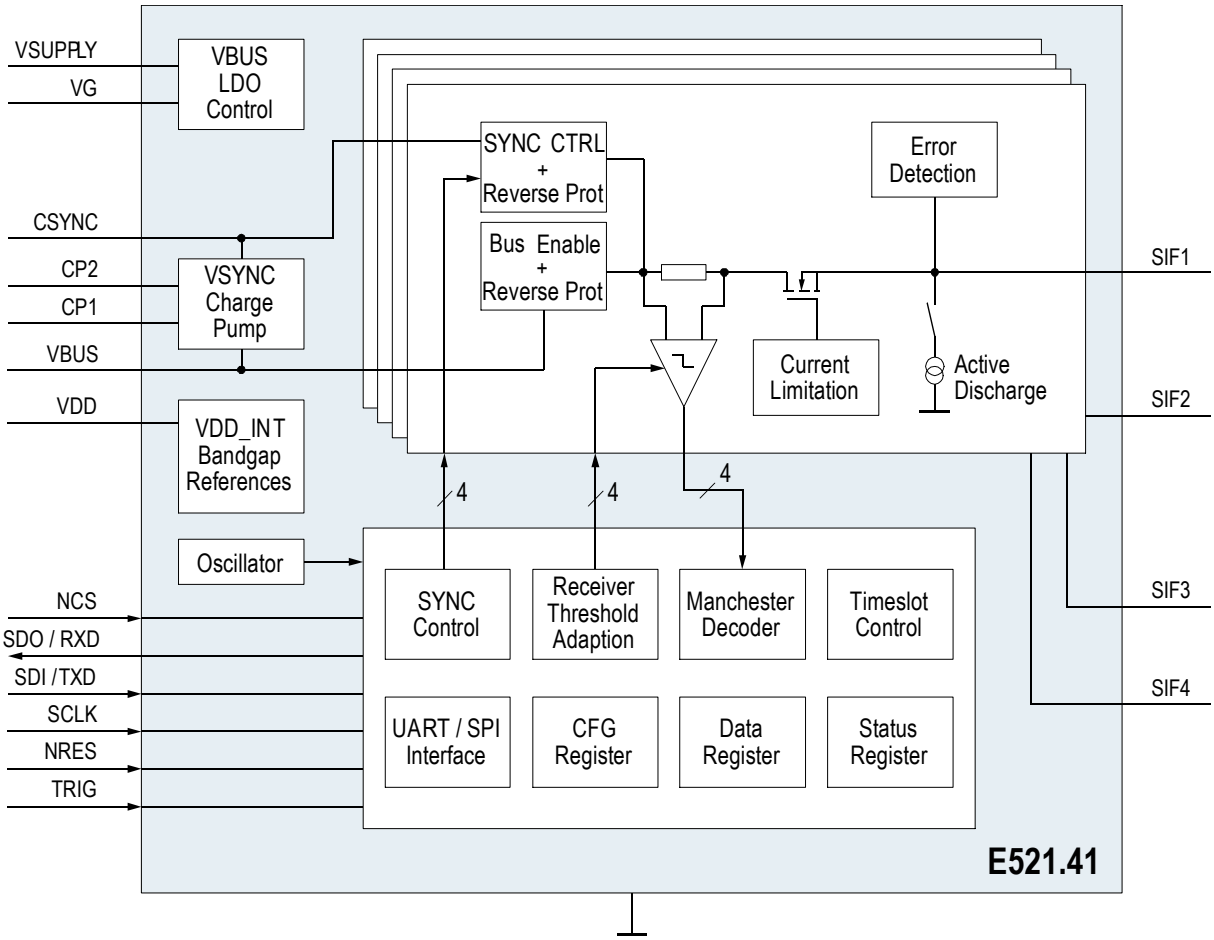
Ordering Information

Ordering-No.:	*Features*	*Package*
E52141A62CXX2	4-channel	QFN20L5
E52141A55E	4-channel	SOIC20

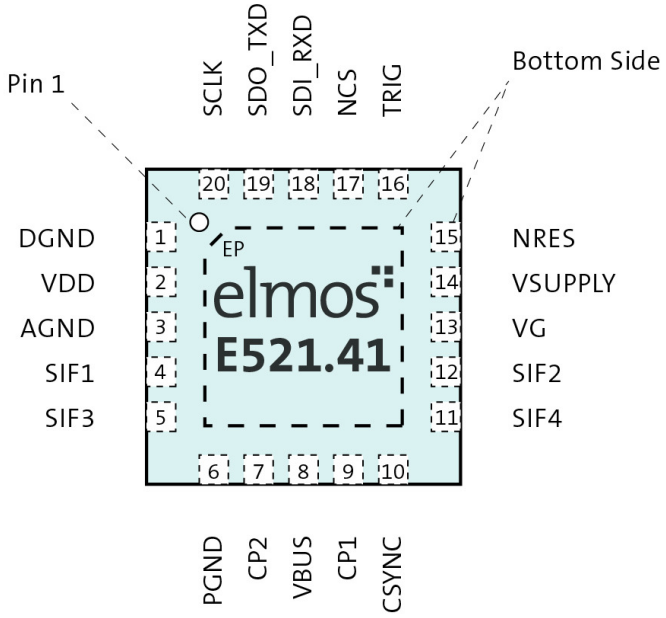
Typical Application Circuit

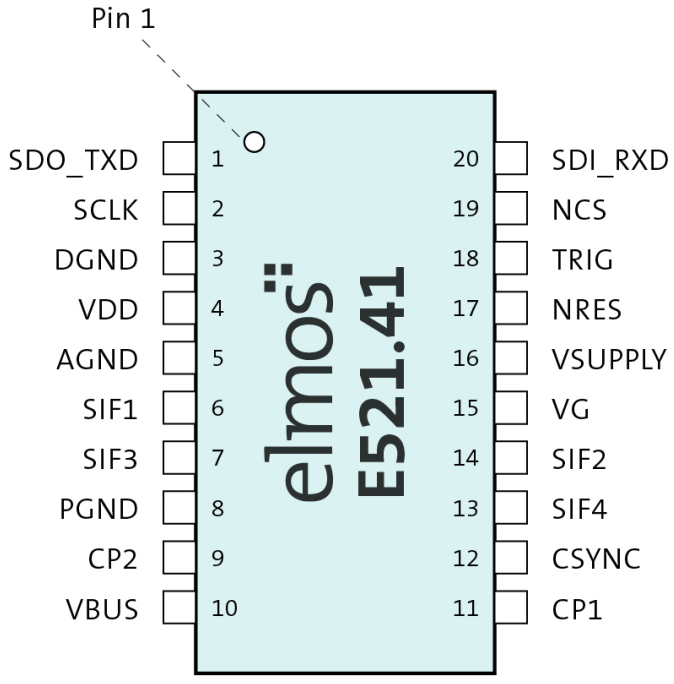


Functional Diagram



1 Package Pinout QFN20L5,SO20





1.1 Pin Description QFN20L5

Table 1.1-1: Pin Description

No	Name	Type	Description
1	DGND	S	Digital voltage supply
2	VDD	S	Digital voltage supply
3	AGND	S	Analog ground
4	SIF1	HV_A_O	Sensor Interface 1
5	SIF3	HV_A_O	Sensor Interface 3
6	PGND	S	Power ground
7	CP2	HV_A_O	Sync charge pump fly capacitor
8	VBUS	HV_S	VBUS voltage
9	CP1	HV_A_O	Sync charge pump fly capacitor
10	CSYNC	HV_S	Sync supply voltage
11	SIF4	HV_A_O	Sensor Interface 4
12	SIF2	HV_A_O	Sensor Interface 2
13	VG	HV_A_O	Gate voltage for external transistor
14	VSUPPPLY	HV_S	Supply voltage
15	NRES	D_I	Negative reset and test mode pin
16	TRIG	D_I	Sync pulse trigger input
17	NCS	D_I	SPI chip select
18	SDI_RXD	D_I	SPI or UART data input
19	SDO_TXD	D_O	SPI or UART data output
20	SCLK	D_I	SPI clock input
	EP	S	QFN20L5 package only Exposed Pad. Connect to large copper ground plane for optimal heat dissipation. Connect to GNDA and GNDD.

Note: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

1.2 Pin Description SO20

Table 1.2-1: Pin Description

No	*Name*	*Type*	*Description*
1	SDO_TXD	D_O	SPI or UART data output
2	SCLK	D_I	SPI clock input
3	DGND	S	Digital ground
4	VDD	S	Digital voltage supply
5	AGND	S	Analog ground
6	SIF1	HV_A_O	Sensor Interface 1
7	SIF3	HV_A_O	Sensor Interface 3
8	PGND	S	Power ground
9	CP2	HV_A_O	Sync charge pump fly capacitor
10	VBUS	HV_S	VBUS voltage
11	CP1	HV_A_O	Sync charge pump fly capacitor
12	CSYNC	HV_S	Sync supply voltage
13	SIF4	HV_A_O	Sensor Interface 4
14	SIF2	HV_A_O	Sensor Interface 2
15	VG	HV_A_O	Gate voltage for external transistor
16	VSUPPPLY	HV_S	Supply voltage
17	NRES	D_I	Negative reset and test mode pin
18	TRIG	D_I	Sync pulse trigger input
19	NCS	D_I	SPI chip select
20	SDI_RXD	D_I	SPI or UART data input

Note: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

2 Application Description

2.1 Application Circuits

2.1.1 Application Circuits

Pin NCS: terminate with GND for UART-mode only, otherwise is used internal pull-up for SPI-mode.
Pin VSUPPLY: terminate with GND if LDO is not used.
Pin VG: terminate with GND if LDO is not used.
Pin CP1: no termination (OPEN) if charge pump is not used.
Pin CP2: no termination (OPEN) if charge pump is not used (must not be connected to GND!!!).
Pin CSYNC: short to VBUS for asynchronous mode.
The CSYNC voltage can be supplied on pin CSYNC (if available on ECU) without using the charge pump.
This option is not shown here.

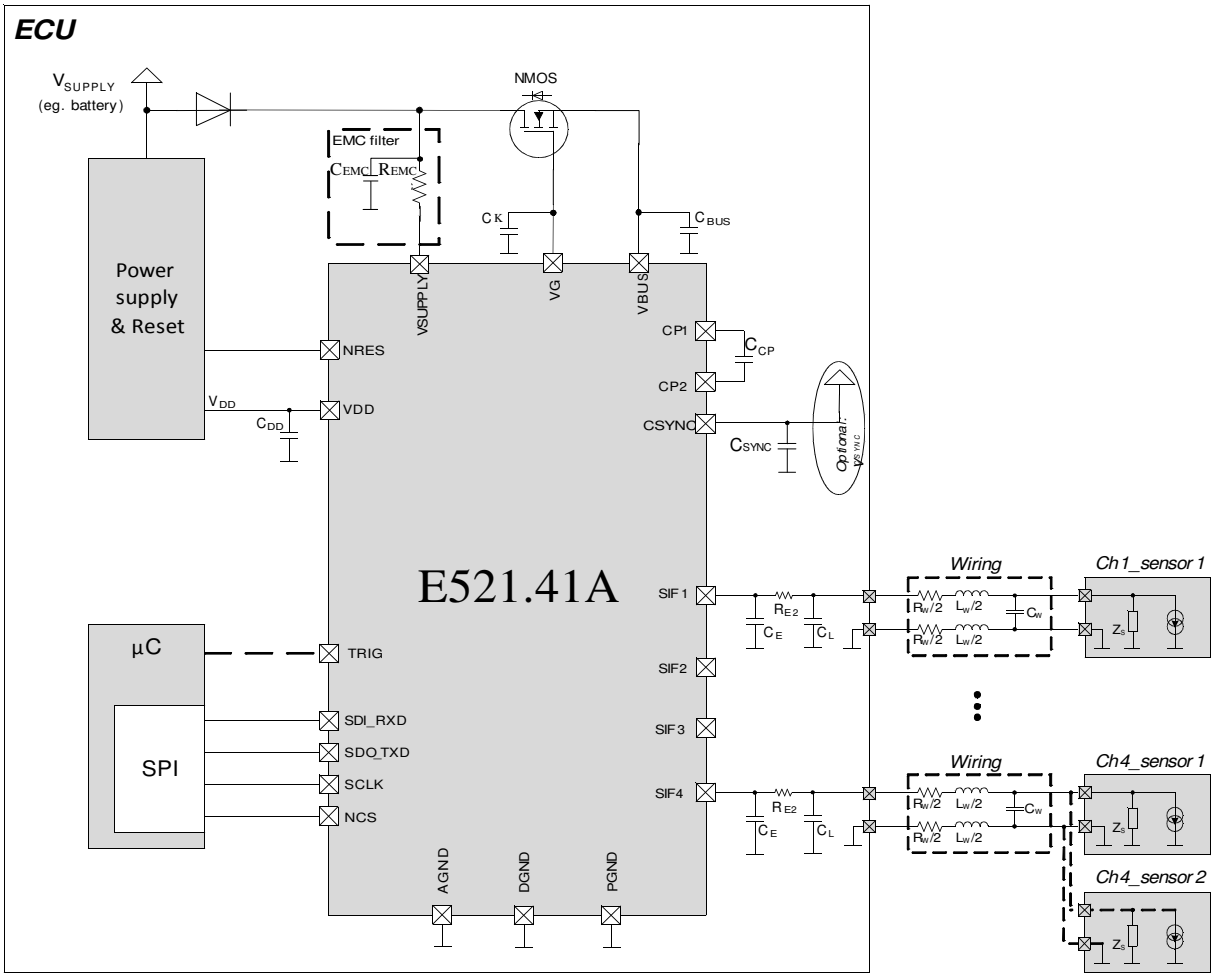


Figure 2.1.1-1: Application Circuit with LDO

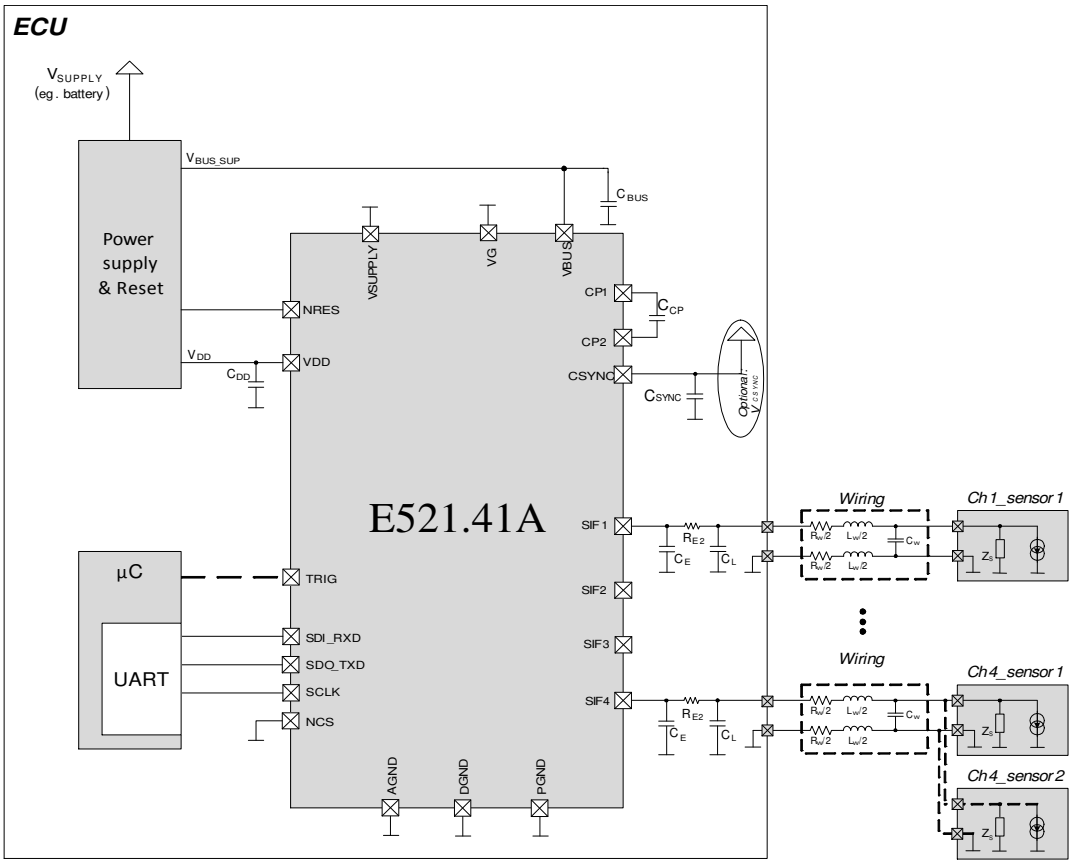


Figure 2.1.1-2: Application Circuit with VBUS Supplied from ECU

Table 2.1.1-1: Application Circuit Electrical Parameter

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Capacitance at VDD		C_{VDD}	100		220	nF
ECU bus capacitance		C_E	15		35	nF
ECU resistor		R_{E2}		2.0		Ω
Satellite capacitance		C_L	2.2			nF
Total bus capacitance		C_E+C_{L_X} (x=1..3)	25		107	nF
LDO Output capacitor	Ceramic capacitor, ESR<=100mΩ	C_{BUS}	4.7		20	µF
Charge pump fly capacitor	Ceramic capacitor; ESR <= 100mΩ	C_{CP}	270			nF
Charge pump storage capacitor	Ceramic capacitor; ESR <= 100mΩ	C_{SYNC}	14.1		20	µF
V_{SUPPLY} EMC capacitor		C_{EMC}		220		nF
V_{SUPPLY} EMC resistor		R_{EMC}			100	Ω
Single wire resistance		$R_W/2$		0.5		Ω
Wire inductance		$2*(L_W/2)$	0		8.7	µH
Wire capacitance		C_W	0		600	pF

The device can be supplied via pin V_{SUPPLY} with an appropriate voltage. This voltage supplies an external NMOS transistor that is driven by an internal LDO via the pin V_G.
The following external NMOS transistor are recommended:

- IRFZ24NS,
- BUK7635-55A,
- HUFA76409D3ST,
- SQD15N06-42L.

The stability of the output voltage can be achieved with an external compensation capacitor C_K connected between pin V_G and AGND. In the following table is shown a suitable compensation capacitor C_K:

Table 2.1.1-2: Recommended Compensation Capacitor

Transistor	***C_K***
IRFZ24NS	100nF-220nF
BUK7635-55A	100nF-220nF
HUFA76409D3ST	100nF-220nF
SQD15N06-42L	100nF-220nF

3 Functional Safety

3.1 Functional Safety Requirements

The device fulfils the functional safety requirement up to ASIL-Level C (system) according to ISO 26262, depending on the safety mechanisms used.

3.2 FMEDA

The following toplevel safety requirements were analysed with FMEDA method:

- TSR1: Transceiver shall avoid transmission of corrupted data to the micro controller interface
- TSR2: Transceiver shall avoid storage of corrupted safety related data

3.2.1 Safety Measures mandatory to reach ASIL Level C

Table 3.2.1-1: mandatory safety mechanisms for ASIL C derived from FMEDA

Safety Mechanism	***IC / System level***	***Description***
SM1	IC	Synchronous decoding of input data in Manchester decoder with fixed baud rate, fixed frame length and fixed bit count. Decoding errors will be indicated in the error status and potentially corrupted data will be invalidated.
SM2	IC	Data consistency check using parity bit or CRC error detection mechanism. Note: These mechanisms must be enabled by interface configuration options from system level.
SM3	System	Observe failure rate of Manchester decoder or parity/CRC errors on system level in order to detect channels with latent faults that could degrade the robustness of decoding or even cause spurious data corruption.
SM4	System / IC	Internal supplies and references are monitored cyclically with a sampling interval of typ. 2ms. Diagnosis block has a separate reference voltage generation independent from the reference of analyzed signals. Supervisor function is implemented for the following signals: V_{BUS}, V_{CSYNC}, V_{SIF1}, V_{SIF2}, V_{SIF3}, V_{SIF4}, VDD, V_{DD_INT}, V_{CP_GATE}.
SM5	System	Data consistencies check using CRC error detection mechanism for SPI and UART.
SM6	System	Configuration data written to registers of the IC shall be (cyclically) verified by reading them back. Available configuration lock mechanisms shall be used.
SM7	System	Compare the SPI response with the command (address, command,CHID,BID, except frame data, register data & XCRC)
SM8	System	Compare the frame ID, ch ID (if not all CH configurations are same) with respect to the configuration & calculate and compare the 3-bit CRC/parity for the sensor data
SM9	System	If interface/asic error indicated, read the error status registers
SM10	System	If start-or stop bit in UART is not detected in time uC can detect UART error on transceiver
SM11	System	Loop Back Diagnosis: Check digital data processing (Manchester decoder / Data latch / MUX / XCRC / UART/SPI).

4 Operating Conditions

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to V(GND). Currents flowing into terminals are positive, those drawn out of a terminal are negative.

4.1 Absolute Maximum Ratings

Table 4.1-1: ESD requirements

No.	Description	Condition	Symbol	Min	Max	Unit
1	ESD according Human Body Model (HBM), Q100-002 for pins SIFx; VSUPPLY; (100pF/1.5kΩ)		ESD pins SIFX,VSUPPLY	±4000		V
2	ESD according Human Body Model (HBM), Q100-002 for all other pins; (100pF/1,5kΩ)		ESD all other pins	±2000		V
3	ESD according Charged Device Model (CDM), Q100-011 Corner pins		ESD corner pins CDM	±750		V
4	ESD according Charged Device Model (CDM), Q100-011 Non-corner pins		ESD non corner pins CDM	±450		V
5	Input voltage range (supply from ECU)		$V_{SUPPPLY}$	-0.3	40	V
6	VBUS voltage range		V_{BUS}	-0.3	40	V
7	NMOS gate voltage at pin V_G		V_G	-0.3	40	V
8	Voltage of charge pump fly cap. - negative pin		V_{CP1}	-0.3	40	V
9	Voltage of charge pump fly cap. - positive pin		V_{CP2}	-0.3	40	V
10	Voltage of charge pump storage capacitor or CSYNC voltage supply (from ECU)		V_{SYNC}	-0.3	40	V
11	Voltage at sensor interface	X=1-4	V_{SIF_X}	-0.3	40	V
12	Supply voltage for analog blocks and digital I/O pins		V_{DD}	-0.3	19	V
13	Voltage of digital input pins		V_{IN_DIG}	-0.3	19	V
14	Voltage of the digital outputs pins		V_{OUT_DIG}	-0.3	19	V
15	Voltage of NRES and testmode pin		V_{NRES}	-0.3	19	V
16	Junction temperature		T_J	-40	150	°C
17	Storage temperature		T_{STG}	-40	125	°C
18	Ambient operating temperature range		T_{AMB}	-40	125	°C
19	Thermal Resistance (junction-ambient) (refer to application notes of QFN-packages, thermal connection of exposed die pad very important)		R_{TJA}		23	K/W

4.2 Recommended Operating Conditions

Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified.
All voltages are referred to ground (0V). Currents flowing into the circuit have positive values.
The first electrical potential connected to the IC must be GND. (If not specified specify timing sequence of electrical contacts.)

Table 4.2-1: Recommended Operation Conditions

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Input voltage range at pin V_{SUPPLY}[1)]	Application with LDO and external NMOS transistor; low voltage mode;	V_{SUPPLY_lp}	5.3		19	V
2	Input voltage range at pin V_{SUPPLY}[1)]	Application with LDO and external NMOS transistor; standard voltage mode;	V_{SUPPLY_std}	6.95		19	V
3	Input voltage range at pin V_{SUPPLY}[1)]	Application with LDO and external NMOS transistor; increased voltage mode;	V_{SUPPLY_inc}	8.0		19	V
4	Input voltage range at pin V_{BUS} limited range[2)]	Application with (externally generated) available V_{BUS} voltage; @ I_{SIFX_OP}=0-25mA LDO is disabled	$V_{BUS\_SUP\_lr}$	4.6		5.05	V
5	Input voltage range at pin V_{BUS} full range[3)]	Application with (externally generated) available V_{BUS} voltage; @ I_{SIFX_OP}=0-65mA LDO is disabled	$V_{BUS\_SUP\_fr}$	5.05		11	V
6	V_{BUS} voltage ripple; 50Hz<f<50kHz[3)]	Application with (externally generated) available V_{BUS} voltage; LDO is disabled	$V_{BUS\_SUP\_RPL}$			100	mVpp
7	V_{BUS} voltage ripple; 50kHz<f<500kHz[3)]	Application with (externally generated) available V_{BUS} voltage; LDO is disabled	$V_{BUS\_SUP\_RPL}$			40	mVpp

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
8	V_{CSYNC} voltage input range[4]	Application with available V_{CSYNC} voltage;	V_{CSYNC}	V_{t3} +V_{CSYNC_DR}		35	V
9	V_{CSYNC} voltage ripple	Application with available V_{CSYNC} voltage;	V_{CSYNC_RPL}			500	mVpp
10	Digital supply voltage	3V3-mode	V_{DD}	2.97		3.63	V
11	Digital supply voltage	5V-mode	V_{DD}	4.5		5.5	V
12	[5]	V_{BUS} voltage rising slew rate	V_{BUS_RISE}			$8/C_{SYNC}$	V/µs
13	Sensor quiescent current	Standard current	I_{LOW_std}	-19.0		-4	mA
14	Sensor quiescent current	Extended current	I_{LOW_ext}	-35.0		-4	mA
15	Sensor sink current	Low power mode	ΔI_{S_lp}	-15.0	-13.0	-11.0	mA
16	Sensor sink current	Common mode	ΔI_{S_ext}	-30.0	-26.0	-22.0	mA
17	Sensor interface current, low power mode	$I_{SIFX}=-(I_{low}+\Delta I_S)$	$I_{SIFX\_OP\_lp}$	-50.0		-4.0	mA
18	Sensor interface current,increased mode	$I_{SIFX}=-(I_{low}+\Delta I_S)$	$I_{SIFX\_OP\_inc}$	-65.0		-4.0	mA
19	Clock frequency depending on UART data rate	UART mode	f_{SCLK_EXT}	13		32	MHz
20	Baud rate	UART mode	f_{UART}		$f_{SCLK\_EXT}/5$		bps
21	Duty cycle of f_{SCLK_EXT}	UART mode	DC_{SCLK_EXT}	30		70	%
22	Frequency deviation of f_{SCLK_EXT}	UART mode,maximum deviation with one UART tele-gram (11 bit)	$FDEV_{SCLK\_EXT}$	-1.5		1.5	%
23	SPI frequency	50% duty cycle	f_{SCLK}	0		5	MHz

[1] The following external NMOS transistors are recommended: IRFZ24NS, BUK7635-55A, HUFA76409D3ST and SQD15N06-42L.
The max.input current of V_{SUPPLY} is 350mA (operating mode). Max. value including: 4 sensor interfaces including current modulation, CSYNC charge pump avg.current, short circuit for one interface and internal current consumption.
[2] Limited range of I_{SIFX}: V_{BUS_min}=4.6V with I_{SIFX_OPM}=25mA (I_{LOW}=10mA and I_{SINK}=15mA)
[3] Full range of I_{SIFX} operating
[4] V_{SYNC_DR} is the voltage drop between V_{CSYNC} and V_{SIFx}, V_{t3} see Figure 6.1.3.6-1
[5] To limit the current through schottky diodes and V_{CSYNC} capacitor to 8A

5 Detailed Electrical Specification

5.1 ANALOG PART

5.1.1 SUPPLY

Table 5.1.1-1: Current Consumption: Electrical Parameter Table

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	$I_{VSUPPLY}$ quiescent current consumption*) 1)	Application with LDO disabled	$I_{VSUPPLY\_Q}$		15		µA
2	$I_{VSUPPLY}$ current consumption operating1)	Application with LDO enabled	$I_{VSUPPLY\_OP}$	0.1		1	mA
3	I_{VBUS} quiescent current consumption	Application with available V_{BUS} voltage; interfaces off	I_{VBUS_Q}	1		4	mA
4	I_{VBUS} current consumption operating	Application with available V_{BUS} voltage; interfaces on; without load;	I_{VBUS_OP}	6		14	mA
5	I_{CSYNC} quiescent current consumption	Application with available V_{CSYNC} voltage; interfaces on; without load;	I_{CSYNC_Q}	0.05		5	mA
6	Logic supply operating current	VDD=5.5V;NRES=0V	I_{VDD_off}	4		10	mA
7	Logic supply operating current	VDD=5.5V;NRES=VDD	I_{VDD_on}	1		10	mA

*) Not tested in production
1) $I_{VSUPPLY}$ is the current consumption of the pin V_{SUPPLY}

5.1.1.1 LDO Control Block

5.1.1.1.1 Electrical Parameter of LDO

Table 5.1.1.1.1-1: Electrical Parameter Table of LDO

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Stabilized output voltage of LDO at pin V_{BUS}1)	low power mode; 5mA<=I_{LOAD_BUS}<=350mA; 5.3V<=V_{SUPPLY}<=19V	V_{BUS_LP}	5.15 - 2%	5.15	5.15 + 2%	V
2	Stabilized output voltage of LDO at pin V_{BUS}1)	standard power mode; 5mA<=I_{LOAD_BUS}<=350mA; 6.95V<=V_{SUPPLY}<=19V	V_{BUS_STD}	6.65 - 3%	6.65	6.65 + 3%	V

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
3	Stabilized output voltage of LDO at pin V_{BUS} [1)]	increased power mode; 5mA<=I_{LOAD_BUS}<=350mA; 8.0V<=V_{SUPPLY}<=19V	V_{BUS_INC}	7.7 - 3%	7.7	7.7 + 3%	V
4	Input voltage ripple rejection ratio for low frequencies [*)]	50Hz<=f<=20kHz; V_{SUPPLY_AC}=4V_{PP}; V_{SUPPLY_DC}>9V; C_{BUS}=4.7µF;VBUS=6.65V-setting 5mA<=I_{BUS}<=350mA;	$V_{BUS\_RR\_LF}$	40			dB
5	Input voltage ripple rejection ration for high frequencies [*)]	100kHz<=f<=500kHz; V_{SUPPLY_AC}=400m-V_{PP}; 5.6V<=V_{SUPPLY}<=6.4V; C_{BUS}=4.7µF;VBUS=5.15V-setting 5mA<=I_{LOAD_BUS}<=350mA;	$V_{BUS\_RR\_HF}$	20			dB
6	Line regulation (ΔV_{BUS} voltage for variable V_{SUPPLY} voltage)	I_{LOAD_BUS} is constant during test: 5mA<=I_{LOAD_BUS}<=350mA; V_{SUPPLY} varies: 5.6V<=V_{SUPPLY}<=19V	V_{BUS_LIR}	-25	0	25	mV
7	Load regulation (ΔV_{BUS} voltage for variable I_{LOAD_BUS} current)	V_{SUPPLY} is constant during test: 5.6V<=V_{SUPPLY}<=19V;I_{LOAD_BUS} varies during test: 5mA<=I_{LOAD_BUS}<=350mA	V_{BUS_LOR}	-25	0	25	mV
8	V_{BUS} voltage overshoot [*)]		V_{BUS_OS}			10	%
9	V_{BUS} voltage start-up time [*) 2)]		t_{start_LDO}			[2)]	
10	Internal charge pump for LDO	LDO charge pump output voltage	V_{CP_GATE}	10		19	V

*) Not tested in production
1) trimmed
2) Start-Up time t_{start_LDO} can be calculated by following formula: $t_{start\_LDO}=(V_{TH}+V_{GS\_eff})*C_K/I_{VG\_DRV}$; for V_{TH} and V_{GS_eff} see NMOS transistor data sheet; C_K is the compensations capacitor connected between V_G and AGND; I_{VG_DRV} is the driver charge current.

5.1.1.1.2 Electrical Parameter Control Voltage

Table 5.1.1.1.2-1: Gate Control Voltage at Pin V_G

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	NMOS gate voltage at pin V_G operating	V_{SUPPLY}=5.3V	V_{G_ON}	V_{BUS} + 4.5			V
2	NMOS gate voltage at pin V_G non operating	R_{DG}<=500kΩ between V_G and V_{SUPPLY}, 250µA current sink at pin V_{BUS} (source)	V_{G_OFF}			1	V
3	Pull down current in off condition		I_{VG_PD}	30	50	70	µA
4	Clamp voltage V_G - V_{BUS}*)		V_{GS_CLAMP}	7		13	V
5	Driver capability		I_{VG_DRV}	50	80	100	µA

*) Not tested in production

5.1.1.2 Charge Pump for Sync Voltage

Table 5.1.1.2-1: Electrical Parameter Table of the Charge Pump for SYNC Voltage

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Charge pump output voltage at pin CSYNC without load*)	I_{LOAD}=0mA	$V_{CSYNC\_no\_ld}$	2*V_{BUS} -1.35V		2*V_{BUS}	V
2	Charge pump output voltage at pin CSYNC in low power mode	V_{BUS}=5.05V; I_{LOAD}=25mA	V_{CSYNC_lp}	8.65		10.1	V
3	Charge pump output voltage at pin CSYNC in low power mode	V_{BUS}=5.05V; I_{LOAD}=28mA (7mA per SIFx)	V_{CSYNC_lp}	8.6		10.1	V
4	Charge pump output voltage at pin CSYNC in standard mode	V_{BUS}=6.45V; I_{LOAD}=28mA (7mA per SIFx)	V_{CSYNC_std}	11.35		12.9	V
5	Charge pump output voltage at pin CSYNC in increased mode	V_{BUS}=7.47V; I_{LOAD}=28mA (7mA per SIFx)	V_{CSYNC_inc}	13.34		14.94	V
6	Start-up time for voltage at pin CSYNC*)	Test condition: 80%*V_{SYNC} at $t_{START\_CP\_SYNC}$; without load at pin V_{SYNC};	$t_{START\_CP\_CSYNC}$			3	ms

*) Not tested in production

5.1.2 POR AND POWER-UP SEQUENCE

Table 5.1.2-1: Electrical Parameter Table of POR

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Power ON reset threshold value	Related to VDD	V_{POR_ON}	2.3		2.9	V
2	Power OFF reset threshold value	Related to VDD	V_{POR_OFF}	2.2		2.7	V
3	Power ON reset hysteresis*)		V_{POR_HYS}	0.1		0.3	V
4	Minimum time NRES=low*)		t_{NRES_LOW}	1		10	µs
5	Power ON reset delay time*) 1)	At power-up of V_{DD_INT}	$t_{POR\_D\_LH}$			50	µs

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
6	Power OFF reset delay time*)		$t_{POR\_D\_HL}$	0.5			µs
7	Input threshold NRES low*)		V_{NRES_low}	0.8			V
8	Input threshold NRES high*)		V_{NRES_high}			2	V
9	Pull down resistor NRES		$R_{NRES\_PULL\_DOWN}$	70	100	130	kΩ

*) Not tested in production
1) The output voltage of the internal VDD-regulator

5.1.3 PSI5 INTERFACE

5.1.3.1 Interface Driver

Table 5.1.3.1-1: Electrical Parameter Table of the Interface Driver

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Voltage at pin SIFx (x=1-4), low power mode*)	Low voltage mode; Test condition for V_{SIFX_min} measurement: V_{BUS}=5.05V; I_{SIFX_OP}=65mA and V_{BUS} is supplied directly	$V_{SIFx\_lp\_VBUS\_min}$	4.543		V_{BUS}	V
2	Voltage at pin SIFx (x=1-4), low power mode*)	Low voltage mode; V_{BUS}=4.6V..5.05V; Test condition for V_{SIFX_min} measurement: V_{BUS}=4.6V; I_{SIFX_OP}=25mA and V_{BUS} is supplied directly	V_{SIFx_lp}	4.405		5.05	V
3	Voltage at pin SIFx (x=1-4), common mode*)	Standard mode; Condition for V_{SIFX_min} measurement: V_{BUS}=6.45V; I_{SIFX_OP}=65mA and V_{BUS} is supplied directly	V_{SIFx_std}	5.943		V_{BUS}	V
4	Voltage at pin SIFx (x=1-4), common mode*)	Increased mode; Condition for V_{SIFX_min} measurement: V_{BUS}=7.47V; I_{SIFX_OP}=65mA and V_{BUS} is supplied directly	V_{SIFx_inc}	6.963		V_{BUS}	V
5	Resistance between pin V_{BUS} and pins SIFx	I_{SIFX_OP} =65mA, including temperature drift and long term drift	R_{VBUS_SIFx}	4.5		7.8	Ω

*) Not tested in production

5.1.3.2 Over Current Detection and Limitation

Table 5.1.3.2-1: Electrical Parameter Table of the Over Current Detection and Limitation

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Sensor interface current limitation		I_{LIM_SIFx}	-130	-100	-75	mA
2	Threshold value for detection of SCG "hard short"(low impedance to GND)*) 1)		I_{SIFx_HaSh}	200			mA
3	Activation time for over current limitation at pin SIFx at "hard short"*)		$t_{SIFx\_HaSh\_act}$			300	ns
4	Over current switch off delay*)		$t_{SIFx\_LIM\_act}$	491	544	566	µs
5	SIFx over current start up delay (default value:ASIC_CNFG_3:BL_CHANNEL_1-4=0000)*)		$t_{OC\_SIFx\_5ms}$	5.007	5.248	5.458	ms
6	SIFx over current start up delay(ASIC_CNFG_3:BL_CHANNEL_1-4=1111)*)		$t_{OC\_SIFx\_10ms}$	10.014	10.464	10.882	ms

*) Not tested in production
1) SCG:Short to GND

5.1.3.3 Reverse Current Detection and Limitation

5.1.3.3.1 Reverse Current Flow from SIFx to VBUS

Table 5.1.3.3.1-1: Electrical Parameter Table of the Reverse Current Detection and Limitation (Revese Current Flow from SIFx to VBUS)

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Reverse current into SIFx-pin in ON-state	equal to ΔV_{REV_TRIG} /$R_{VBUS-SIFx}$	$I_{SIFx\_REV\_ON}$			200	mA
2	Reverse current into SIFx-pin in OFF-state*)		$I_{SIFx\_REV\_OFF}$		1		mA
3	Threshold value for detection of the reverse current1)		$I_{SIFx\_REV\_THR}$	10	30	60	mA
4	Activation time for reverse protection at pins SIFx*)		$t_{SIFx\_REV\_act}$			500	ns
5	SIFx reverse current shut-off activation time (deglitcher)*)		$t_{SIFx\_REV\_CUR}$	61	96	100	µs

*) Not tested in production
1) $\Delta V_{REV\_TRIG}=V_{BUS}-V_{SIFx}$ in short to V_{BAT} condition

5.1.3.3.2 Reverse Current Flow from SIFx to CSYNC

Table 5.1.3.3.2-1: Electrical Parameter Table of the Reverse Current Detection and Limitation (Reverse Current Flow from SIFx to CSYNC)

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Threshold value for detection of the reverse current		$I_{CSYNC\_REV\_THR}$	-100		-4	mA

5.1.3.4 Data Comparator

Table 5.1.3.4-1: Electrical Parameter Table of the Data Comparator

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Data comparator threshold low->high transition	Low power mode	$I_{COMP\_th\_lp\_lh}$	-8.3	-6.3	-4.3	mA
2	Data comparator threshold high->low transition	Low power mode	$I_{COMP\_th\_lp\_hl}$	-7.7	-5.7	-3.7	mA
3	Data comparator threshold low->high transition	Common mode	$I_{COMP\_th\_com\_lh}$	-16.6	-12.6	-8.6	mA
4	Data comparator threshold high->low transition	Common mode	$I_{COMP\_th\_com\_hl}$	-15.4	-11.4	-7.4	mA
5	Data comparator hysteresis*)	Low power mode	$I_{COMP\_hys\_lp}$		0.6		mA
6	Data comparator hysteresis*)	Common mode	$I_{COMP\_hys\_com}$		1.2		mA
7	Data comparator filter time (deglitcher)*)	Manchester code pattern 125kbps; 2bit deglitcher; resolution 250ns;	$I_{DATA\_DGL\_lf}$	480	750		ns
8	Data comparator filter time (deglitcher)*)	Manchester code pattern 189kbps; 2bit deglitcher; resolution 167ns;	$I_{DATA\_DGL\_hf}$	320	500		ns

*) Not tested in production

5.1.3.5 Sync Pulse Generation

5.1.3.5.1 Sync Pulse Generation DC-Parameter

Table 5.1.3.5.1-1: Sync Pulse Generation DC-Parameter

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Sync slope reference voltage*)	Referenced to V_{SIFx}; t2 defined by V_{t2}	V_{t0}		0.5		V
2	Lower boundary of sync signal sustain voltage*)	Low power mode; Referenced to V_{SIFx}; t2 defined by V_{t2}	V_{t2_lp}		2.5		V
3	Lower boundary of sync signal sustain voltage*)	Common mode; Referenced to V_{SIFx};	V_{t2_com}		3.5		V
4	Upper boundary of sync signal sustain voltage	Low power mode	V_{t3_lp}	$2.7+V_{S\ IFX}$	$3.7+V_{S\ IFX}$	$4.3+V_{S\ IFX}$	V
5	Upper boundary of sync signal sustain voltage	Common mode	V_{t3_com}	$4.2+V_{S\ IFX}$	$4.8+V_{S\ IFX}$	$5.5+V_{S\ IFX}$	V
6	Ripple of voltage V_{t3} (supply rejection between pins CSYNC and SIFx)*)	Test condition: t=close to end of short sync signal =>t=t0+15µs;	$V_{t3\_rippple}$			100	mV_{PP}
7	Current limitation during Sync pulse slope*)		I_{CSYNC_LMT}	-210.0	-150.0	-110.0	mA
8	CSYNC voltage drop between pin CSYNC and SIFx		V_{CSYNC_DR}			0.8	V

*) Not tested in production

5.1.3.5.2 Sync Pulse Generation AC Parameter

Table 5.1.3.5.2-1: Sync Pulse Generation AC-Parameter

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Sync slope rising slew rate	Transition from V_{t0} to V_{t2}; 24nF<=C_{BUS}<=107nF; 4mA<=I_{SIFx}<=35 mA	SR_{rise}	0.43		1.5	V/µs
2	Sync slope falling slew rate	Transition from V_{t2} to V_{t0}; 24nF<=C_{BUS}<=107nF; 4mA<=I_{SIFx}<=35 mA	SR_{fall}	-1.5			V/µs
3	Reference time for Sync slope*) 1)	Reference time base defined at V_{t0}	t_0		0		µs
4	Sync signal earlist start*) 1)		t_1	-1			µs
5	Sync signal sustain time*) 1)	Short sync pulse	t^0_3	16			µs
6	Sync signal sustain time*) 1)	Long sync pulse	t^1_3	43			µs
7	Discharge time limit*) 1)	Short sync pulse	t^0_4			35	µs
8	Discharge time limit*) 1)	Long sync pulse	t^1_4			62	µs
9	Minimum idle time of Tx_LEN counter*)		$t_{Tx\_LEN\_IDLE}$	32			µs

*) Not tested in production
1) see timing diagram Figure 6.1.3.6-1

5.1.3.6 Sync Pulse Generation by Pin TRIG

Table 5.1.3.6-1: Trigger via Pin TRIG

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Schmitt-Trigger - low input level at pin TRIG		V_{SMT_L}	0.8			V
2	Schmitt-Trigger - high input level at pin TRIG		V_{SMT_H}			2	V
3	Trigger pulse at pin TRIG - short SYNC pulse*)	70% of rising slope to 30% of falling slope	$t_{trig\_sh\_pulse}$	10	15	20	µs
4	Trigger pulse at pin TRIG - long SYNC pulse*)	70% of rising slope to 30% of falling slope	$t_{trig\_lng\_pulse}$	40	45	50	µs
5	Trigger pulse rise and fall*)	Transition from 20% to 80% (and vice versa);	$t_{trig\_RI/RA}$		50		ns
6	Trigger pulse filter time*)	3bit deglitcher; resolution 1µs	t_{DGL_trig}	4.72	5	5.2	µs
7	Delay counter to distinguish between short/long SYNC pulse*)		t_{DLY}		30		µs

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
8	SYNC pulse delay timer*)	step size = 2µs; configuration via UART/SPI with 10bit	t_{SYNC_DLY}	0		$8/f_{CLK\_INT}*(2^{10}-1)$	µs
9	SYNC pulse delay from counter*)		$t_{SYNC\_DLY\_CNT}$		$32/f_{CLK\_INT}$		µs
10	Time between two sync pulses on different SIFx channels*)		t_{SYNC_REP1}	0			µs
11	Sync pulses repetition time on the SIFx channel*)	limited if charge pump is used; Applies for I_{SIFx_Q} =4...-19mA (standard current)	$t_{SYNC\_REP2\_std}$	200			µs
12	Sync pulses repetition time on the SIFx channel*)	limited if charge pump is used; Applies for I_{SIFx_Q} =4...-35mA (extended current)	$t_{SYNC\_REP2\_ext}$	300			µs
13	Pull down resistor pin TRIG, applies for voltage VTRIG<3.3V		$R_{TRIG\_PULL\_DOWN}$	70	100	150	kΩ
14	Pull down current pin TRIG, applies for voltage VTRIG>3.3V		$I_{TRIG\_PULL\_DOWN}$	10		60	µA

*) Not tested in production

5.1.4 CLOCK GENERATION

Table 5.1.4-1: Electrical Parameter Table of the Internal Oscillator

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Internal oscillator clock frequency1)		f_{CLK_INT}	11.52	12.00	12.48	MHz
2	Duty cycle of f_{CLK_INT}*)		DC_{CLK_INT}	40		60	%

*) Not tested in production
1) trimmed

5.1.5 DIAGNOSIS

5.1.5.1 ADC Voltage Measurements

Table 5.1.5.1-1: Electrical Parameter Table of the ADC.

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Positive reference voltage		V_{REFH}	2.6	2.7	2.75	V
2	Offset measurement of V_{BUS} diagnosis voltage of ADC output	V_{BUS}=4.6V .. 11V	V_{BUS_Offset}	-450		250	mV
3	Gain measurement of V_{BUS} diagnosis voltage of ADC output	V_{BUS}=4.6V .. 11V	V_{BUS_Gain}	0.94	1	1.06	V_{BUS}
4	Offset measurement of V_{CSYNC} diagnosis voltage of ADC output	V_{CSYNC}=8V .. 33V	V_{CSYNC_Offset}	-1.8		1.4	V
5	Gain measurement of V_{CSYNC} diagnosis voltage of ADC output	V_{CSYNC}=8V .. 33V	V_{CSYNC_Gain}	0.85	1	1.15	V_{CSYNC}

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
6	Offset measurement of VDD diagnosis voltage of ADC output	VDD=3.0V .. 5.5V	VDD_{Offset}	-400		200	mV
7	Gain measurement of VDD diagnosis voltage of ADC output	VDD=3.0V .. 5.5V	VDD_{Gain}	0.93	1	1.07	VDD
8	Offset measurement of V_{SIFX} diagnosis voltage of ADC output	V_{BUS}=4.6V .. 11V	V_{SIFX_Offset}	-450		250	mV
9	Gain measurement of V_{SIFX} diagnosis voltage of ADC output	V_{BUS}=4.6V .. 11V	V_{SIFX_Gain}	0.94	1	1.06	V_{BUS}
10	Measurement of V_{CP_LDO} diagnosis voltage of ADC output	$V_{SUPPPLY}$=5.3V,V_{BUS}=7V	V_{CP_LDO}	10.2	12.2	14.2	V
11	Measurement of V_{CP_LDO} diagnosis voltage of ADC output	$V_{SUPPPLY}$=6.95V,V_{BUS}=7V	V_{CP_LDO}	12.2	14.2	16.2	V
12	Measurement of V_{CP_LDO} diagnosis voltage of ADC output	$V_{SUPPPLY}$=8V,V_{BUS}=7V	V_{CP_LDO}	13.2	15.2	17.2	V
13	Measurement of V_{DD_INT} diagnosis voltage of ADC output	VDD=3.3V	V_{DD_INT}	3.0	3.2	3.4	V
14	Measurement of V_{DD_INT} diagnosis voltage of ADC output	VDD=5V	V_{DD_INT}	3.0	3.2	3.4	V

5.1.5.2 Over Temperature Monitoring (OT)

Table 5.1.5.2-1: Electrical Parameter Table of the Over temperature Sensing:

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Junction temperature threshold value; low->high transition*)		T_{J_HI}	154	165	174	℃
2	Junction temperature threshold value; high->low transition*)		T_{J_LI}	145	155	165	℃
3	Junction temperature hysteresis*)		T_{J_HYS}		10		℃
4	Over temperature filter time (deglitcher)*)		t_{OT}		8.1		ms

*) Not tested in production

5.1.5.3 V_{BUS} Over Voltage Monitoring

Table 5.1.5.3-1: VBUS over voltage monitoring

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	V_{BUS} over voltage comparator - threshold value		$V_{BUS\_OV\_THR}$	11.8		13	V
2	V_{BUS} over voltage comparator - hysteresis*)		$V_{BUS\_OV\_HYS}$	0.5			V
3	V_{BUS} over voltage filter time (deglitcher)*)		t_{VBUS_OV}	61	96	100	µs

*) Not tested in production

5.2 DIGITAL PART

5.2.1 SPI

5.2.1.1 DC Electrical Parameter Table of SPI IOs

Table 5.2.1.1-1: DC Electrical Parameter Table of the Digital Inputs and Outputs

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Input threshold low SDI_RXD, NCS,SCLK		V_{THDIG_L}	0.8			V
2	Input threshold high SDI_RXD, NCS,SCLK		V_{THDIG_H}			2	V
3	Output voltage SDO_TXD low	$I_{SDO\_TXD\_L}$=3.2mA	$V_{SDO\_TXD\_L}$			0.4	V
4	Output voltage SDO_TXD high	$I_{SDO\_TXD\_H}$=-2mA	$V_{SDO\_TXD\_H}$	V_{DD}-0.4V		V_{DD}	V
5	Pull Up resistor NCS		$R_{NCS\_PULL\_UP}$	70	100	130	kΩ
6	Pull Up resistor RXD		$R_{SDO\_RXD\_PULL\_UP}$	70	100	130	kΩ

5.2.1.2 AC Electrical Parameter Table of SPI I/Os

Table 5.2.1.2-1: Electrical Parameter Table of SPI

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	SPI frequency*)		f_{SCLK}	0		5	MHz
2	SDO_TXD rise and fall time*)	20pF...150pF load	t_{sdo_trans}	5		35	ns
3	Minimum time CLK=LOW*)		t_{clh}	75			ns
4	Minimum time CLK=HIGH*)		t_{cll}	75			ns
5	Propagation delay (SCLK to data at SDO active)*)	150pF load; from SCLK=2.3V to SDO=0.5*V_{DD_SUP}, applies for 3.3V/5V;	t_{pcld}			50	ns
6	NCS low to output SDO active*)	150pF load	t_{csdv}			75	ns
7	SCLK low before NCS low (setup time SCLK to NCS change H/L)*)		t_{sclch}	75			ns
8	SCLK change L/H after NCS=low*)		t_{hclcl_app}	600			ns
9	SDI input setup time (SCLK change H/L after SDI data valid)*)		t_{scld}	15			ns
10	SDI input hold time (SDI data holdafter SCLK change H/L)*)		t_{hcld}	15			ns
11	SCLK low before NCS high*)		t_{sclcl}	100			ns
12	SCLK high after NCS high*)		t_{hclhc}	100			ns
13	NCS L/H to SDO@high impedance*)		t_{pchdz}			75	ns
14	NCS min. high time between two consecutive commands*)		t_{on_NCS}	700			ns
15	NCS filter time*)		t_{fNCS}	10		40	ns

*) Not tested in production

6 Functional Description

6.1 ANALOG PART

6.1.1 SUPPLY

Various supply voltage concepts are supported by the device due to the various possible applications. The device is supplied via the pin V_{SUPPLY} with an appropriate voltage. This voltage supplies an external transistor that is driven by an internal LDO via the pin V_G. The output of the external transistor is fed back via the pin V_{BUS} to the LDO control block.

If an external NMOS transistor is used, the internal error amplifier has to be compensated with an external compensation capacitor C_K connected between V_G and AGND. For low supply voltages V_{BUS} on the ECU, the ASIC can be supplied directly at pin VBUS with the voltage provided by V_{SUPPLY}, when no voltage drop between the pins V_{SUPPLY} and V_{BUS} can be accepted. In this case the LDO must be disabled.
The voltage V_{CSYNC} , which is necessary for providing the sync pulse is generated in the block CHARGE PUMP FOR SYNC VOLTAGE (CP). The voltage V_{CSYNC} is available at the pin CSYNC. Alternatively, the CSYNC voltage can be supplied directly at the pin CSYNC with external voltage V_{CSYNC}. The V_{CSYNC} charge pump must be disabled in this case. The following table gives an overview of possible supply voltage concepts, which can be chosen via SPI or UART commands.

Table 6.1.1-1: Overview Supply Voltage Concepts

Config Options	***V_{DD}***	***V_{SUPPLY}***	***V_{BUS}***	***V_{CSYNC}***	***LDO enabled***	***CP enabled***
A	VDD supplied directly	V_{SUPPLY} supplied directly	Generated by LDO	Generated by charge pump	YES	YES
B	VDD supplied directly	V_{SUPPLY} supplied directly	Generated by LDO	V_{SYNC} supplied from ECU	YES	NO
C	VDD supplied directly	N.A.	V_{BUS} supplied directly	Generated by charge pump	NO	YES
D	VDD supplied directly	N.A.	V_{BUS} supplied directly	V_{SYNC} supplied from ECU	NO	NO

6.1.1.1 LDO Control Block

A low drop out regulator (LDO) with external NMOS and compensation capacitor C_K is implemented to generate a stable V_{BUS} voltage out of the input voltage V_{SUPPLY}. A LDO control circuit is implemented to drive the external NMOS transistor. Three voltage levels for V_{BUS} are configurable via bit combination ASIC_CNFG_1[V_BUS] (see description of register ASIC_CNFG_1 for details). The LDO control circuit is disabled by default value ASIC_CNFG_1[V_BUS]="00". The voltage loop has be to compensated with an external compensation capacitor C_K at pin V_G for stability reasons. The LDO charge pump provides an appropriate voltage V_{CP_GATE} for control of the external NMOS transistor at pin V_G. A gate source voltage clamping to the voltage V_{GS_CLMP} is implemented.

6.1.1.2 Charge Pump for Sync Voltage

A charge pump is used to generate the SYNC pulse voltage from the voltage VBUS. The charge pump consists of two external capacitors, the fly capacitor CP connected to pins CP1 and CP2, the storage capacitor CSYNC connected to pin CSYNC, two diodes and two high voltage switches inside the IC. The charge pump is configurable via bit ASIC_CNFG_3[EN_CP_SYNC] (see description of register ASIC_CNFG_3).

- EN_CP_SYNC='0' means disabled
- EN_CP_SYNC='1' means enabled

The charge pump circuit is disabled for the asynchronous mode. If the charge pump is not used, then it is not allowed to connect the pin CSYNC with ground. The diode path from V_{BUS} to C_{SYNC} will result in high current and destruction of IC.

6.1.2 POR AND POWER-UP SEQUENCE

The POR-block observes the voltages V_{DD_INT}, V_{ANA}, NRES, V_{AGND} and V_{PGND}. It generates the POR-signal. During the power up time, the following actions take place:

- The voltage regulators V_{DD_INT} and V_{ANA} provide the voltage V_{DD_INT} and V_{ANA}
- The bandgap/biasing block provides the voltage V_{BG} and the bias
- The internal oscillator starts up and provides a stable clock frequency for the digital part After power-up time, the rising edge of the NRES determines the interface mode (SPI/UART), depending on the state of the pin NCS. When NCS is LOW the UART interface is selected. When NCS is HIGH the SPI is chosen. During the power up time is not allowed to change the logic level of NRES.

6.1.3 PSI5 INTERFACE

6.1.3.1 Interface Driver

Each of the four interfaces provide a voltage V_{SIFx} and a current I_{SIFx} for the connected satellite sensors by "switching" voltage V_{BUS} to the pin SIFx via internal transistor switches and shunt. The interfaces are short-circuit protected to V_{BAT} and GND. The four interfaces operate independent from each other. The interfaces can be en-/disabled via an UART/SPI command with the bits EN_CHx , described in register ASIC_CNFG_3. The default state of the interface is disabled. The current sensing block includes an I_{BASE} tracking function and the DATA-comparator.

Any time a channel is enable by [EN_CHx], a blanking time is started. During this delay time $t_{SIFx\_BLANKING}$, the Manchester decoder, SYNC pulse generator and overcurrent filter time t_{OC_SIFx} are disabled.
No channel enable possible if following error bits are set to '1':

- ERROR_STATUS_1[VBUS_OV]
- ERROR_STATUS_x[REV_CUR_CHx] if REV_CUR_CH_DIS='1'
- ERROR_STATUS_x[OC_CHx]
- ERROR_STATUS_1[DIAG_OT]

6.1.3.2 Over Current Detection and Limitation

The circuit provides an over current limitation and protection of the interfaces. The current limitation for I_{SIFx} is implemented with a voltage measurement over the shunt resistor R_{SH} and with the control of the transistor T2. If the current I_{SIFx} exceeds the threshold current I_{LMT_SIFx}, the comparator output signal $i_{sifx\_oc\_det}$ is set to high. This signal is filtered in the digital block by a deglitcher with the filter time $t_{SIFX\_LIM\_act}$, latched in the register ERROR_STATUS_x[OC_CHx] and the appropriate channel is disabled ,that means the affected EN_CHx bits are reset by the device automatically. To switch on the channel again it is essential to read out the appropriate error register ("clear on read"). To ensure proper over current detection, the threshold value for overcurrent limitation is higher than the over current detection threshold.
In order to avoid over current switch off during start up (enable of channels), a blanking time of $t_{OC\_SIFX\_5ms}$ resp. $t_{OC\_SIFX\_10ms}$ is implemented. During this time the over current switch off is disabled. The blanking time can be programmed in the Register ASIC_CONFG_3 BL_ChannelX.

6.1.3.3 Reverse Current Detection and Limitation

The IC provides two different paths of the reverse current protection:

- from pin SIFx to pin VBUS
- from pin SIFx to pin CSYNC

6.1.3.3.1 Reverse Current Flow from SIFx to VBUS

The circuit provides the reverse current detection from SIFx pin to VBUS pin. The reverse current detection is implemented with a voltage measurement over the shunt resistor R_{SH} (like described in the chapter Over current Detection). If a reverse current is detected the comparator output signal will be set to high. The signal will be deglitched and latched in the register ERROR_STATUS_x[REV_CUR_CHx]. The affected channel will be disabled if configuration bit ASIC_CNFG_2 [REV_CUR_CH_DIS] is set to high and the affected EN_CHx bits are reset by the device automatically.
To switch on the channel again it is essential to read out the appropriate error register ("clear on read").

6.1.3.3.2 Reverse Current Flow from SIFx to CSYNC

The circuit provides the reverse current detection from pin SIFx to pin CSYNC. The reverse current detection is implemented with a MOS-transistor. The reverse current protection circuit stops the reverse current from SIFx pin to CSYNC pin when SIFx becomes higher then CSYNC.

6.1.3.4 Quiescent Current Threshold Tracking

The quiescent current of the circuit is measured and adapted continously during during operation, to avoid corrupted data transmission because of drift or aging processes.

6.1.3.5 Data Comparator

The satellite sensors modulate the current in order to realize a Manchester coded data transmission.
The "low" level of the current is represented by the quiescent current $I_{SAT\_Q\_range}$ of the sensor, while a "high" level is created by switching on a current sink to the line, which increases the current to I_{SAT_OP}.
A current transition in the middle of the bit time represents the logical value of the transferred data. A "high current-low current" transition stand for a logical '1', a "low current-high current" transition for a logical '0'.
This current can be detected by measuring the voltage drop via an internal shunt. The current threshold is automatically adapted to the quiescent current of the sensors.
The threshold value is configured with register ASIC_CNFG_1[ΔIs_CHx] with 1bit per SIFx (changed individually). The default value is ΔIs='0' (common mode). ΔIs='1' means the threshold value for low power mode is choosen (see register description of ASIC_CNFG1).

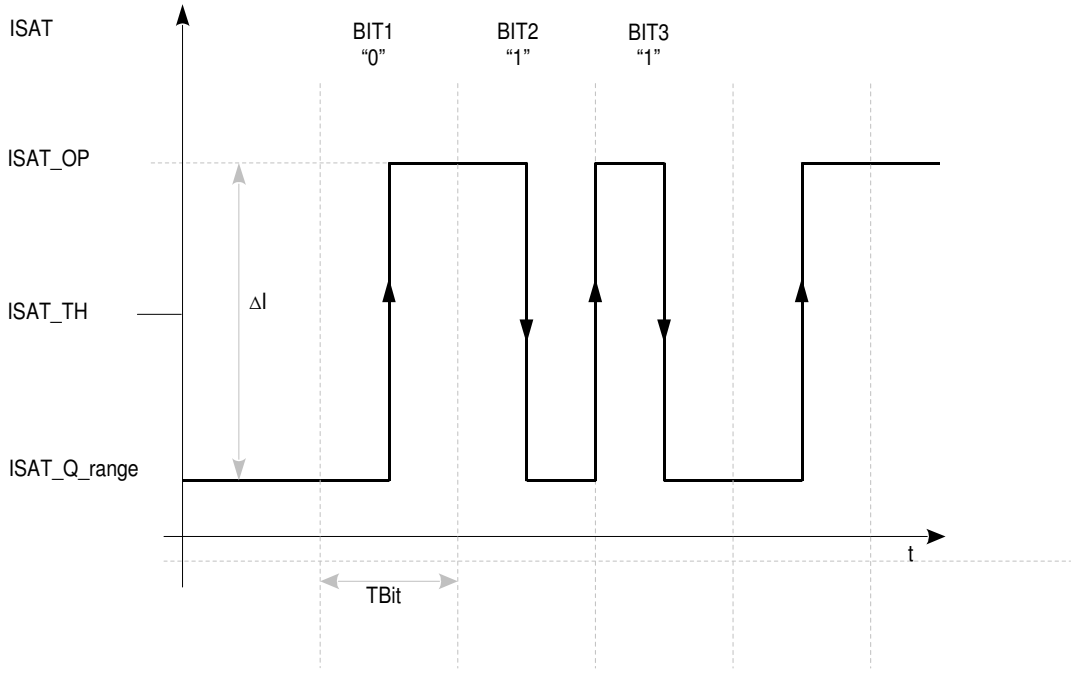


Figure 6.1.3.5-1: Current Modulation

6.1.3.6 Sync Pulse Generation

For PSI5 synchronous mode, the IC generates the SYNC pulse to synchronize the sensors. During SYNC pulse the voltage level at pins SIFx will be increased for a defined time and then decreased before the sensor to ECU communication (current modulation) starts. The SYNC pulse is shaped to limit emissions. The SYNC voltage is either generated by SYNC pulse charge pump or supplied from external via pin CSYNC.
The voltage level Vt3 is configured with the register ASIC_CNFG_1[VSYNC_V3_CHx] with 1 bit per SIFx (channel individually).
The IC provide a reverse protection for the short circuit to the battery at the interfaces and current limitation of the SYNC pulse. The current limitation is active during SYNC sustain time only. The current limitation is disabled during rising/falling slope to guarantee slope at max. load.
There are two ways to generate an event triggered SYNC pulse:

- by trigger voltage pulse at pin TRIG
- by UART/SPI command

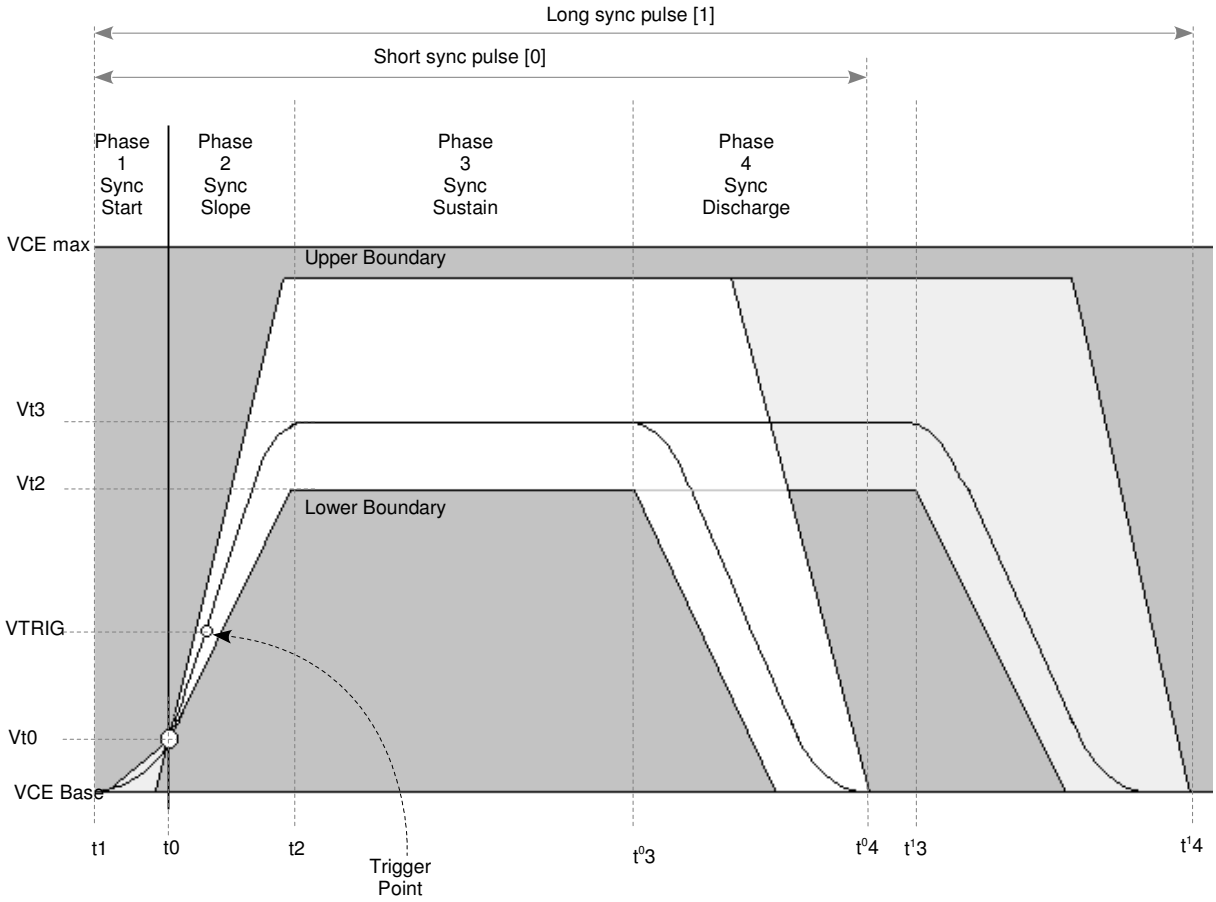


Figure 6.1.3.6-1: Sync Pulse Timing Diagram

6.1.3.7 Sync Pulse Generation by Pin TRIG

Following diagram shows the timing requirements for the trigger voltage pulse at pin TRIG with:

- high time $t_{trig\_sh\_pulse}$ for a short SYNC pulse
- high time $t_{trig\_lo\_pulse}$ for a long SYNC pulse

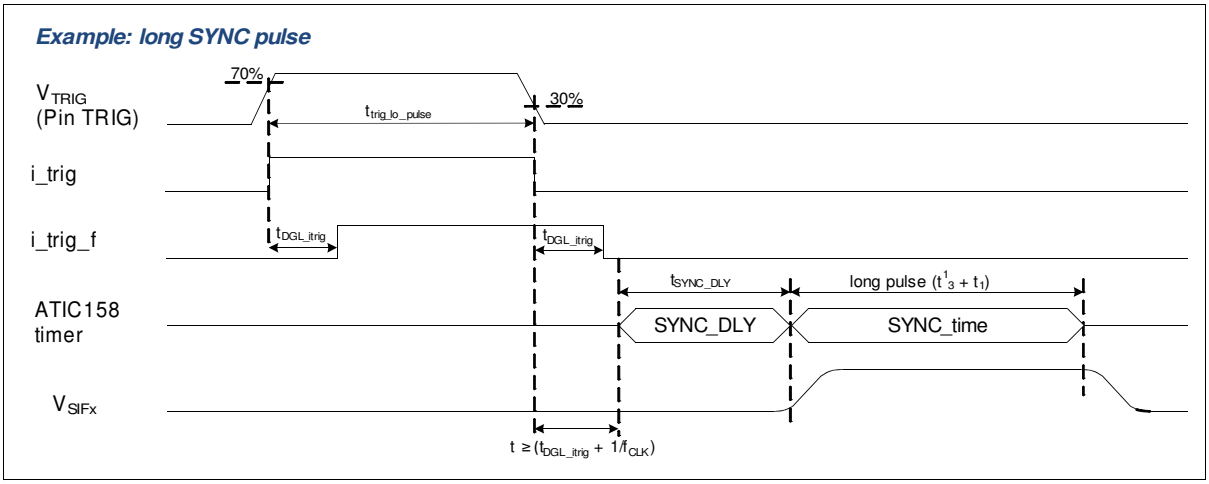


Figure 6.1.3.7-1: Long SYNC Pulse Trigger via Pin TRIG

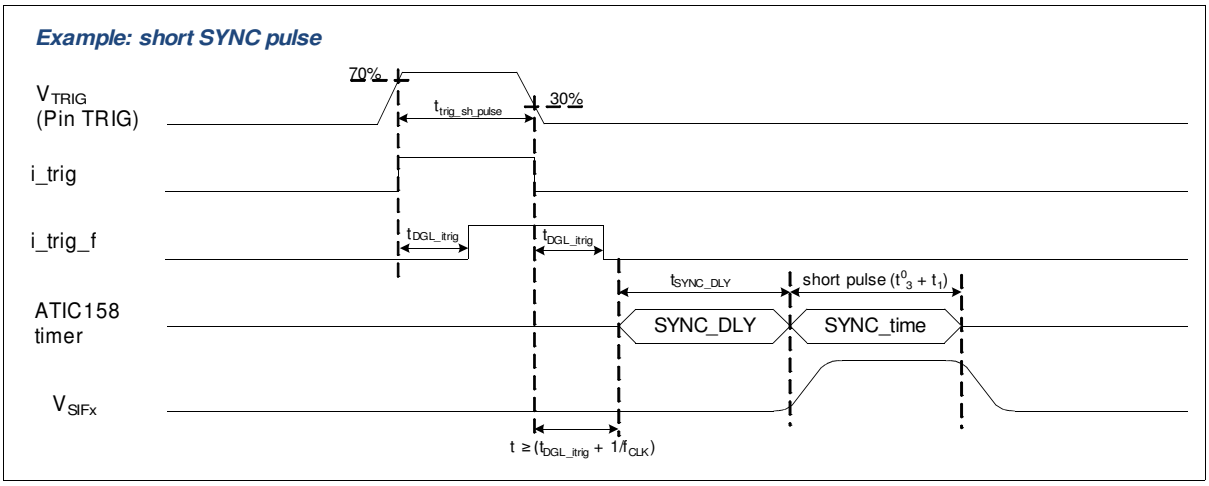


Figure 6.1.3.7-2: Short SYNC Pulse Trigger via Pin TRIG

6.1.3.8 Sync Pulse Generation by UART/SPI Command

Following timing diagrams show the SYNC pulse generation triggered by a UART or SPI command.

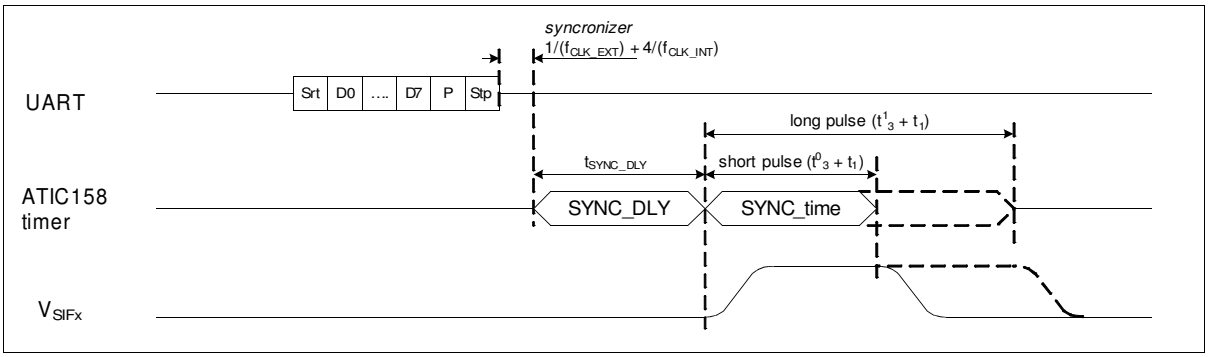


Figure 6.1.3.8-1: Short SYNC Ptrigger via UART

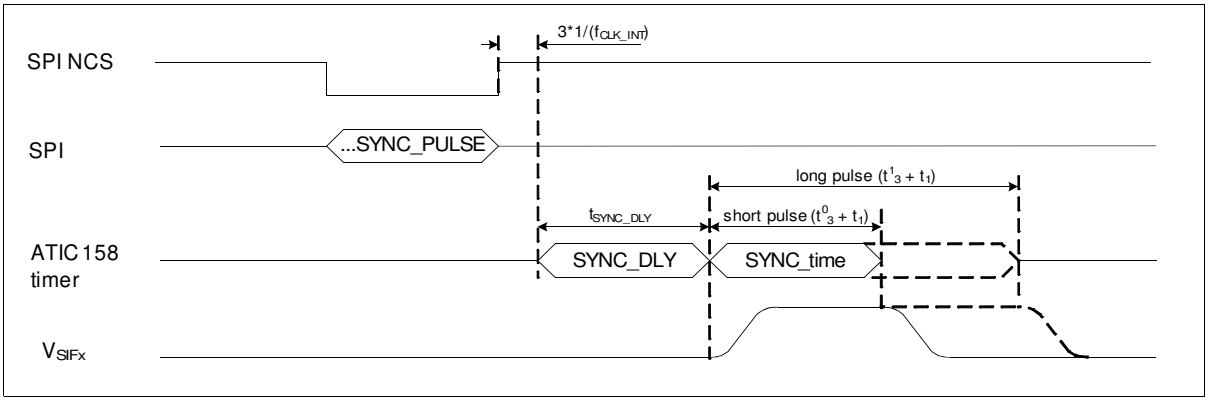


Figure 6.1.3.8-2: Short SYNC Pulse Trigger via SPI

6.1.4 CLOCK GENERATION

The internal oscillator is the central clock source for the digital part and provides the clock signal required for the internal charge pumps. The oscillator starts up automatically as soon as V_{DD_INT} and V_{ANA} are stable.

An external clock has to be supplied via pin SCLK for UART communication. The ratio between external clock and UART baud rate is 5/1 (= 5 times oversampling for UART telegrams on SDI_RXD).

6.1.5 DIAGNOSIS

6.1.5.1 ADC Voltage Measurements

Several voltage levels can be measured by the ASIC with an analog-digital converter for diagnostic purposes. The digital values will be written into status registers after conversion. These registers can be read out by the micro controller via UART/SPI.

An 8-bit ADC (Successive Approximation Register concept) is implemented for diagnosis purposes. In total 9 internal voltages are measured sequentially in a repeating (endless) loop. The measurement of one voltage is called a cycle.

Steps within a cycle:
- Voltage is selected via MUX
- ADC conversion is performed
- Data is transferred into register DIAGNOSIS_ADC_1_2 to DIAGNOSIS_ADC_9_10

One sequence is performed within t_{CYC}. Each measured voltage is stored in a dedicated register. The update rate of the register values is given by number of voltages multiplied with cycle time -> 9 x t_{CYC}.The ADC sequence starts with release of reset automatically. For *synchronous mode* the values at "pin SIFx" can vary between V_{SIFx} and V_{t3}, depending whether a SYNC pulse was generated during conversion time or not. For *asynchronous mode* the voltage at pin SIFx is measured properly.

The following table shows the voltage divider ratio of the different voltages.

Table 6.1.5.1-1: Voltage Divider Ratio

Voltage	***Divider ratio***
V_{BUS}	1/5
V_{SYNC}	1/13
V_{CP_GATE}	1/7
V_{SIFx}	1/5
V_{DD_INT}	1/2
V_{DD}	1/3

6.1.5.2 Over Temperature Monitoring (OT)

chThe junction temperature is monitored with a temperature sensor to detect excessive temperature levels. If the junction temperature exceeds T_{J_HI} then following protection actions will be processed automatically:
- All SIFx will be disabled -> reset bit ASIC_CNFG_3[EN_CHx]='0'
- The affected EN_CHx bits are reset by the device automatically. To switch on the channel again it is essential to read out the appropriate error register ("clear on read").
- SYNC pulse charge pump will be disabled -> reset bit ASIC_CNFG_3[EN_CP_SYNC]='0'
- over temperature event is latched in status register ERROR_STATUS_1[DIAG_OT] after t_{OT} (clear on read)
- With read of ERROR_STATUS_1[DIAG_OT], the filter timer for t_{OT} is reseted (deglitcher reset), independently of the current error status.
- If the read cycle of ERROR_STATUS_1[DIAG_OT] is shorter than t_{OT}, the ERROR_STATUS_1[DIAG_OT] bit will never be set.
- The channel will not be enabled automatically, if the error condition disappears.

6.1.5.3 V_{BUS} Over Voltage Monitoring

A comparator for V_{BUS} over voltage monitoring is implemented to avoid any damage of PSI5 sensors by exceeding their input voltage range.
If VBUS exceeds the value of $V_{BUS\_OV\_THR}$ then following protection actions are processed automatically:

- All SIFx will be disabled -> reset bit ASIC_CNFG_3[EN_CHx]='0'
- The affected EN_CHx bits are reset by the device automatically. To switch on the channel again it is essential to read out the appropriate error register ("clear on read").
- SYNC pulse charge pump will be disabled -> reset bit ASIC_CNFG_3[EN_CP_SYNC]='0'
- The over voltage event is latched in status register ERROR_STATUS_1[VBUS_OV] after t_{VBUS_OV} (clear on read)
- With read of ERROR_STATUS_1[VBUS_OV], the filter timer for t_{VBUS_OV} is reseted (deglitcher reset), independently of the current error status.
- If the read cycle of ERROR_STATUS_1[VBUS_OV] is shorter than t_{VBUS_OV}, the ERROR_STATUS_1[VBUS_OV] bit will never be set.
- The channel will not be enabled automatically, if the error condition disappears.

6.1.5.4 Leakage to GND, Leakage to V_{BAT} and Open Load

The detection of leakage To GND, leakage to VBAT and open load are implemented in the digital logic, based on the Ibase tracking function.
The digital counter for I_{BASE} indicates a leakage to GND for high counter values (high quiescent current) and the actual state is latched in status register ERROR_STATUS_x[DIAG_CHx].
For low counter values either a leakage to V_{BAT} or an open load condition is indicated (low or no quiescent curret).
The actual state is latched in status register ERROR_STATUS_x[DIAG_CHx].
The differentiation of leakage to V_{BAT} / open load failure has to be done by the micro controller
via the status of reverse current protection ERROR_STATUS_x[REV_CUR_CHx]

- Reverse current protection not active [REV_CUR_CHx]='0' -> Open Load
- Reverse current protection active [REV_CUR_CHx]='1' -> Leakage to VBAT or via ADC voltage measurement at pins SIFx (if flag [REV_CUR_CHx]='0'),
- $V_{SIFx} = V_{BUS}$ -> Open Load
- $V_{SIFx} > V_{BUS}$ -> Leakage to VBAT

6.1.5.5 GND Loss Detection

A comparator for GND loss detection is implemented to detect missing GND connections.
A detected GND loss results in a reset of the IC.
Following GNDs will be monitored:

- AGND
- PGND

6.1.5.6 Transfer of Error- and Diagnosis Information to µController

6.1.5.6.1 Error Information

All error analog/digital information are flagged in status registers ERROR_STATUS_1 ... ERROR_STATUS _10.
Every error is latched and is cleared by a read request by SPI or UART.

An overall error information is transmitted to the micro controller, included in some frames (see below) within bits Err[1:0]. For detailed error information the dedicated status registers shall be read.

- UART: Bits Err[1:0] included in header (UART frame1)
- SPI: Bits Err[1:0] included in the first response frame (SPI frame2)

The error information, bits Err[1:0], are transmitted in following messages to the micro controller:

- **UART**
  - Response to Read Command
  - Transfer PSI5 Data
- **SPI**
  - Responses to commands "cmd_get data_xxbit"

These responses allows the µController to know which kind of an error occurred.

(All interface errors, shown in the table below, are flagged in registers ERROR_STATUS_3 to ERROR_STATUS_10.
Register ERROR_STATUS_2 includes an OR-combination of all interface errors, one bit per channel.
E.g. ERROR_STATUS_2[0] includes the OR-combination of bits in registers ERROR_STATUS_3 and ERROR_STATUS_4 (=error information of channel 1).)

For detailed information see register table.

Note:
It is recommended to read out register ERROR_STATUS_2 if bit **Err[0] (interface error)** is set in a response of the transceiver to determine which channels are affected. In register ERROR_STATUS_2 the four LSBs [3:0] belongs to channel 4, channel 3, channel 2 and channel 1 and the appropriate channel bit is set in case of an interface error on the affected channel.
Afterwards the micro controller shall read the dedicated registers ERROR_STATUS_3 .. ERROR_STATUS_10 (depend of the affected channels) to get the detailed error information. There are two detailed error registers available per channel.
If bit **Err[1] (asic error)** is set in a message to the micro controller register ERROR_STATUS_1 shall be read for more information.
It is not recommended to read out the appropriate ERROR_STATUS_X with a cycle time of less than 9ms.

Table 6.1.5.6.1-1: Overview of Possible Error Information

TYPE OF ERROR	*ASIC*	*INTERFACE CH1-CH4*	*FRAME 1-6*	*ERROR STATUS REGISTER*	*ERROR BIT FLAG*
UART parity error. ASIC	x			ERROR_STATUS_1[0]	Err[1]
UART framing error (invalid stop bit). ASIC	x			ERROR_STATUS_1[1]	Err[1]
UART/SPI invalid command received. ASIC	x			ERROR_STATUS_1[2]	Err[1]
UART/SPI collision. ASIC	x			ERROR_STATUS_1[3]	Err[1]
SPI clock error. ASIC	x			ERROR_STATUS_1[4]	Err[1]
over temperature shut down. ASIC	x			ERROR_STATUS_1[5]	Err[1]
V_{BUS} overvoltage. ASIC	x			ERROR_STATUS_1[6]	Err[1]
MCD CRC/Parity Error. Interface		x	x	Ch1: ERROR_STATUS_3[0]/[4]/[8]/[12], ERROR_STATUS_4[0]/[4] Ch2: ERROR_STATUS_5[0]/[4]/[8]/[12], ERROR_STATUS_6[0]/[4] Ch3: ERROR_STATUS_7[0]/[4]/[8]/[12], ERROR_STATUS_8[0]/[4] Ch4: ERROR_STATUS_9[0]/[4]/[8]/[12], ERROR_STATUS_10[0]/[4]	Ch1: ERROR_STATUS_2[0] Ch2: ERROR_STATUS_2[1] Ch3: ERROR_STATUS_2[2] Ch4: ERROR_STATUS_2[3]

TYPE OF ERROR	ASIC	INTERFACE CH1-CH4	FRAME 1-6	ERROR STATUS REGISTER	ERROR BIT FLAG
MD framing error (frame too long(short, MC code violation, compensation window violation). Interface		x	x	Ch1: ERROR_STATUS_3[1]/[5]/[9]/[13], ERROR_STATUS_4[1]/[5] Ch2: ERROR_STATUS_5[1]/[5]/[9]/[13], ERROR_STATUS_6[1]/[5] Ch3: ERROR_STATUS_7[1]/[5]/[9]/[13], ERROR_STATUS_8[1]/[5] Ch4: ERROR_STATUS_9[1]/[5]/[9]/[13], ERROR_STATUS_10[1]/[5]	Ch1: ERROR_STATUS_2[0] Ch2: ERROR_STATUS_2[1] Ch3: ERROR_STATUS_2[2] Ch4: ERROR_STATUS_2[3]
MD no frame received. Interface		x	x	Ch1: ERROR_STATUS_3[2]/[6]/[10]/[14], ERROR_STATUS_4[2]/[6] Ch2: ERROR_STATUS_5[2]/[6]/[10]/[14], ERROR_STATUS_6[2]/[6] Ch3: ERROR_STATUS_7[2]/[6]/[10]/[14], ERROR_STATUS_8[2]/[6] Ch4: ERROR_STATUS_9[2]/[6]/[10]/[14], ERROR_STATUS_10[2]/[6]	Ch1: ERROR_STATUS_2[0] Ch2: ERROR_STATUS_2[1] Ch3: ERROR_STATUS_2[2] Ch4: ERROR_STATUS_2[3]
MD unexpected frame. Interface		x	x	Ch1: ERROR_STATUS_3[3]/[7]/[11]/[15], ERROR_STATUS_4[3]/[7] Ch2: ERROR_STATUS_5[3]/[7]/[11]/[15, ERROR_STATUS_6[3]/[7] Ch3: ERROR_STATUS_7[3]/[7]/[11]/[15, ERROR_STATUS_8[3]/[7] Ch4: ERROR_STATUS_9[3]/[7]/[11]/[15, ERROR_STATUS_10[3]/[7]	Ch1: ERROR_STATUS_2[0] Ch2: ERROR_STATUS_2[1] Ch3: ERROR_STATUS_2[2] Ch4: ERROR_STATUS_2[3]
Diagnosis: leakage to GND / VBAT. Interface		x		Ch1: ERROR_STATUS_4[9:8] Ch2: ERROR_STATUS_6[9:8] Ch3: ERROR_STATUS_8[9:8] Ch4: ERROR_STATUS_10[9:8]	Ch1: ERROR_STATUS_2[0] Ch2: ERROR_STATUS_2[1] Ch3: ERROR_STATUS_2[2] Ch4: ERROR_STATUS_2[3]
overcurrent. Interface		x		Ch1: ERROR_STATUS_4[10] Ch2: ERROR_STATUS_6[10] Ch3: ERROR_STATUS_8[10] Ch4: ERROR_STATUS_10[10]	Ch1: ERROR_STATUS_2[0] Ch2: ERROR_STATUS_2[1] Ch3: ERROR_STATUS_2[2] Ch4: ERROR_STATUS_2[3]
Data buffer configuration error (width=96bit). Interface		x		Ch1: ERROR_STATUS_4[11] Ch2: ERROR_STATUS_6[11] Ch3: ERROR_STATUS_8[11] Ch4: ERROR_STATUS_10[11]	Ch1: ERROR_STATUS_2[0] Ch2: ERROR_STATUS_2[1] Ch3: ERROR_STATUS_2[2] Ch4: ERROR_STATUS_2[3]

TYPE OF ERROR	ASIC	INTERFACE CH1-CH4	FRAME 1-6	ERROR STATUS REGISTER	ERROR BIT FLAG
Reverse current. Interface		x		Ch1: ERROR_STATUS_4[12] Ch2: ERROR_STATUS_6[12] Ch3: ERROR_STATUS_8[12] Ch4: ERROR_STATUS_10[12]	Ch1: ERROR_ STATUS_2[0] Ch2: ERROR_ STATUS_2[1] Ch3: ERROR_ STATUS_2[2] Ch4: ERROR_ STATUS_2[3]

6.2 DIGITAL PART

6.2.1 COMMUNICATION INTERFACE TO MICRO CONTROLLER

As interface to the micro controller, either an UART or SPI interface can be selected. The pins for both interfaces are shared.
The interface is configurable from µC

- with rising edge of NRES the UART / SPI interface is latched
- depending on state of pin NCS either UART or SPI is selected
- **NCS = low** means **UART**
- **NCS = high** means **SPI**

Following pins are used for UART communication:

- SDI_RXD
- SDO_TXD
- SCLK

Following pins are used for SPI communication:

- SDI_RXD
- SDO_TXD
- SCLK
- NCS

6.2.2 MANCHESTER DECODER

The manchester decoder is compliant to PSI5 1.3 and 2.1. The following interface diagnosis features are supported:

- wrong data rate
- wrong start bit combination
- wrong number of data bits
- CRC or parity failure
- wrong interframe time
- no or unexpected frame

6.2.2.1 Manchester Data Handling and Buffer Architecture

For each channel are a MCD_data_buffer with a width of 36bits and a data_buffer with a width of 96bits implemented.

- Data_buffer (96bit) is used in different configurations for UART / SPI mode (see figure below).
- Data_buffer and MCD_data_buffer will be set to default bit value = '1' if the channel is disabled.
  - Disabled either by writing bits ASIC_CNFG_3[EN_CHx] via UART/SPI Write_Register command or
  - by automatically switch-off in an error condition (e.g. over current error).

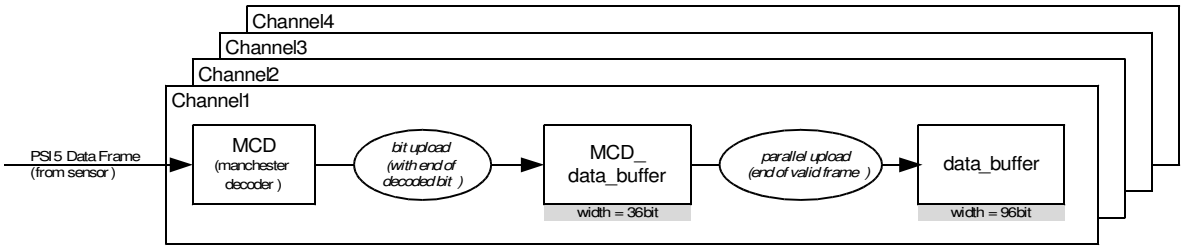


Figure 6.2.2.1-1: Buffer Architecture Overview

6.2.2.1.1 UART DATA BUFFER

UART buffer behavior:

- One frame will be stored
- Data will be filled up starting at bit0 (LSB) of buffer
- Empty bits will be filled up with default bit value = '1' ('1' not used as frame ID)
- Min data length = Fid0...Fid2 + Err0...Err1 + D0...D7 + parity; Σ = 14bit
- Max data length = Fid0...Fid2 + Err0...Err1 + D0...D27 + CRC; Σ = 36bit

'"With an appropriate UART baud rate, the IC transmits the data to the µController without any overwriting."'

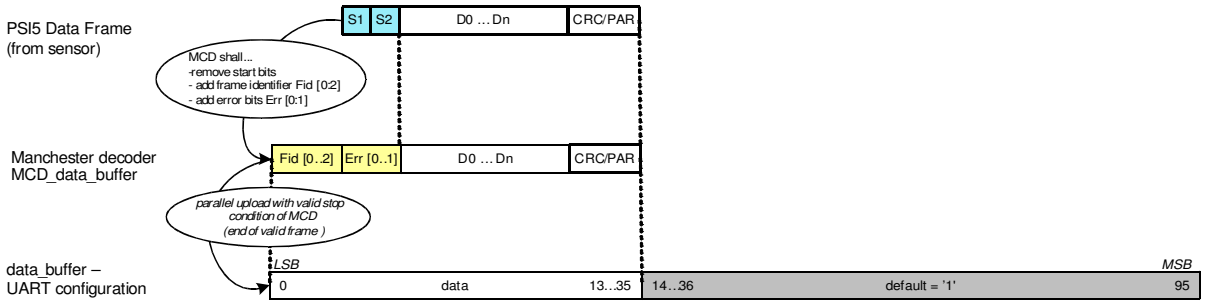


Figure 6.2.2.1.1-1: UART Data Buffer

6.2.2.1.2 SPI DATA BUFFER

SPI data buffer behavior:

- MCD_data_buffer has a length of 36bit; only the configured nb of bits (according TSx_FLEN) + Err[0:1] + Fid[0:2] are uploaded into SPI_data_buffer; the remaining bits of MCD_data_buffer are filled up (stuffed) with '1'. A special case occurs for SPI_BUFFER_CONFIG =0b00 (48bit): after upload of MCD_data_buffer, bits [0:35] includes data + stuffing '1', whereas bits [36:47] are stuffed with '0' (described as don't care bits in Figure Figure 6.2.3.9.4-1). This doesn't matters for other SPI_BUFFER_CONFIG configuration as buffer length is smaller than MCD_data_buffer length.
- The data_buffer has to be configured during IC start up, by bits CHx_CFG7[SPI_BUFFER_CONFIG]. The buffer is divided in blocks with equal number of bits.
- Data will be filled up starting at LSB of every individual block
- Unused buffer identifiers (BID[x]) are filled up with value = '1' (per default). A read request will result in
  - Frame identifier - Fid[2:0] ='111'-> µC can detect that no data were written into this block (wrong BID[x] was read).
  - Error Bits - Err[1:0] = '11' -> µC has to discard (default values instead of error information)
- **It's mandatory to read block wise via commands SPI_Get_Data_xxb according the appropriate buffer configuration. This means for SPI_BUFFER_CONFIG="11" the command SPI_Get_Data_16b is mandatory.**
- After reading, all bits per block will be filled up with default bit value = '1'
- During transfer from MCD_data_buffer to data_buffer, an error is flagged in ERROR_STATUS_4/6/8/10[11] = BUFF_ERR_CHx if number of bits(MCD_data_buffer) > number of bits per BID. In this case no data is transferred.
- The data_buffer is completely **erased** (filled up with default value ='1') if a **channel is disabled**, e.g. by ASIC_CNFG_3[EN_CHx]='0', VBUS overvoltage, overtemperature or overcurrent shut down.

The number of PSI5 data bits (payload) per buffer identifier (BID) is shown in the table below for all configurations.

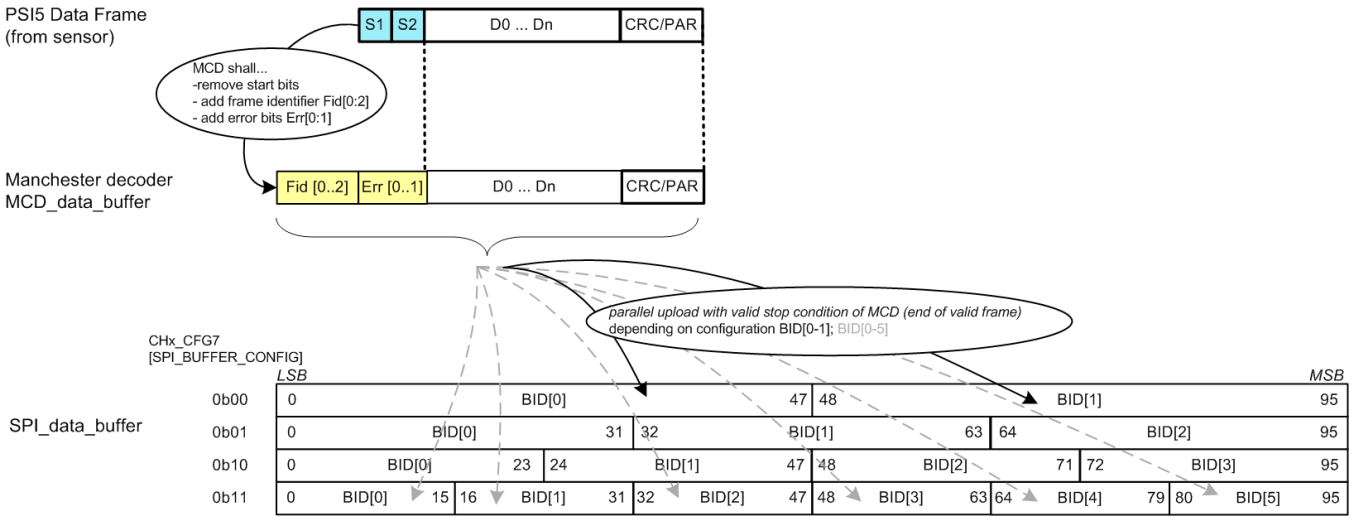


Figure 6.2.2.1.2-1: SPI Data Buffer

If number of frames higher than number of configured buffers (Fid > BID):

- A buffer has to be used for several frames
- µController has to ensure to read buffer data before new data is loaded, otherwise it's overwritten.

Following example shows buffer configuration CHx_CFG7[SPI_BUFFER_CONFIG]=0b01 with 4 identical PSI5 frames:

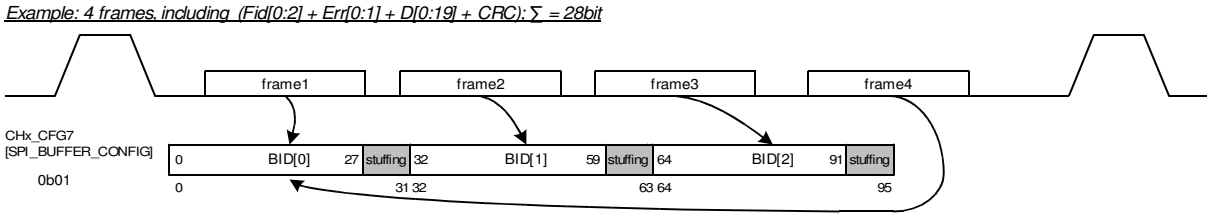


Figure 6.2.2.1.2-2: SPI Data Buffer incl. 4 Frames

Table 6.2.2.1.2-1: SPI Buffer Configuration

CHx_CFG7 [SPI_BUFFER_CONFIG]	***Σ per BID [bit]***	***FiD + Err [bit]***	***max payload = PSI5 data w/o start bits [bit]***
0b00	48*	5	43
0b01	32*	5	27
0b10	24*	5	19
0b11	16*	5	11

*: Please note the appropriate SPI_Get_Data_xxb-command selected by the number of bits in this column.

6.2.2.2 Manchester Bit Encoding

6.2.2.2.1 Definition of data edge / compensation edge

According PSI5 standard, a current transition in the middle of the bit time represents the logical value of the transferred data (Manchester code) with

"**high** current -> **low** current" transition for a logical '**1**',
"**low** current -> **high** current" transition for a logical '**0**'.

Within this specification, this transition is called **data edge**; transitions at start / end of the bits are called **compensation edge**.

6.2.2.2.2 Interpretation with Manchester Decoder

The implemented Manchester Decoder (MCD) state machine converts PSI5 data (transmitted by sensors in Manchester code) into NRZ code.
The input signal is filtered by the analog datacomparator.

The user is able to configure the time slot in which a data edge / compensation edge is accepted via register ASIC_CNFG_1[MCD_DATA_CMP_WINDOWS].
In principle, the default configuration is recommended with MCD_DATA_CMP_WINDOWS=0b00.
For certain pattern of electro-magnetic disturbers (from environment) the configuration of MCD_DATA_CMP_WINDOWS=0b01 could improve immunity by decreasing the data edge window, but reduces the range of MCD duty cycle.

6.2.2.2.3 Definition of Duty Cycle

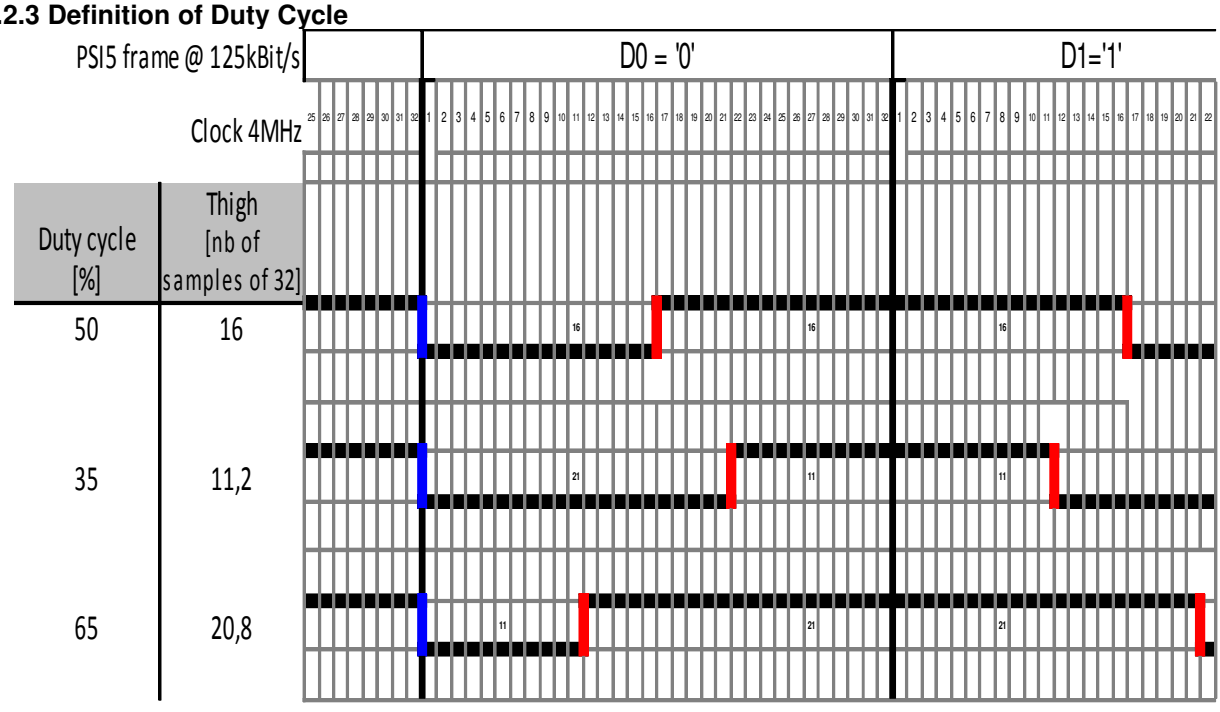


Figure 6.2.2.2.3-1: Example MCD Duty Cycle

6.2.2.2.4 Decoder Error Flags

The following chapter gives some details about the setting of flags MD_PERR_CHx_Fx, MD_FERR_CHx_Fx, MD_NO_FR_CHx_Fx and MD_UNEX_FR_CHx_Fx.

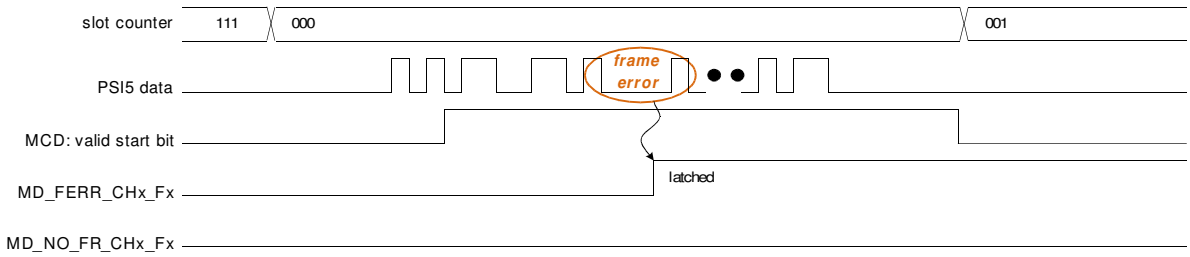


Figure 6.2.2.2.4-1: MD_FERR_CHx_F1

Note that for a special failure condition two error flags for one frame can be set.
Failure condition:
e.g. default IC configuration; PSI5 sensor with 189kbps connected (instead of 125kbps); depending on PSI5 data, either 1 or 2 error bits are flagged.

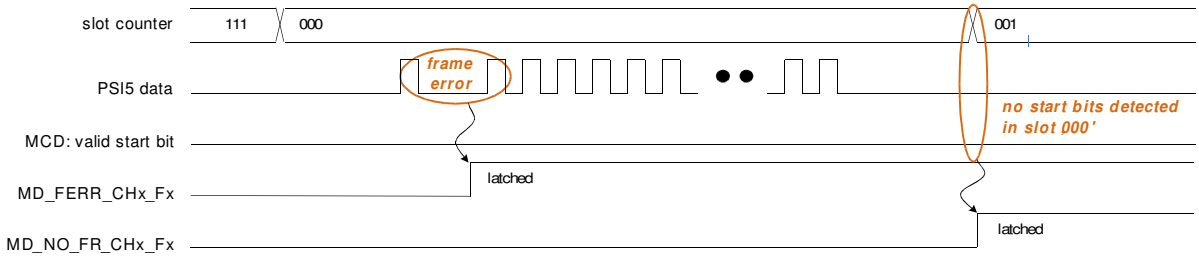


Figure 6.2.2.2.4-2: Set Of Error Flags (2errors; data=0x3FF)

6.2.3 SPI

The SPI communication between one master and multiple slaves can be operated in parallel or in daisy chain.

Parallel Operation

Several SPI-slaves can be connected to one SPI channel. The communication lines SDI_RXD, SDO_TXD and CLK are shared and every slave has its own chip select line (NCS).

Daisy Chain Operation

Several slaves can be connected to the µC in daisy chain operation to save µC interface pins (one common chip select line for all slaves in the chain).

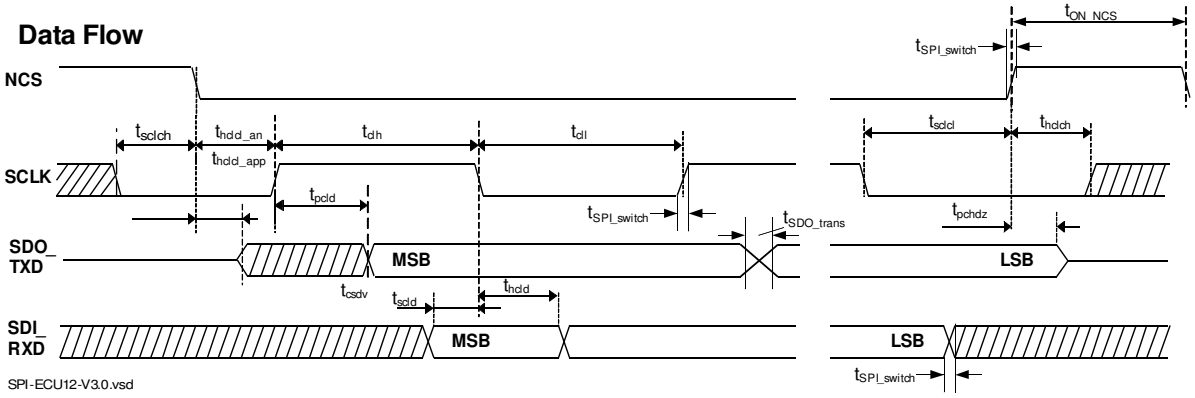


Figure 6.2.3-1: Data Flow Graphic

In case NCS is high, any signals (e.g. very high clock frequencies e.g. 20MHz max.) at the SCLK and SDI_RXD pins are ignored, and SDO_TXD remains in a high impedance state. After an NCS High to Low transition, the SPI response word is multiplexed from the latches that were specified by the last command into the shift register, i.e. the SDO_TXD changes from high impedance state to the state of the MSB of the last addressed SPI register, independent of the SPI clock state.

The SCLK pin must be low when NCS switches to low.
At each rising edge of the clock pulse after NCS goes low, the response word is serially shifted out on the SDO_TXD pin.
At each falling edge of the clock pulse (after NCS goes low) the new control word is serially shifted in on the SDI_RXD pin. The SPI command bits are decoded to determine the destination address for the data bits. After the 16th (or multiple of 16, for daisy chains) clock cycle, at the next NCS low to high transition, the SPI shift register data bits are transferred into the latch whose address was decoded from the SPI shift register command bits.
A command is executed after 16 SCLK (or a multiple of 16) and NCS goes high.
During reset, SDO_TXD is forced into a high impedance state and any inputs from SCLK and SDI_RXD are ignored.

SPI Format
Each device is controlled with a 16 bit control command, see following chapters.
The command is stored in a command register after the rising edge of NCS. The response consists of a 16 bit word which contains the before requested information like e.g. diagnostic or output state.

Response after Reset or Communication Error
In case of reset or communication error (not valid commands, number of clocks not multiples of 16) following response will be sent in the next valid SPI frame: "0x0000". The execution of not valid commands is blocked and command with NCS low without clock are ignored.

Order of MSB/LSB Bit
MSB is sent first.

CRC
SPI Packet Frames from transceiver to µController include a XCRC (see 6.2.5).

Daisy Chain
Daisy chain operation is supported.

6.2.3.1 Error Handling

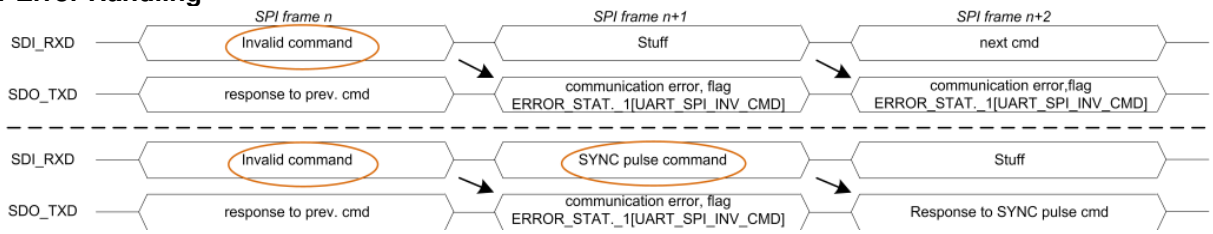


Figure 6.2.3.1-1: SPI Error Handling Example 1

1: Examples invalid command for 'Read Sensor Data 16bit':

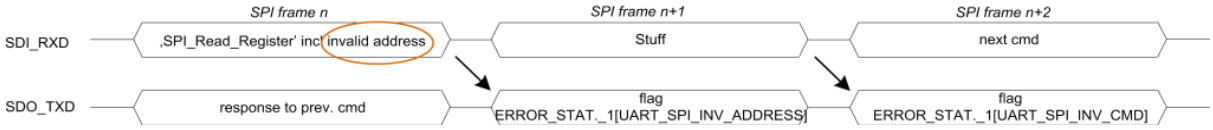


Figure 6.2.3.1-2: SPI Error Handling Example 2

4a: Example: Command 'SPI_Read_Register' including invalid address A[5:0]:

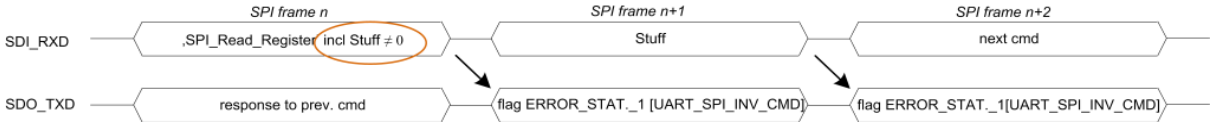


Figure 6.2.3.1-3: SPI Error Handling Example 3

4b: Example: Command 'SPI_Read_Register' including Stuff ≠ 0 (frame n):

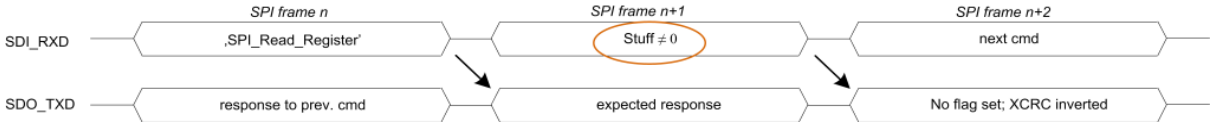


Figure 6.2.3.1-4: SPI Error Handling Example 4

4c: Example: Command 'SPI_Read_Register' including Stuff ≠ 0 (frame n+1):

Table 6.2.3.1-1: SPI Communication Error

#	Root cause for communication error	Reaction/Flag	Description
1	invalid commands	ERROR_STATUS_1 [UART_SPI_INV_CMD]	command rejected
2	number of clocks NOT multiples of 16	ERROR_STATUS_1 [SPI_CLK_ERR]	command rejected
3a	command 'SPI_Write_Register' including invalid address A[5:0]	ERROR_STATUS_1 [UART_SPI_INV_ADDRESS] & [UART_SPI_INV_CMD]	command rejected
3b	command 'SPI_Write_Register' including stuff ≠ 0 (in frame n+1)	No flag	frame n+1: correct response frame n+2: wrong XCRC (6bit stuff is used for calculation)

#	Root cause for communication error	Reaction/Flag	Description
4a	command 'SPI_Read_Register' including invalid address A[5:0]	see #3a	command rejected
4b	command 'SPI_Read_Register' including stuff ≠ 0 (in frame n)	see #1	command rejected
4c	command 'SPI_Read_Register' including stuff ≠ 0 (in frame n+1)	no flag	frame n+1: correct response frame n+2: send zero response including inverted XCRC to uC
5a	commands 'SPI_Get_Data_xxb' - NOT according buffer configuration e.g. SPI_BUFFER_CONFIG="00" and "SPI_Get_Data_16/24/32b"	ERROR_STATUS_1 [UART_SPI_INV_ADDRESS]	command rejected
5b	commands 'SPI_Get_Data_xxb' - according buffer configuration - including invalid ChID[2:0] Invalid channel identifier ChID[2:0]: '000' / '101' / '110' / '111'	see #5a	command rejected
5c	commands 'SPI_Get_Data_xxb' - according buffer configuration - including invalid BID[2:0] Invalid buffer identifier BID[2:0] depends on configuration: e.g. SPI_BUFFER_CONFIG=0b00 -> '010' / '011' / '100' / '101' / '110' / '111'	see #5a	command rejected
5d	commands 'SPI_Get_Data_xxb' - including stuff ≠ 0 (in frame n)	see #1	command rejected
5e	commands 'SPI_Get_Data_xxb' - including stuff ≠ 0 (in frame n+1)	no flag	frame n+1: correct response frame n+2 till before the end of command response: communication error Last command response: send zero response including inverted XCRC to uC
5f	commands 'SPI_Get_Data_xxb' - including correct SPI_SYNC_PULSE cm with 4bit stuff ≠ 0 (in frame n+1)	see #1	frame n+1: correct response frame n+2 till before the end of command response: communication error Last command response: send zero response including inverted XCRC to uC
6	command 'SPI_SYNC_PULSE' - including stuff ≠ 0 (in frame n)	see #1	command rejected

#	Root cause for communication error	Reaction/Flag	Description
8	command 'SPI_NOP' - including stuff ≠ 0 (in frame n)	see #1	command rejected
9	command 'SPI_SW_RESET' - including stuff ≠ 0 (in frame n)	see #1	command rejected

6.2.3.2 Overview of Communication Frames

Table 6.2.3.2-1: Overview of SPI Communication Frames

Communication Path	Commands/Responses	SPI Frame n [SPI Packet Frame]	SPI Frame n+1 [SPI Packet Frame]	SPI Frame n+2 [SPI Packet Frame]	SPI Frame n+3 [SPI Packet Frame]	SPI Frame n+4 [SPI Packet Frame]
µC->transceiver	SPI_NOP	cmd[3:0]; Stuff [11:0]	next cmd			
µC->transceiver	Response	response to previous cmd	cmd[3:0]; Stuff [11:0]			
µC->transceiver	SPI_Write_Register	cmd[3:0]; A[5:0]; D[15:10]	D[9:0]; Stuff [5:0]	SPI_WRITE_Register SPI_READ_Register SPI_SYNC_Pulse SPI_NOP SPI_SW_Reset		
µC->transceiver	Response to SPI_Write_reg	response to previous cmd	cmd[3:0]; A[5:0]; D[15:10];	D[9:0]; XCRC[5:0]		
µC->transceiver	SPI_read_reg	cmd[3:0]; A[5:0]; Stuff[5:0]	Stuff[15:0]	next cmd		
µC->transceiver	Response to SPI_Read_Register	response to previous cmd	cmd[3:0]; A[5:0]; D[15:10]	D[9:0]; XCRC[5:0]		
µC->transceiver	SPI_SYNC_Pulse	cmd[3:0]; ChT[3:0]; ChL[3:0]; Stuf f[3:0]	next cmd			
µC->transceiver	Response	response to previous cmd	cmd[3:0]; ChT[3:0]; ChL[3:0]; Stuff[3:0]			
µC->transceiver	Response	response to previous cmd	cmd[3:0]; Stuff [11:0]			
µC->transceiver	SPI_Get_Data_16b	cmd[3:0]; ChID[2:0]; BID[2:0]; Stuff[5:0]	Stuff[15:0] Optional: SPI_SYNC_Pulse	next cmd		
µC->transceiver	Response to SPI_Get_Data_16b	response to previous cmd	cmd[3:0]; ChID[2:0]; BID[2:0]; Stuff[5:0]	D[9:0]; XCRC[5:0]		
µC->transceiver	SP_Get_Data_24b	cmd[3:0]; ChID[2:0]; BID[2:0]; Stuff[5:0]	Stuff [15:0] Optional: SPI_SYNC_Pulse	Stuff [15:0]	next cmd	
µC->transceiver	Response to SPI_Get_Data_24b	response to previous cmd	cmd[3:0]; CHID[2:0]; BID[2:0] Fid[2:0]; Err[1:0]; D[18]	D[17:2]	D[1:0]; Stuff [7:0]; XCRC[5:0]	
µC->transceiver	SPI_Get_Data_32b	cmd[3:0]; ChID[2:0]; BID[2:0]; Stuff [5:0]	Stuff [15:0] Optional: SPI_SYNC_Pulse	Stuff [15:0]	next cmd	
µC->transceiver	Response to SPI_Get_Data_32b	response to previous cmd	cmd[3:0]; CHID[2:0]; BID[2:0] Fid[2:0]; Err[1:0]; D[26]	D[25:10]	D[9:0]; XCRC[5:0]	
µC->transceiver	SPI_Get_Data_48b	cmd[3:0]; ChID[2:0]; BID[2:0]; Stuff [5:0]	Stuff [15:0] Optional: SPI_SYNC_Pulse	Stuff [15:0]	Stuff [15:0]	next cmd
µC->transceiver	Response to SPI_Get_Data_48b	response to previous cmd	cmd[3:0]; CHID[2:0]; BID[2:0] Fid[2:0]; Err[1:0]; D[42]	D[41:26]	D[25:10]	D[9:0]; XCRC[5:0]
µC->transceiver	SPI_SW_Reset	cmd[3:0]; Stuff [11:0]	next cmd			
µC->transceiver	Response	response to previous cmd	cmd[3:0]; Stuff [11:0]			

BID = Buffer Identifier
CHID = Channel Identifier
ChTx = Channel Trigger for sync pulse (0=disabled; 1=enabled)

ChLx = Sync pulse length (0=short; 1=long)

Note:
- For 'Read Sensor Data xxbit' commands the SPI frame n+1 includes optional the 'SYNC Pulse command' instead of NOP command to optimize the SPI bandwidth
- **The idle time between consecutive SPI frames has to fulfill parameter** ton_NCS**.**

6.2.3.3 Overview of SPI commands

All valid SPI commands are shown in the table below.
Any other combinations (commands from micro controller) are rejected but flagged in register ERROR_STATUS_1[UART_SPI_INV_CMD] for diagnosis purpose.
In case of reset or communication error the following response will be sent: 0x0000 in the following valid SPI frame. Execution of command is blocked.

Chip select (NCS) low without any clock pulses at SCLK will be ignored. Next response to previous valid frame.

Table 6.2.3.3-1: Overview SPI commands

SPI command	***command bits[15:12]***	***remaining bits [11:0]***
SPI_Write_Register	0001	0000 0000 0000
SPI_Read_Register	0010	0000 0000 0000
SPI_Sync_Pulse	0011	0000 0000 0000
SPI_Get_Data_16b	0100	0000 0000 0000
SPI_Get_Data_24b	0101	0000 0000 0000
SPI_Get_Data_32b	0111	0000 0000 0000
SPI_Get_Data_48b	1000	0000 0000 0000
SPI_NOP	1110	0000 0000 0000
SPI_SW_Reset	1111	0000 0000 0000

6.2.3.4 No Operation Command

Receiving a NOP command, the IC will perform no operation.
It shall be used to get the last frame of a SPI communication sequence.

The bit configuration of this one frame command is shown in the figure below:

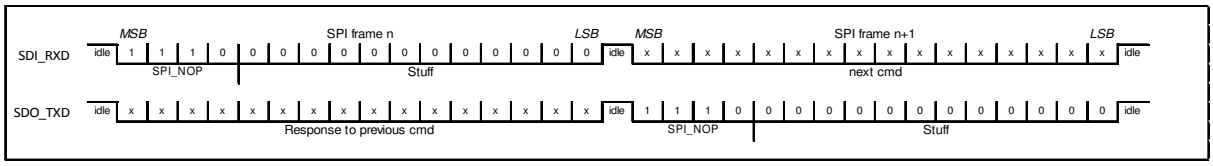


Figure 6.2.3.4-1: SPI NOP Command

6.2.3.5 Write Configuration Register Command

With the command "Write Configuration Register" any 16bit register can be written.
Every command consists of three consecutive SPI frames, shown in the figure below.
As SPI frame n+2 on SDI_RXD are following cmds allowed: SPI_Write_Register, SPI_Read_Register, SPI_SYNC_Pulse, SPI_NOP or a SPI_SW_Reset.

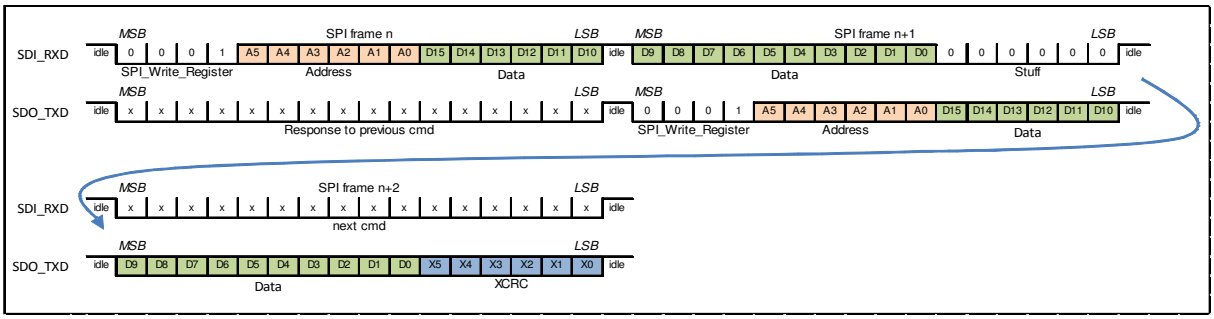


Figure 6.2.3.5-1: SPI Write Register Command

6.2.3.6 Software Reset Command

With the first execution of the software reset command, all configuration registers are initialized to default values if bit ASIC_CNFG_1[CNFG_LOCK]='0'.
If bit ASIC_CNFG_1[CNFG_LOCK]='1' all configuration registers are initialized to default values except register ASIC_CNFG_1 and ASIC_CNFG_2.

With the second execution of the software reset command, the bit ASIC_CNFG_1[CNFG_LOCK] is reset to '0'.

The Software Reset Command includes one SPI Frame only:

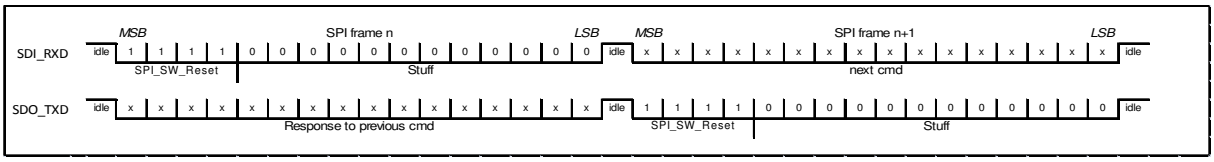


Figure 6.2.3.6-1: SPI Software Reset Command

6.2.3.7 Read Configuration Register Command

With the command "Read Configuration Register" any 16bit register can be read.
Every command consists of three consecutive SPI frames.

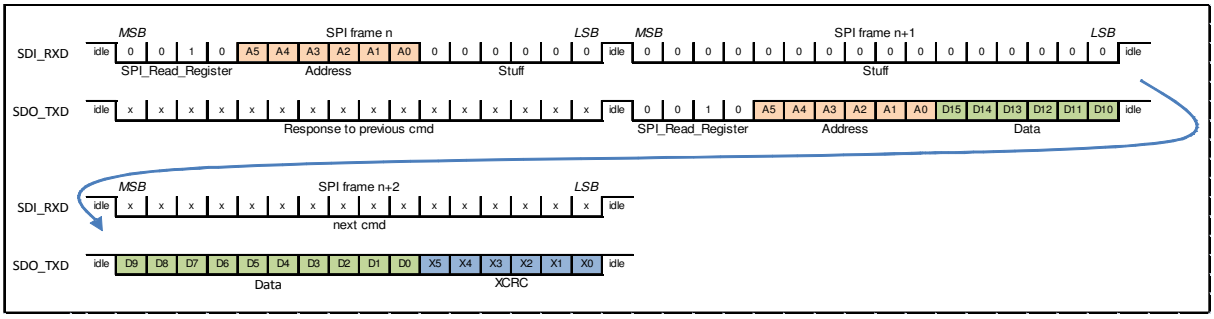


Figure 6.2.3.7-1: SPI Read Register Command

6.2.3.8 SYNC Pulse Command

Sync pulses with different widths can be triggered by sending the sync pulse command.
For configuration of the sync pulses there are the two bits ChTx and ChLx available.

Bit ChTx determines the generation of the sync pulse on the desired channel and ChLx determines the width of the pulse, whereas a logical '0' leads to a short and a logical '1' leads to a long sync pulse.

The detailed bit setting is shown in the table below:

Table 6.2.3.8-1: SYNC Pulse Command

SPI command	*Command[15:12]*	*SYNC trigger ChT[11:8]+SYNC length ChLx[7:4]*	*Stuffing[3:0]*
SYNC Pulse	0011	ChT3 & ChT2 & ChT1 & ChT0 & ChL3 & ChL2 & ChL1 & ChL0	0000
Long Sync Pulse all Ch	0011	11111111	0000
Long Sync Pulse Ch1	0011	00010001	0000
Long Sync Pulse Ch2	0011	00100010	0000
Long Sync Pulse Ch3	0011	01000100	0000
Long Sync Pulse Ch4	0011	10001000	0000
Short Sync Pulse all Ch	0011	11110000	0000
Short Sync Pulse Ch1	0011	00010000	0000
Short Sync Pulse Ch2	0011	00100000	0000
Short Sync Pulse Ch3	0011	01000000	0000
Short Sync Pulse Ch4	0011	10000000	0000

Example: e.g. '0011 1001 1001 0000' (MSB->LSB) defines two long SYNC pulses on channel 1 and channel 4.
Note: The application shall ensure to trigger the SYNC pulse generator only once during TSYNC by max. 1 "SYNC Pulse command" per TSYNC. More trigger commands overwrite the former command (if SYNC pulse delay counter has not exceeded) or trigger a new SYNC pulse.

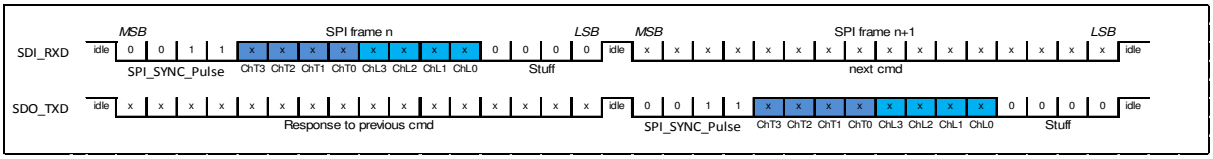


Figure 6.2.3.8-1: SPI SYNC Pulse Command

6.2.3.9 Read Sensor Data

Sensor data is requested by executing the "Read Sensor Data" command. The number of SPI frames increases with the number of requested sensor data bits.
For example, a request of 16 sensor data bits results in a communication with three SPI frames.

The SPI frame 2 has to be filled with stuffing bits or (optional) it can contain the "SYNC Pulse command" to optimize the SPI bandwidth by "Read Sensor Data" command.

It's mandatory to read block wise via commands SPI_Get_Data_xxb according the appropriate buffer configuration. This means for SPI_BUFFER_CONFIG="11" the command SPI_Get_Data_16b is mandatory (see 6.2.2.1.2**).**

For details of the bit position of PSI5 parity/CRC see 6.2.3.9.1.

For synchronous PSI5 mode the "SPI_data_buffer" has to be synchronized with the PSI5 data.
It is recommended to read PSI5 data buffer after all PSI5 slots within the current cycle where received.
The SPI read access shall start later than "latest PSI5-slot end" + 3 · t_{GAP} and shall end before "earliest PSI5-slot end" of the next PSI5 slot.

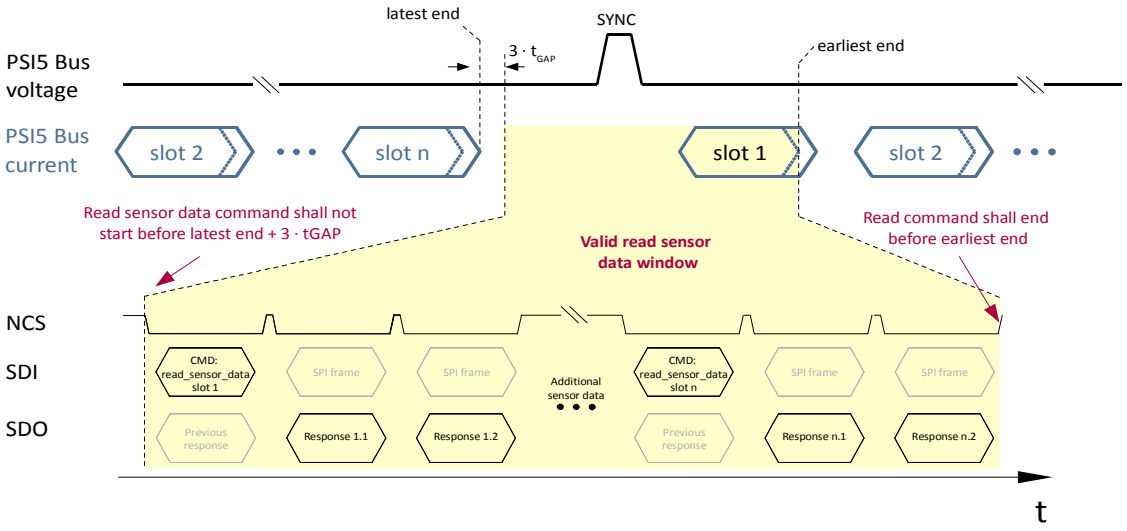


Figure 6.2.3.9-1: Valid read sensor data window 1

If data buffer has to be read interleaved within the PSI5 cycle the same constrains have to be considered.
The SPI read access shall start later than "latest PSI5-slot end" + 3 · t_{GAP} and shall end before "earliest PSI5-slot end" of the next PSI5 slot.

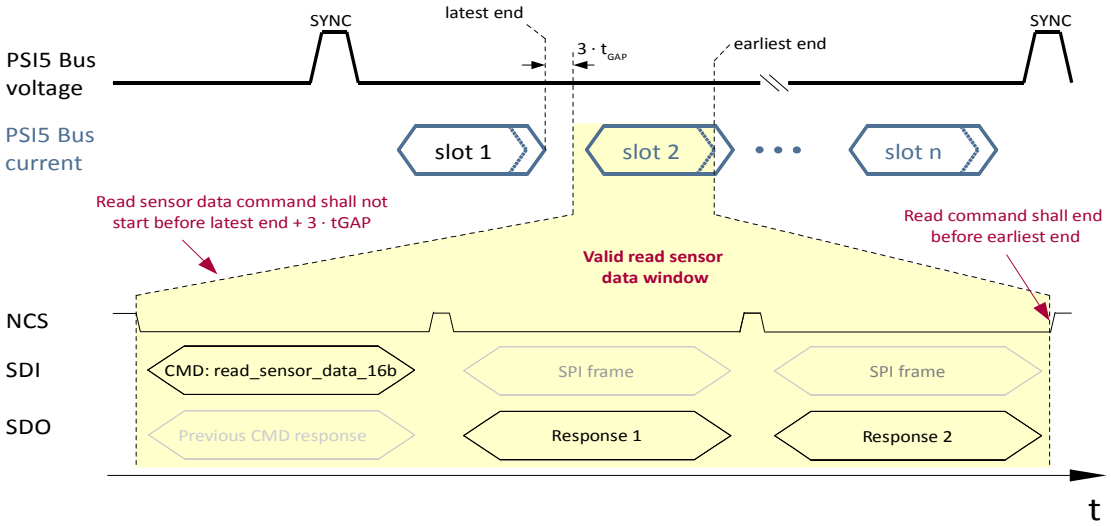


Figure 6.2.3.9-2: Valid read sensor data window 2

For asynchronous sensor mode it is not possible to access the data buffer synchronous to PSI5 data.
In this case it is recommended to use the UART mode.

6.2.3.9.1 Read of 16bit (11bit sensor data)

Communication template for 16bit (= 3xFrameID + 2xErrBits + 11 DataBits) is shown in the figure above.

Note: Position of PSI5 parity/CRC bits in data frame is represented by highest 'used' data bit Dx of SPI buffer. See following examples:

- 10 bit data + 1 parity bit -> D10 = parity bit
- 8 bit data + 1 parity bit -> D8 = parity bit
- 8 bit data + 3 crc bits -> D10=C0, D9=C1, D8=C2

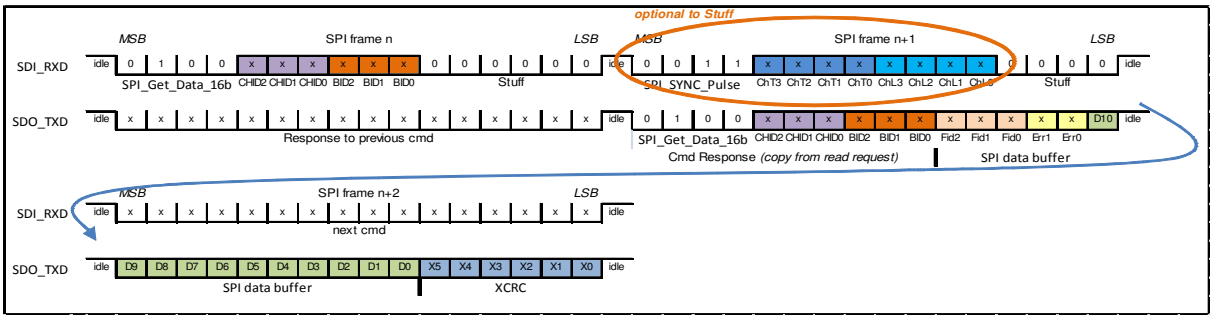


Figure 6.2.3.9.1-1: SPI Read Sensor Data 16bit

SPI_Get_Data_16b; **frame1; SDI_RXD**	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
	cmd3	cmd2	cmd1	cmd0	Chid2	Chid1	Chid0	BID2	BID1	BID0						
	Command				Channel ID			Buffer ID			Stuff					
Identifier Ch1	0	1	0	0	0	0	1				0	0	0	0	0	0
Identifier Ch2					0	1	0									
Identifier Ch3					0	1	1									
Identifier Ch4					1	0	0									
Identifier Buffer0								0	0	0						
Identifier Buffer1								0	0	1						
Identifier Buffer2								0	1	0						
Identifier Buffer3								0	1	1						
Identifier Buffer4								1	0	0						
Identifier Buffer5								1	0	1						

Figure 6.2.3.9.1-2: SPI Read Sensor Data 16bit-request at SDI_RXD -1st SPI frame-

SPI_Get_Data_16b; **frame2; SDO_TXD**	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
	cmd3	cmd2	cmd1	cmd0	Chid2	Chid1	Chid0	BID2	BID1	BID0	Fid2	Fid1	Fid0	Err1	Err0	D0
	Command				Channel ID			Buffer ID			Frame ID			Error bits		Data
Identifier Ch1	0	1	0	0	0	0	1									x
Identifier Ch2					0	1	0									
Identifier Ch3					0	1	1									
Identifier Ch4					1	0	0									
Identifier Buffer0								0	0	0						
Identifier Buffer1								0	0	1						
Identifier Buffer2								0	1	0						
Identifier Buffer3								0	1	1						
Identifier Buffer4								1	0	0						
Identifier Buffer5								1	0	1						
Identifier Frame1											0	0	0			
Identifier Frame2											0	0	1			
Identifier Frame3											0	1	0			
Identifier Frame4											0	1	1			
Identifier Frame5											1	0	0			
Identifier Frame6											1	0	1			
Error bit - no error														0	0	
Error bit - Interface error														0	1	
Error bit - ASIC error														1	0	
Error bit - Interf. + ASIC error														1	1	

Figure 6.2.3.9.1-3: Response to SPI Read Sensor Data 16bit at SDO_TXD -2nd SPI frame-

6.2.3.9.2 Read of 24bit (19bit sensor data)

Communication template for 24bit (= 3xFrameID + 2xErrBits + 19 DataBits):

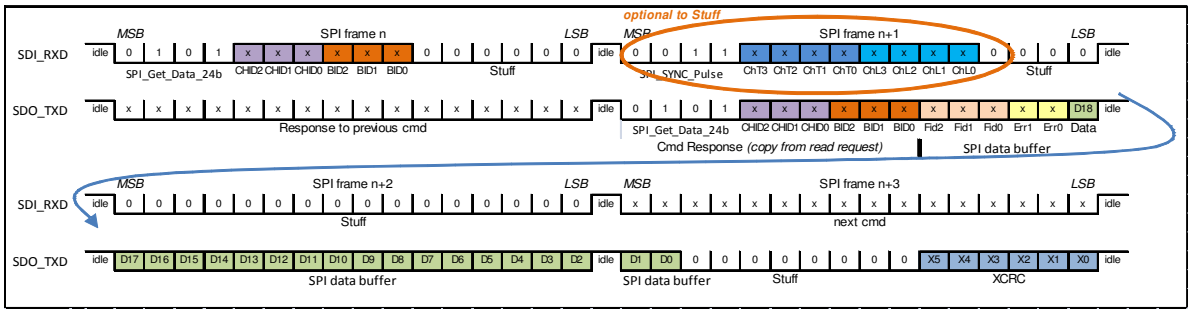


Figure 6.2.3.9.2-1: Read Sensor Data 24bit command

6.2.3.9.3 Read of 32bit (27bit sensor data)

Communication template for 32bit (= 3xFrameID + 2xErrBits + 27 DataBits):

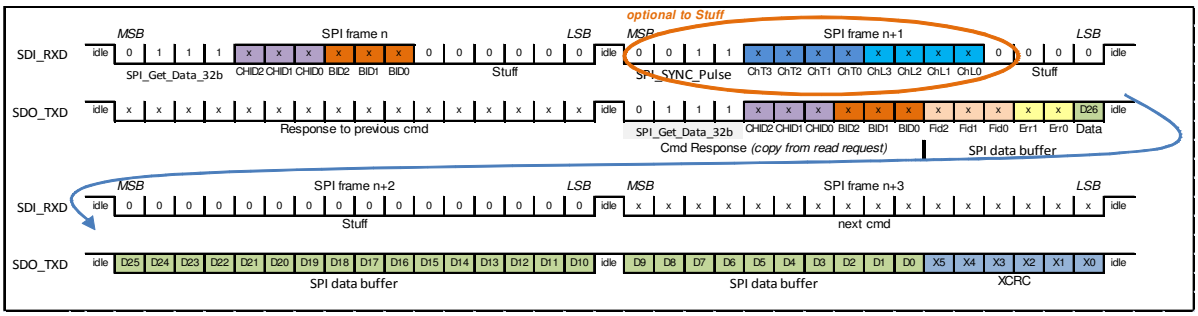


Figure 6.2.3.9.3-1: Read Sensor Data 32bit command

6.2.3.9.4 Read of 48bit (43bit sensor data)

Position of PSI5 parity/CRC bits -> see 'Read Sensor Data 16bit'
Communication template for 48bit (= 3xFrameID + 2xErrBits + 43 DataBits):

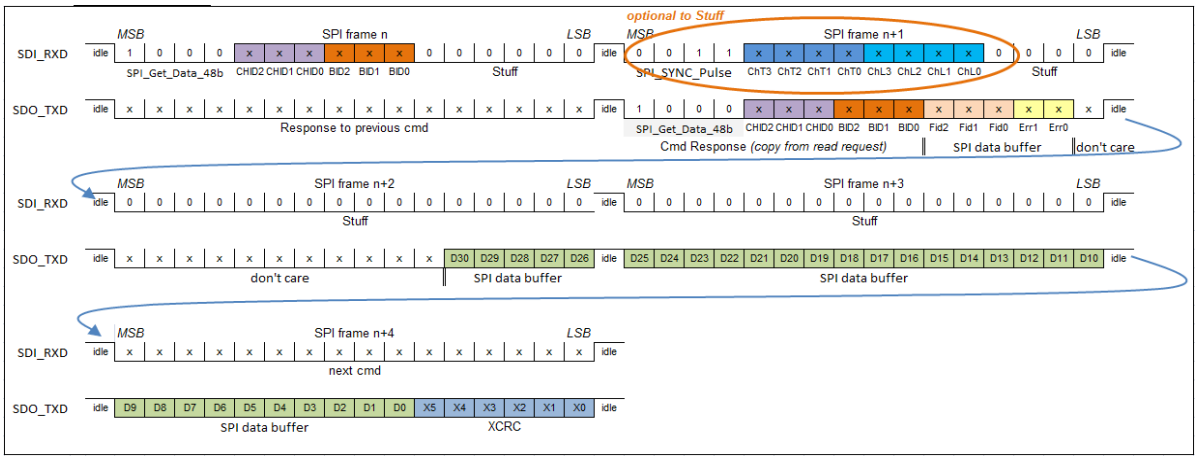


Figure 6.2.3.9.4-1: Read Sensor Data 48bit command

Note: For bits 'don't care' in frame n+1 / n+2 on SDO_TXD there are two scenarios: all 12 bits are either '0' or '1'; for more details see chapter 6.2.2.1.2.

6.2.4 UART

The UART data rate is derived from an external clock signal f_{SCLK_UART} with DC_{SCLK_UART} at pin SCLK and is calculated with the following formula $f_{UART} = \frac{fCLK\_UART}{5}$.

The external clock has to be supplied permanent.
The bit shift direction supports "Little Endian" format with LSB sent first.

6.2.4.1 Error Handling

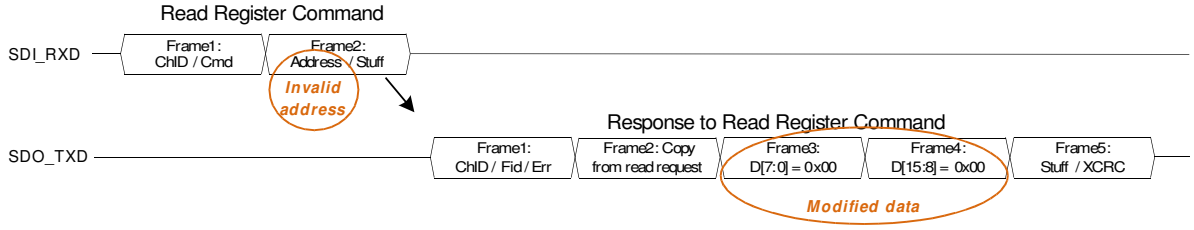


Figure 6.2.4.1-1: UART Error Handling Example 1

see #3: Command 'UART_Read_Register' including invalid address A[5:0]:
The 'Response to Read Register Command' is uploaded with with data bits D[15:0] = 0x0000.

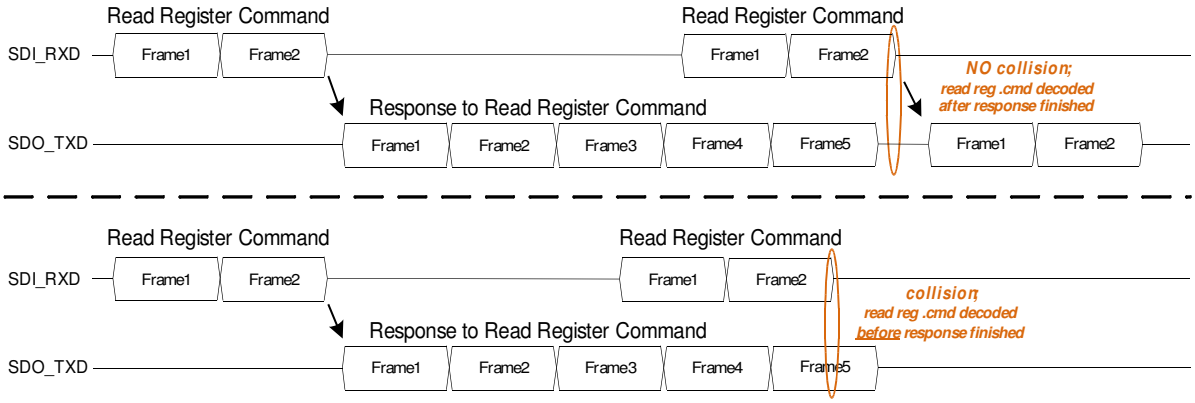


Figure 6.2.4.1-2: UART Error Handling Example 2

see #6: Collision of 'UART_Read_Register' commands:

While read register request command a collision with frames sent by the transceiver might occur.
In case of frames sent to the transceiver at pin RXD while the transceiver is transmitting data on pin TXD the RXD frame is ignored. To ensure a response from E521.4x device to a "Read Register cmd", the SDO_TXD has to be idle during decoding of "Read Register cmd". This is feasible if "Transfer of PSI5 data" is predictable.
For systems with asynchronous sensors it is recommended to use only one asynchronous sensor per chip. The probability of a response to "Read Register cmd" increases with decreased payload on SDO_TXD. The probability of a response to "Read Register cmd" increases with increased UART baud rate.
To decrease payload the UART idle time can be increased by Register ASIC_CNFG_2 / UART_IDLE_TIME[3:0] set to maximum value.

If synchronous mode is used the UART idle time can be predicted.
Example for UART =4MBaud:

- t1 = tnEE (earliest end of frame) = 142us
- t2 ≈ 3 x staggering + 1 UART frame = 3*10us + 55bit*0.25us = 44us => idle time = t1 + t2 = 98us

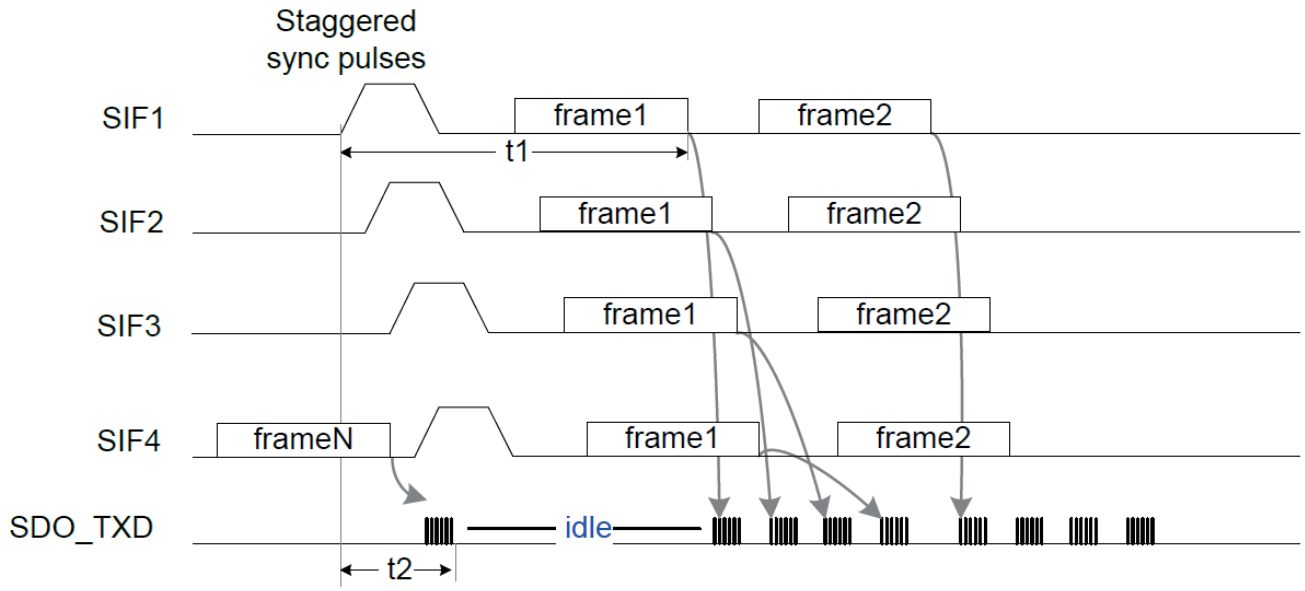


Figure 6.2.4.1-3: Syncpulse staggering

Table 6.2.4.1-1: UART Error Handling

#	Root cause	Reaction/Flag	Description
1	invalid commands	ERROR_STATUS_1 [UART_SPI_INV_CMD]	Command rejected
2a	command 'UART_Write_Register' including invalid address A[5:0]	ERROR_STATUS_1 [UART_SPI_INV_ADDRESS]	Command rejected
2b	command 'UART_Write_Register' including ChId ≠ 0	ERROR_STATUS_1 [UART_SPI_INV_CMD]	Command rejected
2c	command 'UART_Write_Register' including stuff ≠ 0	ERROR_STATUS_1 [UART_SPI_INV_ADDRESS]	Command rejected
3a	Command 'UART_Read_Register' including invalid address A[5:0]	ERROR_STATUS_1 [UART_SPI_INV_ADDRESS]	Command rejected
3b	Command 'UART_Read_Register' including ChId ≠ 0	ERROR_STATUS_1 [UART_SPI_INV_CMD]	Command rejected

#	Root cause	Reaction/Flag	Description
3c	Command 'UART_Read_Register' including stuff ≠ 0	ERROR_STATUS_1 [UART_SPI_INV_ADDRESS]	Command rejected
4	Wrong parity bit received	ERROR_STATUS_1 [UART_PERR]	Command rejected
5	Frame error = invalid stop bit	ERROR_STATUS_1 [UART_FERR]	Command rejected
6	Collision of 'UART_Read_Register' commands e.g. read request received while last read was not completed yet	ERROR_STATUS_1 [UART_SPI_COLLISION]	2nd Command rejected
7	Command 'Short SYNC pulse' including ChId >4	ERROR_STATUS_1 [UART_SPI_INV_CMD]	Command rejected
8	Command 'Long SYNC pulse' including ChId >4	ERROR_STATUS_1 [UART_SPI_INV_CMD]	Command rejected
9	Command 'No SYNC pulse' including ChId ≠ 0	ERROR_STATUS_1 [UART_SPI_INV_CMD]	Command rejected
11	Command 'SW reset' including ChId ≠ 0	ERROR_STATUS_1 [UART_SPI_INV_CMD]	Command rejected

6.2.4.2 Packet Frame Definition

A frame on the PSI5 interface is represented by a Packet Frame on the transmission line from the transceiver to the Controller.
Also the commands on the transmission line from the Controller to the transceiver ASIC, as well as the responses, are represented by a Packet Frame.
A Packet Frame can be a concatenation of 1 to 6 UART Frames.
For ASIC->uC: An idle time from 1 to 16 idle bits (configurable in register ASIC_CNFG_2) is implemented between consecutive Packet Frames from the UART in order to enable a re-synchronization of the next Packet Frame. The UART frame following an idle time which is equal or greater than the minimum idle time thus is always be assumed as the header of the next Packet Frame (default configuration: one bit minimum idle time between two Packet Frames).
For uC->ASIC: frames can be sent w/o idle time (back-to-back transfer possible)

6.2.4.3 UART Frame Definition

For transceiver to µC communication a UART frame (inside a packet frame) is composed of 1 start bit, 8 data bits, optional parity bit and 1 stop bit.
For µC to transceiver communication a UART frame (inside a packet frame) is composed of 1 start bit, 8 data bits, 1 parity bit and 1 stop bit.
Odd parity is enabled by default. For transceiver to µC communication the usage of a parity bit is configurable.
There is no idle time between UART frames inside a packet frame (i.e. a stop bit of a UART frame is followed by the start bit of a potentially following UART frame without any gap).

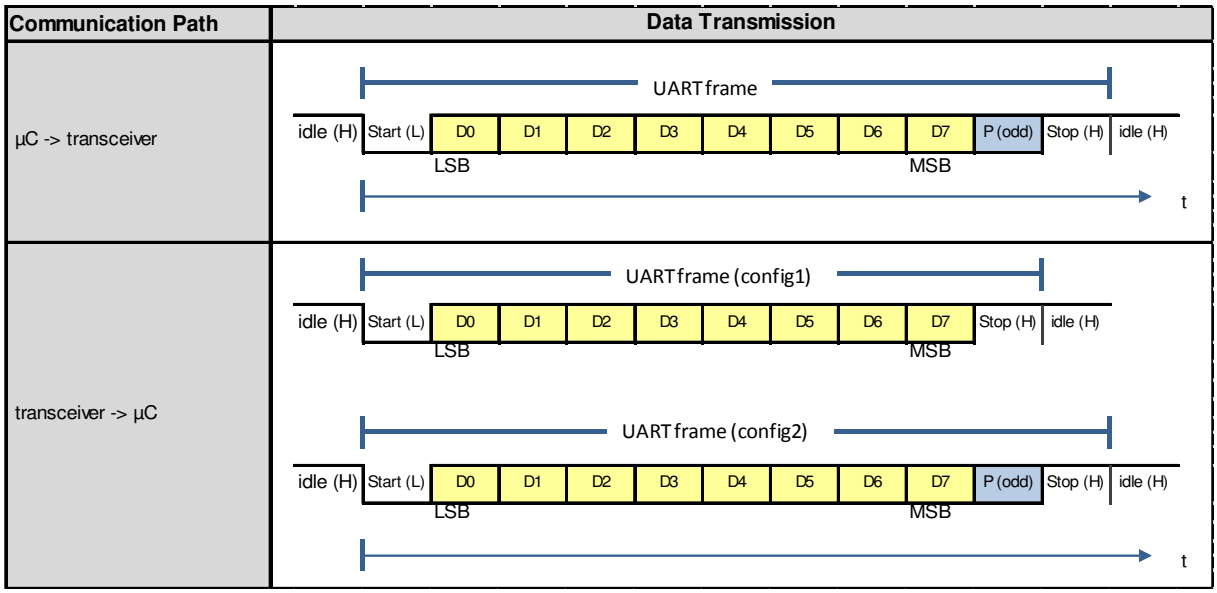


Figure 6.2.4.3-1: UART Data Transmission

6.2.4.4 Overview of Communication Frames

The defined UART commands and responses, with number of UART frames per packet frame, are shown in the table below.

- Packet frames from µC to transceiver means downstream
- Packet frames from transceiver to µC means upstream

Table 6.2.4.4-1: Overview of Communication Frames

Communication Path	*Commands/Responses*	*UART Frame 1 [Packet-Frame1]*	*UART Frame 2 [PacketFrame1]*	*UART Frame 3 [PacketFrame1]*	*UART Frame 4 [PacketFrame1]*	*UART Frame 5 [Pack-etFrame1]*	*UART Frame 6 [PacketFrame1]*
µC -> transceiver	UART_Write_Register	cmd[4:0], Chld[2:0]	Stuff[1:0], A[5:0]	D[7:0]	D[15:8]		
µC -> transceiver	UART_Read_Register	cmd[4:0], Chld[2:0]	Stuff[1:0], A[5:0]				
µC -> transceiver	UART_Short_SYNC_Pulse	cmd[4:0], Chld[2:0]					
µC -> transceiver	UART_Long_SYNC Pulse	cmd[4:0], Chld[2:0]					
µC -> transceiver	UART_No_SYNC_Pulse	cmd[4:0], Chld[2:0]					
µC -> transceiver	UART_Software_Reset	cmd[4:0], Chld[2:0]					
transceiver -> µC	Response to Read Register	Err[1:0], Fid[2:0], Chld[2:0]	CmdRes[7:0]	D[7:0]	D[15:8]	XCRC[5:0], Stuff[1:0]	
transceiver -> µC	Upload PSI5 data	Err[1:0], Fid[2:0], Chld[2:0]	D[7:0]	x*	x*	x*	x*

Note: x* = depending on definition of the corresponding PSI5 frame

6.2.4.5 Overview of UART Commands

All valid UART commands are shown in the table below. These commands have a hamming distance ≥2 to each other. Any other command from µController is rejected but flagged in register ERROR_STATUS_1[UART_SPI_INV_CMD] for diagnosis purpose.

Table 6.2.4.5-1: UART Command Table

UART Command	*Command[7:3]*	*Channel ID[2:0]*
UART_Write_Register	00001	000
UART_Read_Register	00010	000

UART Command	Command[7:3]	Channel ID[2:0]
UART_Short_Sync_Pulse all Ch	00100	000
UART_Short_Sync_Pulse Ch1	00100	001
UART_Short_Sync_Pulse Ch2	00100	010
UART_Short_Sync_Pulse Ch3	00100	011
UART_Short_Sync_Pulse Ch4	00100	100
UART_Long_Sync_Pulse all Ch	00111	000
UART_Long_Sync_Pulse Ch1	00111	001
UART_Long_Sync_Pulse Ch2	00111	010
UART_Long_Sync_Pulse Ch3	00111	011
UART_Long_Sync_Pulse Ch4	00111	100
UART_No_Sync_Pulse	10011	000
UART_Software_Reset	10101	000

6.2.4.6 Write Register Command

The write register sequence includes 4 UART frames:
UART Frame 1: Command bits cmd[4:0]; Channel Identifier ChId[2:0]
UART Frame 2: Stuffing bits[1:0], Address bits A[5:0]
UART Frame 3: Data Low Byte D[7:0]
UART Frame 4: Data Low Byte D[15:8]

Table 6.2.4.6-1: Write Register Command

Write Register Command	Command [7:3]	Channel ID [2:0]
Write Register Command	00001	000

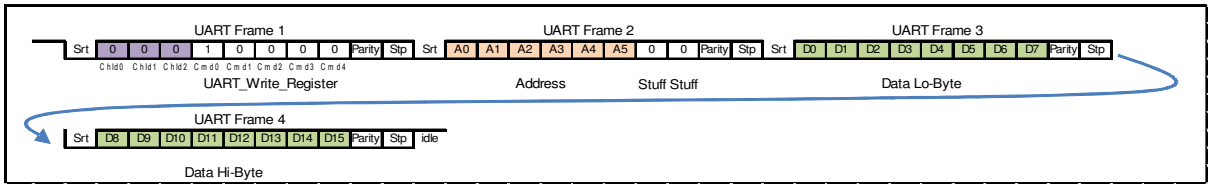


Figure 6.2.4.6-1: Write Register Command Packet Frame

6.2.4.7 Read Register Command

The read register sequence includes 2 UART frames:
UART Frame 1: Command bits cmd[4:0]; Channel Identifier ChId[2:0]
UART Frame 2: Stuffing bits[1:0], Address bits A[5:0]

Table 6.2.4.7-1: Read Register Command

Read Register Command	Command [7:3]	Channel ID [2:0]
Read Register Command	00010	000

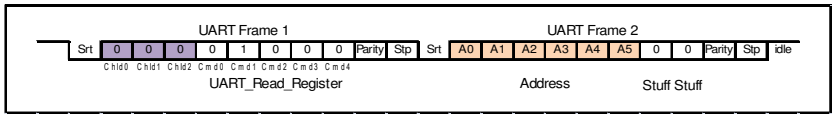


Figure 6.2.4.7-1: Read Register Command Packet Frame

6.2.4.8 Short SYNC Pulse Command

The Short SYNC Pulse Command includes 1 UART Frame only:
UART Frame 1: Command bits cmd[4:0]; Channel Identifier ChId[2:0]

Following table shows the configuration of Channel IDs:

Table 6.2.4.8-1: Short SYNC Pulse Command

Short SYNC Pulse Command	*Command [7:3]*	*Channel ID [2:0]*
Short Sync Pulse all Ch	00100	000
Short Sync Pulse Ch1	00100	001
Short Sync Pulse Ch2	00100	010
Short Sync Pulse Ch3	00100	011
Short Sync Pulse Ch4	00100	100

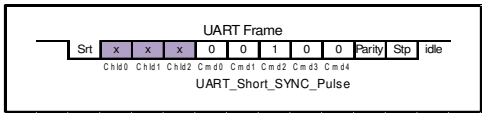


Figure 6.2.4.8-1: Short SYNC Command Packet Frame

6.2.4.9 Long SYNC Pulse Command

The Long SYNC Pulse Command includes 1 UART frame only:
UART Frame 1: Command bits cmd[4:0]; Channel Identifier ChId[2:0]

Following table shows the configuration of Channel IDs:

Table 6.2.4.9-1: Long SYNC Pulse Command

Long SYNC Pulse Command	*Command [7:3]*	*Channel ID [2:0]*
Long Sync Pulse all Ch	00111	000
Long Sync Pulse Ch1	00111	001
Long Sync Pulse Ch2	00111	010
Long Sync Pulse Ch3	00111	011
Long Sync Pulse Ch4	00111	100

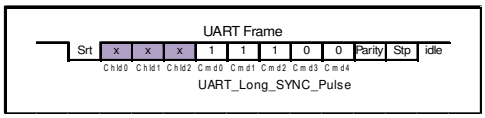


Figure 6.2.4.9-1: Long SYNC Command Packet Frame

6.2.4.10 No SYNC Pulse Command

For the tooth gap method, if a logical '0' (=absence of SYNC pulse) for ECU to sensor communication is required, a no sync pulse command can be send by the µController.

The no sync pulse command includes 1 UART frame only.
UART Frame 1: Command bits cmd[4:0]; Channel Identifier ChId[2:0]

Table 6.2.4.10-1: No SYNC Pulse Command

No SYNC Pulse Command	*Command [7:3]*	*Channel ID [2:0]*
No sync pulse	10011	000

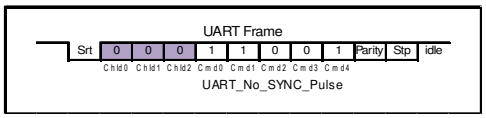


Figure 6.2.4.10-1: No SYNC Pulse Command Packet Frame

6.2.4.11 Software Reset Command

With the first execution of the software reset command, all configuration registers are initialized to default values if bit ASIC_CNFG_1[CNFG_LOCK]='0'.
If bit ASIC_CNFG_1[CNFG_LOCK]='1' all configuration registers are initialized to default values except register ASIC_CNFG_1 and ASIC_CNFG_2.

With the second execution of the software reset command, the bit ASIC_CNFG_1[CNFG_LOCK] is reset to '0'.

The Software Reset Command includes 1 UART frame only:
UART Frame 1: Command bits cmd[4:0]; Channel Identifier ChId[2:0]

Table 6.2.4.11-1: Software Reset Command

Software Reset Command	*Command [7:3]*	*Channel ID [2:0]*
Software Reset	10101	000

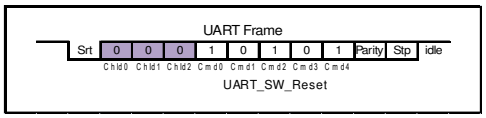


Figure 6.2.4.11-1: Software Reset Command Frame

6.2.4.12 Response to Read Register Command

Each valid read command, received by the transceiver ASIC, results in a response sequence including 5 UART Frames.
UART Frame 1: Channel Identifier ChId[2:0]; Frame Identifier Fid[2:0]; Error bits Err[1:0]
UART Frame 2: Command response CmdRes[4:0]; Channel Identifier[2:0]= copy from UART frame 1 of read request
UART Frame 3: Data Low Byte D[7:0]
UART Frame 4: Data Low Byte D[15:8]
UART Frame 5: Stuffing bits Stuff[1:0]; 6bit checksum XCRC[5:0]

Following table shows the bit configuration of UART Frame 1 including ChId, Fid and Err bits.
Table 6.2.4.12-1: Response To Read Command Bit Configuration

Response to Read Register: Configuration of UART Frame 1	*Error bits[7:6]*	*Frame ID[5:3]*	*Channel ID[2:0]*
Error bit - no ASIC error	00	000	000
Error bit - interface error	01	000	000
Error bit - ASIC error	10	000	000
Error bit - ASIC and interface error	11	000	000

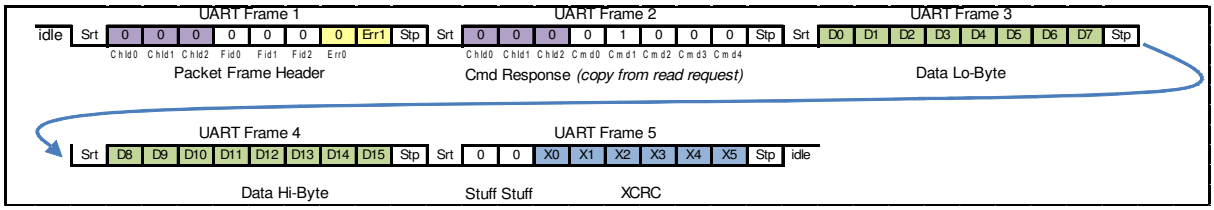


Figure 6.2.4.12-1: Response to Read Register Command Packet Frame

6.2.4.13 Transfer PSI5 Data

Incoming PSI5 data frames are processed and transmitted to the µController in UART frames.
The sequence includes 3 - 6 UART frames, depending on the length of the corresponding PSI5 frame.

Example: Frame configuration for minimum packet frame (according to v1.3):
UART Frame 1: Channel Identifier Chld[2:0]; Frame Identifier Fid[2:0]; Error bits Err[1:0]
UART Frame 2: Data bits D[7:0]
UART Frame 3: Parity; Stuffing bit Stuff; 6bit checksum XCRC[5:0]

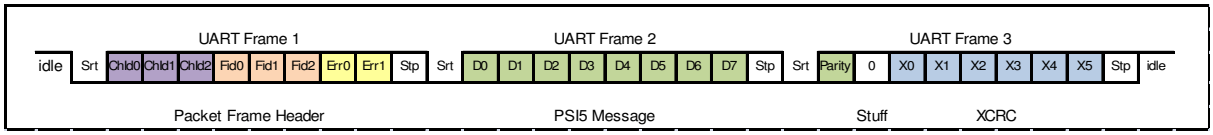


Figure 6.2.4.13-1: Example: Upload PSI5 Data Minimum Packet Frame

Example: Frame configuration for maximum Packet Frame (according to v2.0):
UART Frame 1: Channel Identifier Chld[2:0]; Frame Identifier Fid[2:0]; Error bits Err[1:0]
UART Frame 2: Data bits D[7:0]
UART Frame 3: Data bits D[15:8]
UART Frame 4: Data bits D[23:16]
UART Frame 5: Data bits D[27:24]; 3bit checksum C[2:0]; Stuffing bit Stuff
UART Frame 6: Stuffing bits Stuff[1:0]; 6bit checksum XCRC[5:0]

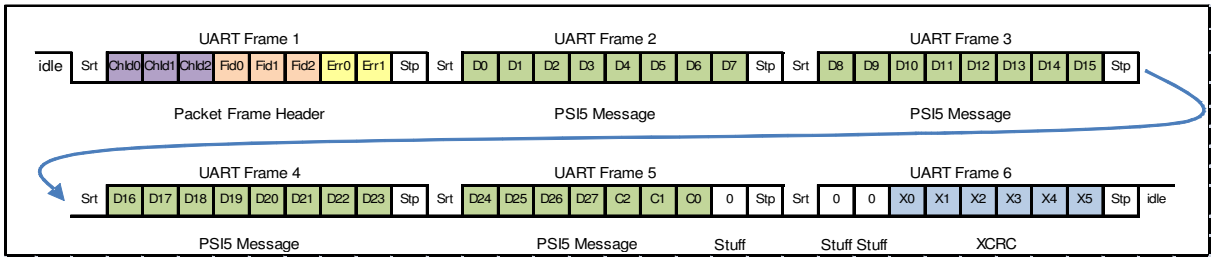


Figure 6.2.4.13-2: Example: Upload PSI5 Data Maximum Packet Frame

Following table shows the bit configuration of UART Frame 1 including ChId, Fid and Err bits.

Table 6.2.4.13-1: PSI5 Data UART Frame1 Bit Configuration

PSI5 data: Configuration of UART Frame 1	*Error bits*	*Frame ID*	*Channel ID*
Identifier for channel0 (diagnosis)	xx	xxx	000
Identifier for channel1	xx	xxx	001
Identifier for channel2	xx	xxx	010
Identifier for channel3	xx	xxx	011
Identifier for channel4	xx	xxx	100
Identifier for frame1	xx	000	xxx
Identifier for frame2	xx	001	xxx
Identifier for frame3	xx	010	xxx
Identifier for frame4	xx	011	xxx
Identifier for frame5	xx	100	xxx
Identifier for frame6	xx	101	xxx
Error bit - no error	00	xxx	xxx
Error bit - Interface error	01	xxx	xxx
Error bit - ASIC error	10	xxx	xxx
Error bit - Interface + ASIC error	11	xxx	xxx

6.2.5 XCRC[5:0] Calculation

A 6-bit XCRC for error detection is calculated and added at the last UART/SPI frame, transferred from transceiver to µC at pin SDO_TXD, for the defined packet frames.
The generator polynomial of the six bit CRC is g(x) = $X^6+X^4+X^3$ + 1 with a binary CRC initialization value "010101". The transmitter extends the data bits by six zeros (= XCRC default condition) as shown in the figures above. This augmented data word is fed (LSB first) into the shift registers of the CRC generator.

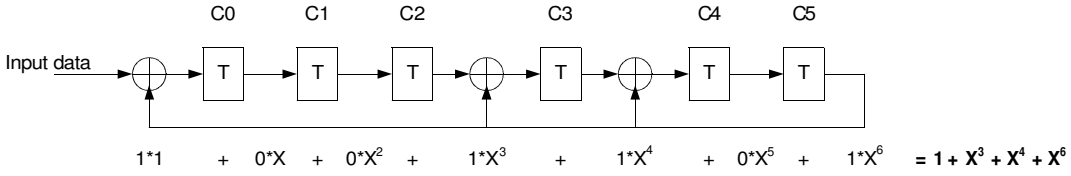


Figure 6.2.5-1: XCRC-calculation for SPI frames

UART Packet Frames:
The sequence of bit shift into the register for the CRC calculation is shown in below, starting with LSB first. The number of stuffing bits varies with the payload (not shown in the figures below).

1. **Transfer PSI5 Data**

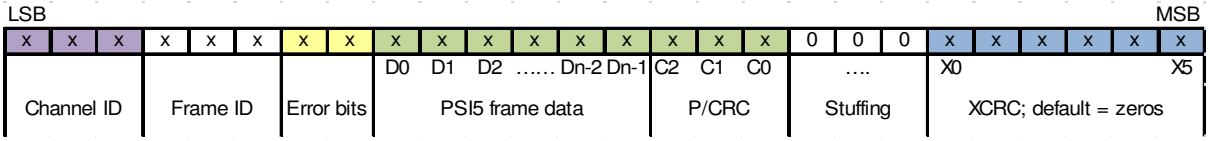


Figure 6.2.5-2: XCRC: Example Transfer PSI5 Data

2. **Response to Read Register Command**

Figure 6.2.5-3: XCRC: Example Response to Read Command

SPI Packet Frames:
The sequence is done in the similar way than for UART Packet frames, except
- Starting with MSB first
- Changed payload (e.g. additional Buffer ID, SYNC_LONG bits)

Example Read Sensor Data 24bit:

Figure 6.2.5-4: XCRC Example Read Sensor Data 24bit

6.2.6 CONFIGURATION

6.2.6.1 ASIC Configuration

The device can be configured and maintained with configuration, diagnosis and error registers.
Every register contains 16 bits, so only 16 bit read/write requests are processed.

Any of the four device channels can be configured independently by writing the read/write (R/W) configuration registers ASIC_CNFG_1, ASIC_CNFG_2 and ASIC_CNFG_3.
The following parameters can be modified per channel:
- current threshold for the data comparator (ΔIs_CHx)
- sync sustain voltage V3 (VSYNC_V3_CHx)
- channel configuration of synchronous / asynchronous mode (ASYNC_CHx)
- PSI5 bit time [kbps] / Baud rate per channel (PSI5_BIT_TIME_CHx)
- enabling of interfaces SIF_CHx (EN_CHx)

The detailed settings are described in the register table below:

Table 6.2.6.1-1: ASIC CONFIGURATION

Register Name	*Address*	*Description*
ASIC_CNFG_1	0x00	ASIC Configuration Register 1
ASIC_CNFG_2	0x01	ASIC Configuration Register 2
ASIC_CNFG_3	0x02	ASIC Configuration Register 3

Reading of unused bits will always return '0' and writing of unused bits don't care. Writing of read-only- or read-on clear-registers, don't care. For SPI accesses the response via SDO_TXD is the echo of the write request (identically behaviour than for write on read/write-registers).

Table 6.2.6.1-2: Register **ASIC_CNFG_1** (0x00) ASIC Configuration Register 1

	MSB														***LSB***
Content	CNFG_LOCK	-	-	-	MCD_DATA_CMP_W[1:0]		VSYNC_V3_CH4	VSYNC_V3_CH3	VSYNC_V3_CH2	VSYNC_V3_CH1	ΔIS_CH4	ΔIS_CH3	ΔIS_CH2	ΔIS_CH1	V_BUS[1:0]
Reset value	0	0	0	0	00		0	0	0	0	0	0	0	0	00
Access	R/W	R	R	R	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**CNFG_LOCK** : lock bit for configuration registers 0b0: registers ASIC_CNFG_1 and ASIC_CNFG_2 are not locked, an update is possible 0b1: registers ASIC_CNFG_1 and ASIC_CNFG_2 are locked, no update possible (exception: The 2nd SW_reset command resets the lock and allows this two registers to be updated) **MCD_DATA_CMP_W[1:0]** : Manchester data compare window setting 0b00: DATA_EDGE = 18 clock counts (low sensitive) & COMPENSATION_WINDOW = 23 clock counts @4MHz: DATA_E=(18*250ns = 4.5us; CMP=23*250ns=5.75us; => Total=10.25us @6MHz: DATA_E=18*167ns = 3us; CMP=23*167ns=3.83us; => Total = 6.83us 0b01: DATA_EDGE = 12 clock counts (low sensitive) & COMPENSATION_WINDOW = 26 clock counts @4MHz: DATA_E=12*250ns = 3us; CMP=26*250ns=6.5us; => Total=9.5us @6MHz: DATA_E=12*167ns = 2us; CMP=26*167ns=4.33us; => Total = 6.33us 0b10: DATA_EDGE = 8 clock counts (low sensitive) & COMPENSATION_WINDOW = 28 clock counts @4MHz: DATA_E=8*250ns = 2us; CMP=28*250ns=7us; => Total=9us @6MHz: DATA_E=8*167ns = 1.33us; CMP=28*167ns=4.67us; => Total = 6us **VSYNC_V3_CH4** : sync sustain voltage V3 (VSYNC_V3_CHx) 0b0: V3 = 4.8V typical (common mode) 0b1: V3 = 3.7V typical (low power mode) **VSYNC_V3_CH3** : sync sustain voltage V3 (VSYNC_V3_CHx) 0b0: V3 = 4.8V typical (common mode) 0b1: V3 = 3.7V typical (low power mode) **VSYNC_V3_CH2** : sync sustain voltage V3 (VSYNC_V3_CHx) 0b0: V3 = 4.8V typical (common mode) 0b1: V3 = 3.7V typical (low power mode) **VSYNC_V3_CH1** : sync sustain voltage V3 (VSYNC_V3_CHx) 0b0: V3 = 4.8V typical (common mode) 0b1: V3 = 3.7V typical (low power mode) **ΔIS_CH4** : current threshold for the data comparator (ΔIs_CHx) 0b0: ΔIS = 26mA 0b1: ΔIS = 13mA **ΔIS_CH3** : current threshold for the data comparator (ΔIs_CHx) 0b0: ΔIS = 26mA 0b1: ΔIS = 13mA **ΔIS_CH2** : current threshold for the data comparator (ΔIs_CHx) 0b0: ΔIS = 26mA 0b1: ΔIS = 13mA **ΔIS_CH1** : current threshold for the data comparator (ΔIs_CHx) 0b0: ΔIS = 26mA 0b1: ΔIS = 13mA **V_BUS[1:0]** : V_{BUS} selection 0b00: LDO disabled; V_{BUS} must be supplied externaly 0b01: VBUS = 5.15V 0b10: VBUS = 6.65V 0b11: VBUS = 7.7V														

Table 6.2.6.1-3: Register **ASIC_CNFG_2** (0x01) ASIC Configuration Register 2

	MSB															***LSB***
Content	-	-	UART_IDLE_TIME[3:0]				REV_CUR_CH_DIS	IDAC_RES	PSI5_BIT_TIME_CH4	PSI5_BIT_TIME_CH3	PSI5_BIT_TIME_CH2	PSI5_BIT_TIME_CH1	ASYNC_CH4	ASYNC_CH3	ASYNC_CH2	ASYNC_CH1
Reset value	0	0	0000				0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**UART_IDLE_TIME[3:0]** : UART idle time between two consecutive UART packet frames (to enable a re-synchronization) 0b0000: minimum idle time = DEFAULT 0b1111: maximum idle time **REV_CUR_CH_DIS** : Disable of channels for reverse current condition 0b0: disabled -> no switch-off of channels by IC (default) 0b1: enabled -> switch-off dedicated channel if REV_CUR_CHx='1' **IDAC_RES** : IDAC resolution 0b0: 300 uA per LSB (default) 0b1: 200 uA per LSB **PSI5_BIT_TIME_CH4** : PSI5 bit time 0b0: bit time equal to 8us (=125kbps) 0b1: bit time equal to 5.3us (=189kbps) **PSI5_BIT_TIME_CH3** : PSI5 bit time 0b0: bit time equal to 8us (=125kbps) 0b1: bit time equal to 5.3us (=189kbps) **PSI5_BIT_TIME_CH2** : PSI5 bit time 0b0: bit time equal to 8us (=125kbps) 0b1: bit time equal to 5.3us (=189kbps) **PSI5_BIT_TIME_CH1** : PSI5 bit time 0b0: bit time equal to 8us (=125kbps) 0b1: bit time equal to 5.3us (=189kbps) **ASYNC_CH4** : channel mode configuration 0b0: channel in synchronous configuration 0b1: channel in asynchronous configuration **ASYNC_CH3** : channel mode configuration 0b0: channel in synchronous configuration 0b1: channel in asynchronous configuration **ASYNC_CH2** : channel mode configuration 0b0: channel in synchronous configuration 0b1: channel in asynchronous configuration **ASYNC_CH1** : channel mode configuration 0b0: channel in synchronous configuration 0b1: channel in asynchronous configuration																

Table 6.2.6.1-4: Register **ASIC_CNFG_3** (0x02) ASIC Configuration Register 3

	MSB															***LSB***
Content	-	BL_CHAN-NEL4	BL_CHAN-NEL3	BL_CHAN-NEL2	BL_CHAN-NEL1	GEN_FUSE_RD	EN_LOOP[2:0]			EN_CP_SYNC	EN_UART_TXD_PAR-ITY	EN_UART_RXD_PAR-ITY	EN_CH4	EN_CH3	EN_CH2	EN_CH1
Reset value	0	0	0	0	0	0	000			0	1	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W			R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**BL_CHANNEL4** : blanking time of MCD/SYNC generation/ovc after channel enable 0=5ms 1=10ms **BL_CHANNEL3** : blanking time of MCD/SYNC generation/ovc after channel enable 0=5ms 1=10ms **BL_CHANNEL2** : blanking time of MCD/SYNC generation/ovc after channel enable 0=5ms 1=10ms **BL_CHANNEL1** : blanking time of MCD/SYNC generation/ovc after channel enable 0=5ms 1=10ms **GEN_FUSE_RD** : Start fuse read out via UART/SPI 0b0: no fuse read out 0b1: start additional fuse read out **EN_LOOP[2:0]** : enable channel in loop back test mode 0b000: all Channel in normal operation 0b001: Channel1 loop back test mode enabled 0b010: Channel2 loop back test mode enabled 0b011: Channel3 loop back test mode enabled 0b100: Channel4 loop back test mode enabled **EN_CP_SYNC** : Enable Sync pulse charge pump 0b0:disabled 0b1:enabled **EN_UART_TXD_PARITY** : Enable parity bit addition for UART Tx frames 0b0:disabled 0b1:enabled **EN_UART_RXD_PARITY** : Enable parity check for UART received frames 0b0:disabled 0b1:enabled **EN_CH4** : Enable Interface SIFx 0b0: Disable PSI5 Interface 0b1: Enable PSI5 Interface **EN_CH3** : Enable Interface SIFx 0b0: Disable PSI5 Interface 0b1: Enable PSI5 Interface **EN_CH2** : Enable Interface SIFx 0b0: Disable PSI5 Interface 0b1: Enable PSI5 Interface **EN_CH1** : Enable Interface SIFx 0b0: Disable PSI5 Interface 0b1: Enable PSI5 Interface															

6.2.6.1.1 Asynchronous mode

Note: Only one sensor allowed per SIFx.

With enable of SIFx via configuration register ASIC_CNFG_3[EN_CHx], the sensor is supplied with voltage VSIFx and starts to transmit PSI5 sensor frames.
For received frames, the implemented Manchester decoder adds to each valid frame the Fid ="0b001".

For UART interface, the Packet frame is transferred to uC automatically. With appropriate UART baud rate, the IC transmits the data to the uC without any overwriting.

For SPI interface, the decoded frame is available in BID[0] of SPI data buffer. The uC has to ensure to read BID[0] before a new PSI5 frame is decoded; otherwise it's overwritten.

6.2.6.2 Timeslot Configuration

For every channel there are seven configuration registers available to configure the following parameters:

- six independent configurable PSI5 timeslots
- timeslot length
- frame length
- parity or crc selection
- error check enabling
- desired delay of sync pulse generation
- mandatory buffer for SPI access Details are described in the following register table.

Table 6.2.6.2-1: CHANNEL_CONFIGURATION

Register Name	*Address*	*Description*
CH1_CFG1	0x03	Channel 1 Configuration Register 1
CH1_CFG2	0x04	Channel 1 Configuration Register 2
CH1_CFG3	0x05	Channel 1 Configuration Register 3
CH1_CFG4	0x06	Channel 1 Configuration Register 4
CH1_CFG5	0x07	Channel 1 Configuration Register 5
CH1_CFG6	0x08	Channel 1 Configuration Register 6
CH1_CFG7	0x09	Channel 1 Configuration Register 7
CH2_CFG1	0x0A	Channel 2 Configuration Register 1
CH2_CFG2	0x0B	Channel 2 Configuration Register 2
CH2_CFG3	0x0C	Channel 2 Configuration Register 3
CH2_CFG4	0x0D	Channel 2 Configuration Register 4
CH2_CFG5	0x0E	Channel 2 Configuration Register 5
CH2_CFG6	0x0F	Channel 2 Configuration Register 6
CH2_CFG7	0x10	Channel 2 Configuration Register 7
CH3_CFG1	0x11	Channel 3 Configuration Register 1
CH3_CFG2	0x12	Channel 3 Configuration Register 2
CH3_CFG3	0x13	Channel 3 Configuration Register 3
CH3_CFG4	0x14	Channel 3 Configuration Register 4
CH3_CFG5	0x15	Channel 3 Configuration Register 5
CH3_CFG6	0x16	Channel 3 Configuration Register 6
CH3_CFG7	0x17	Channel 3 Configuration Register 7

Register Name	*Address*	*Description*
CH4_CFG1	0x18	Channel 4 Configuration Register 1
CH4_CFG2	0x19	Channel 4 Configuration Register 2
CH4_CFG3	0x1A	Channel 4 Configuration Register 3
CH4_CFG4	0x1B	Channel 4 Configuration Register 4
CH4_CFG5	0x1C	Channel 4 Configuration Register 5
CH4_CFG6	0x1D	Channel 4 Configuration Register 6
CH4_CFG7	0x1E	Channel 4 Configuration Register 7

It is highly recommended, not to change the registers CHX_CFG1(IDAC_CNT_MODE, IDAC_CNT_INC2[1:0], IDAC_CNT_INC1[1:0]) and CHX_CFG2(IDAC_CNT_DEC2[1:0], IDAC_CNT_DEC1[1:0]) since these registers control the Ibase tracking function!

Table 6.2.6.2-2: Register **CH1_CFG1** (0x03) Channel 1 Configuration Register 1

	MSB															***LSB***
Content	IDAC_CNT_MODE	IDAC_CNT_INC2[1:0]		IDAC_CNT_INC1[1:0]		EN_ER_CHK	T1_CRC	TS1_FLEN[4:0]					T1_LEN[3:0]			
Reset value	0	00		00		0	0	00011					0100			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_MODE** : reserved **IDAC_CNT_INC2[1:0]** : reserved **IDAC_CNT_INC1[1:0]** : reserved **EN_ER_CHK** : Enable parity/CRC check functionality 0b0: disable functionality 0b1: enable functionality **T1_CRC** : PSI5 frame error detection mode of frames starting in timeslot 1 0b0: PSI5 Sensor in parity mode 0b1: PSI5 Sensor in CRC mode **TS1_FLEN[4:0]** : PSI5 frame length of frames starting in timeslot 1 frame length includes start bit + data + parity/crc $[TSx\_FLEN]_{16} = [Frame\ length]_{10} - [10]_{10}$ 0x0 = bit length of zero (=no frame) 0x01 - 0x17: Frame length => [11..33] 0x18 - 0x1F: reserved Default: P10P (Airbag) = 2 + 10 + 1 = 13->0x3 **T1_LEN[3:0]** : Timeslot 1 Length 0b_nnnn: nnnn x 32 us => [0us..480us] Default: t = 4*32us = 128us															

Table 6.2.6.2-3: Register **CH1_CFG2** (0x04) Channel 1 Configuration Register 2

	MSB															***LSB***
Content	-	IDAC_CNT_DEC2[1:0]		IDAC_CNT_DEC1[1:0]		EN_ER_CHK	T2_CRC	TS2_FLEN[4:0]					T2_LEN[3:0]			
Reset value	0	01		01		0	0	00011					0101			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_DEC2[1:0]** : reserved **IDAC_CNT_DEC1[1:0]** : reserved **EN_ER_CHK** : Enable parity/CRC check functionality 0b0: disable functionality 0b1: enable functionality **T2_CRC** : PSI5 frame error detection mode of frames starting in timeslot 2 0b0: PSI5 Sensor in parity mode 0b1: PSI5 Sensor in CRC mode **TS2_FLEN[4:0]** : PSI5 frame length of frames starting in timeslot 2 frame length includes start bit + data + parity/crc $[TSx\_FLEN]_{16} = [Frame\ length]_{10} - [10]_{10}$ 0x0 = bit length of zero (=no frame) 0x01 - 0x17: Frame length => [11..33] 0x18-0x1F:reserved Default: P10P (Airbag) = 2 + 10 + 1 = 13->0x3 **T2_LEN[3:0]** : Timeslot 2 Length 0b_nnnn: nnnn x 32 us => [0us..480us] Default: t = 5*32us = 160us															

Table 6.2.6.2-4: Register **CH1_CFG3** (0x05) Channel 1 Configuration Register 3

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T3_CRC	TS3_FLEN[4:0]					T3_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00011					0101			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : Enable parity/CRC check functionality 0b0: disable functionality 0b1: enable functionality **T3_CRC** : PSI5 frame error detection mode of frames starting in timeslot 3 0b0: PSI5 Sensor in parity mode 0b1: PSI5 Sensor in CRC mode **TS3_FLEN[4:0]** : PSI5 frame length of frames starting in timeslot 3 frame length includes start bit + data + parity/crc $[TSx\_FLEN]_{16} = [Frame\ length]_{10} - [10]_{10}$ 0x0 = bit length of zero (=no frame) 0x01 - 0x17: Frame length => [11..33] 0x18 - 0x1F: reserved Default: P10P (Airbag) = 2 + 10 + 1 = 13->0x3 **T3_LEN[3:0]** : Timeslot 3 Length 0b_nnnn: nnnn x 32 us => [0us..480us] Default: t = 5*32us = 160us															

Table 6.2.6.2-5: Register **CH1_CFG4** (0x06) Channel 1 Configuration Register 4

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T4_CRC	TS4_FLEN[4:0]					T4_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : Enable parity/CRC check functionality 0b0: disable functionality 0b1: enable functionality **T4_CRC** : PSI5 frame error detection mode of frames starting in timeslot 4 0b0: PSI5 Sensor in parity mode 0b1: PSI5 Sensor in CRC mode **TS4_FLEN[4:0]** : PSI5 frame length of frames starting in timeslot 4 frame length includes start bit + data + parity/crc $[TSx\_FLEN]_{16} = [Frame\ length]_{10} - [10]_{10}$ 0x0 = bit length of zero (=no frame) 0x01 - 0x17: Frame length => [11..33] 0x18-0x1F:reserved Default: = 0 **T4_LEN[3:0]** : Timeslot 4 Length 0b_nnnn: nnnn x 32 us => [0us..480us] Default: t = 0*32us = 0us															

Table 6.2.6.2-6: Register **CH1_CFG5** (0x07) Channel 1 Configuration Register 5

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T5_CRC	TS5_FLEN[4:0]					T5_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : Enable parity/CRC check functionality 0b0: disable functionality 0b1: enable functionality **T5_CRC** : PSI5 frame error detection mode of frames starting in timeslot 5 0b0: PSI5 Sensor in parity mode 0b1: PSI5 Sensor in CRC mode **TS5_FLEN[4:0]** : PSI5 frame length of frames starting in timeslot 5 frame length includes start bit + data + parity/crc $[TSx\_FLEN]_{16} = [Frame\ length]_{10} - [10]_{10}$ 0x0 = bit length of zero (=no frame) 0x01 - 0x17: Frame length => [11..33] 0x18 - 0x1F: reserved Default: = 0 **T5_LEN[3:0]** : Timeslot 5 Length 0b_nnnn: nnnn x 32 us => [0us..480us] Default: t = 0*32us = 0us															

Table 6.2.6.2-7: Register **CH1_CFG6** (0x08) Channel 1 Configuration Register 6

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T6_CRC	TS6_FLEN[4:0]					T6_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : Enable parity/CRC check functionality 0b0: disable functionality 0b1: enable functionality **T6_CRC** : PSI5 frame error detection mode of frames starting in timeslot 6 0b0: PSI5 Sensor in parity mode 0b1: PSI5 Sensor in CRC mode **TS6_FLEN[4:0]** : PSI5 frame length of frames starting in timeslot 6 frame length includes start bit + data + parity/crc $[TSx\_FLEN]_{16} = [Frame\ length]_{10} - [10]_{10}$ 0x0 = bit length of zero (=no frame) 0x01 - 0x17: Frame length => [11..33] 0x18-0x1F:reserved Default:= 0 **T6_LEN[3:0]** : Timeslot 6 Length 0b_nnnn: nnnn x 32 us => [0us..480us] Default: t = 0*32us = 0us															

Table 6.2.6.2-8: Register **CH1_CFG7** (0x09) Channel 1 Configuration Register 7

	MSB															***LSB***
Content	-	-	-	-	SPI_BUF-FER_CNFG[1:0]		SYNC_DLY[9:0]									
Reset value	0	0	0	0	11		0000									
Access	R/W	R/W	R/W	R/W	R/W		R/W									
Bit Description	**SPI_BUFFER_CNFG[1:0]** : SPI buffer (=96bit) configuration 0b00: 48bit/buffer;2 partial buffers; Buffer identifiers[0,1] 0b01: 32bit/buffer;3 partial buffers; Buffer identifiers[0,1,2] 0b10: 24bit/buffer;4 partial buffers; Buffer identifiers[0,1,2,3] 0b11: 16bit/buffer;6 partial buffers; Buffer identifiers[0,1,2,3,4,5](=default) **SYNC_DLY[9:0]** : Sync pulse delay 0xnnn: nnn x 8/fCLK_INT =>[0us..682us]															

Table 6.2.6.2-9: Register **CH2_CFG1** (0x0A) Channel 2 Configuration Register 1

	MSB															***LSB***
Content	IDAC_CNT_MODE	IDAC_CNT_INC2[1:0]		IDAC_CNT_INC1[1:0]		EN_ER_CHK	T1_CRC	TS1_FLEN[4:0]					T1_LEN[3:0]			
Reset value	0	00		00		0	0	00011					0100			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_MODE** : reserved **IDAC_CNT_INC2[1:0]** : reserved **IDAC_CNT_INC1[1:0]** : reserved **EN_ER_CHK** : see CH1_CFG1 **T1_CRC** : see CH1_CFG1 **TS1_FLEN[4:0]** : see CH1_CFG1 **T1_LEN[3:0]** : see CH1_CFG1															

Table 6.2.6.2-10: Register **CH2_CFG2** (0x0B) Channel 2 Configuration Register 2

	MSB															***LSB***
Content	-	IDAC_CNT_DEC2[1:0]		IDAC_CNT_DEC1[1:0]		EN_ER_CHK	T2_CRC	TS2_FLEN[4:0]					T2_LEN[3:0]			
Reset value	0	01		01		0	0	00011					0101			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_DEC2[1:0]** : reserved **IDAC_CNT_DEC1[1:0]** : reseved **EN_ER_CHK** : see CH1_CFG2 **T2_CRC** : see CH1_CFG2 **TS2_FLEN[4:0]** : see CH1_CFG2 **T2_LEN[3:0]** : see CH1_CFG2															

Table 6.2.6.2-11: Register **CH2_CFG3** (0x0C) Channel 2 Configuration Register 3

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T3_CRC	TS3_FLEN[4:0]					T3_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00011					0101			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG3 **T3_CRC** : see CH1_CFG3 **TS3_FLEN[4:0]** : see CH1_CFG3 **T3_LEN[3:0]** : see CH1_CFG3															

Table 6.2.6.2-12: Register **CH2_CFG4** (0x0D) Channel 2 Configuration Register 4

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T4_CRC	TS4_FLEN[4:0]					T4_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG4 **T4_CRC** : see CH1_CFG4 **TS4_FLEN[4:0]** : see CH1_CFG4 **T4_LEN[3:0]** : see CH1_CFG4															

Table 6.2.6.2-13: Register **CH2_CFG5** (0x0E) Channel 2 Configuration Register 5

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T5_CRC	TS5_FLEN[4:0]					T5_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG5 **T5_CRC** : see CH1_CFG5 **TS5_FLEN[4:0]** : see CH1_CFG5 **T5_LEN[3:0]** : see CH1_CFG5															

Table 6.2.6.2-14: Register **CH2_CFG6** (0x0F) Channel 2 Configuration Register 6

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T6_CRC	TS6_FLEN[4:0]					T6_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG6 **T6_CRC** : see CH1_CFG6 **TS6_FLEN[4:0]** : see CH1_CFG6 **T6_LEN[3:0]** : see CH1_CFG6															

Table 6.2.6.2-15: Register **CH2_CFG7** (0x10) Channel 2 Configuration Register 7

	MSB															***LSB***
Content	-	-	-	-	SPI_BUF-FER_CNFG[1:0]		SYNC_DLY[9:0]									
Reset value	0	0	0	0	11		0000									
Access	R/W	R/W	R/W	R/W	R/W		R/W									
Bit Description	**SPI_BUFFER_CNFG[1:0]** : see CH1_CFG7 **SYNC_DLY[9:0]** : see CH1_CFG7															

Table 6.2.6.2-16: Register **CH3_CFG1** (0x11) Channel 3 Configuration Register 1

	MSB															***LSB***
Content	IDAC_CNT_MODE	IDAC_CNT_INC2[1:0]		IDAC_CNT_INC1[1:0]		EN_ER_CHK	T1_CRC	TS1_FLEN[4:0]					T1_LEN[3:0]			
Reset value	0	00		00		0	0	00011					0100			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_MODE** : reserved **IDAC_CNT_INC2[1:0]** : reserved **IDAC_CNT_INC1[1:0]** : reserved **EN_ER_CHK** : see CH1_CFG1 **T1_CRC** : see CH1_CFG1 **TS1_FLEN[4:0]** : see CH1_CFG1 **T1_LEN[3:0]** : see CH1_CFG1															

Table 6.2.6.2-17: Register **CH3_CFG2** (0x12) Channel 3 Configuration Register 2

	MSB															***LSB***
Content	-	IDAC_CNT_DEC2[1:0]		IDAC_CNT_DEC1[1:0]		EN_ER_CHK	T2_CRC	TS2_FLEN[4:0]					T2_LEN[3:0]			
Reset value	0	01		01		0	0	00011					0101			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_DEC2[1:0]** : reserved **IDAC_CNT_DEC1[1:0]** : reserved **EN_ER_CHK** : see CH1_CFG2 **T2_CRC** : see CH1_CFG2 **TS2_FLEN[4:0]** : see CH1_CFG2 **T2_LEN[3:0]** : see CH1_CFG2															

Table 6.2.6.2-18: Register **CH3_CFG3** (0x13) Channel 3 Configuration Register 3

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T3_CRC	TS3_FLEN[4:0]					T3_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00011					0101			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG3 **T3_CRC** : see CH1_CFG3 **TS3_FLEN[4:0]** : see CH1_CFG3 **T3_LEN[3:0]** : see CH1_CFG3															

Table 6.2.6.2-19: Register **CH3_CFG4** (0x14) Channel 3 Configuration Register 4

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T4_CRC	TS4_FLEN[4:0]					T4_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG4 **T4_CRC** : see CH1_CFG4 **TS4_FLEN[4:0]** : see CH1_CFG4 **T4_LEN[3:0]** : see CH1_CFG4															

Table 6.2.6.2-20: Register **CH3_CFG5** (0x15) Channel 3 Configuration Register 5

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T5_CRC	TS5_FLEN[4:0]					T5_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG5 **T5_CRC** : see CH1_CFG5 **TS5_FLEN[4:0]** : see CH1_CFG5 **T5_LEN[3:0]** : see CH1_CFG5															

Table 6.2.6.2-21: Register **CH3_CFG6** (0x16) Channel 3 Configuration Register 6

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T6_CRC	TS6_FLEN[4:0]					T6_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG6 **T6_CRC** : see CH1_CFG6 **TS6_FLEN[4:0]** : see CH1_CFG6 **T6_LEN[3:0]** : see CH1_CFG6															

Table 6.2.6.2-22: Register **CH3_CFG7** (0x17) Channel 3 Configuration Register 7

	MSB															***LSB***
Content	-	-	-	-	SPI_BUF-FER_CNFG[1:0]		SYNC_DLY[9:0]									
Reset value	0	0	0	0	11		0000									
Access	R/W	R/W	R/W	R/W	R/W		R/W									
Bit Description	**SPI_BUFFER_CNFG[1:0]** : see CH3_CFG7 **SYNC_DLY[9:0]** : see CH3_CFG7															

Table 6.2.6.2-23: Register **CH4_CFG1** (0x18) Channel 4 Configuration Register 1

	MSB															***LSB***
Content	IDAC_CNT_MODE	IDAC_CNT_INC2[1:0]		IDAC_CNT_INC1[1:0]		EN_ER_CHK	T1_CRC	TS1_FLEN[4:0]					T1_LEN[3:0]			
Reset value	0	00		00		0	0	00011					0100			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_MODE** : reserved **IDAC_CNT_INC2[1:0]** : reserved **IDAC_CNT_INC1[1:0]** : reserved **EN_ER_CHK** : see CH1_CFG1 **T1_CRC** : see CH1_CFG1 **TS1_FLEN[4:0]** : see CH1_CFG1 **T1_LEN[3:0]** : see CH1_CFG1															

Table 6.2.6.2-24: Register **CH4_CFG2** (0x19) Channel 4 Configuration Register 2

	MSB															***LSB***
Content	-	IDAC_CNT_DEC2[1:0]		IDAC_CNT_DEC1[1:0]		EN_ER_CHK	T2_CRC	TS2_FLEN[4:0]					T2_LEN[3:0]			
Reset value	0	01		01		0	0	00011					0101			
Access	R/W	R/W		R/W		R/W	R/W	R/W					R/W			
Bit Description	**IDAC_CNT_DEC2[1:0]** : reserved **IDAC_CNT_DEC1[1:0]** : reserved **EN_ER_CHK** : see CH1_CFG2 **T2_CRC** : see CH1_CFG2 **TS2_FLEN[4:0]** : see CH1_CFG2 **T2_LEN[3:0]** : see CH1_CFG2															

Table 6.2.6.2-25: Register **CH4_CFG3** (0x1A) Channel 4 Configuration Register 3

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T3_CRC	TS3_FLEN[4:0]					T3_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00011					0101			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG3 **T3_CRC** : see CH1_CFG3 **TS3_FLEN[4:0]** : see CH1_CFG3 **T3_LEN[3:0]** : see CH1_CFG3															

Table 6.2.6.2-26: Register **CH4_CFG4** (0x1B) Channel 4 Configuration Register 4

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T4_CRC	TS4_FLEN[4:0]					T4_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG4 **T4_CRC** : see CH1_CFG4 **TS4_FLEN[4:0]** : see CH1_CFG4 **T4_LEN[3:0]** : see CH1_CGF4															

Table 6.2.6.2-27: Register **CH4_CFG5** (0x1C) Channel 4 Configuration Register 5

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T5_CRC	TS5_FLEN[4:0]					T5_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG5 **T5_CRC** : see CH1_CFG5 **TS5_FLEN[4:0]** : see CH1_CFG5 **T5_LEN[3:0]** : see CH1_CFG5															

Table 6.2.6.2-28: Register **CH4_CFG6** (0x1D) Channel 4 Configuration Register 6

	MSB															***LSB***
Content	-	-	-	-	-	EN_ER_CHK	T6_CRC	TS6_FLEN[4:0]					T6_LEN[3:0]			
Reset value	0	0	0	0	0	0	0	00000					0000			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					R/W			
Bit Description	**EN_ER_CHK** : see CH1_CFG6 **T6_CRC** : see CH1_CFG6 **TS6_FLEN[4:0]** : see CH1_CFG6 **T6_LEN[3:0]** : see CH1_CFG6															

Table 6.2.6.2-29: Register **CH4_CFG7** (0x1E) Channel 4 Configuration Register 7

	MSB															***LSB***
Content	-	-	-	-	SPI_BUFFER_CNFG[1:0]		SYNC_DLY[9:0]									
Reset value	0	0	0	0	11		0000									
Access	R/W	R/W	R/W	R/W	R/W		R/W									
Bit Description	**SPI_BUFFER_CNFG[1:0]** : see CH1_CGF7 **SYNC_DLY[9:0]** : see CH1_CGF7															

6.2.6.2.1 Timeslot Length

The timeslotx length (Bit TX_LEN) is used to assign the frame identifier (Fid) to received PSI5 frames.

Tx_LEN is implemented as a counter. Once loaded, it's counting down to 0.
T1_LEN is loaded with start of SYNC pulse (after SYNC_DLY has expired). If T1_LEN has expired, the following counter T2_LEN is loaded ... until T6_LEN has expired.
For TSX_LEN=0x00(=no frame) the TX_LEN counter is also loaded with 0 and expires with the next 2µs clock cycle.

The timeslot length (bit TX_LEN) is used to assign the frame identifier (fid) to decoded PSI5 frames. Following two examples based on PSI5-P10P-500/3L (Airbag), show the correlation of Fid to TX_LEN counter. The Fid is added to the PSI5 sensor data by the Manchester decoder (MD) once the first start bit (rising slope) is detected.
Example 1, default configuration; T3_LEN expires within frame3.

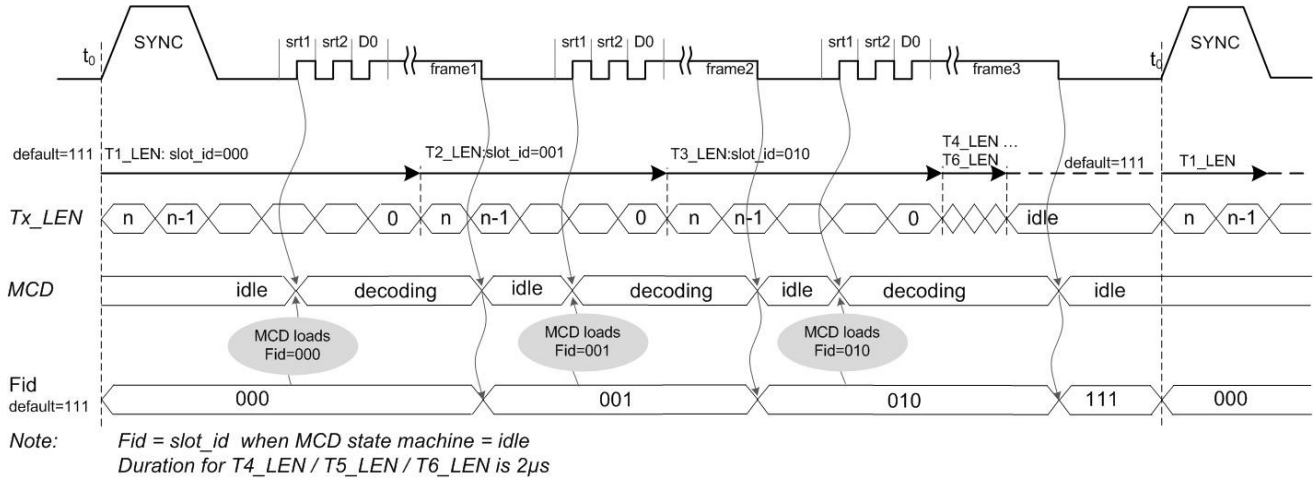


Figure 6.2.6.2.1-1: Example1: TxLEN Configuration

Example 2 default configuration;T3_LEN expires after frame3;MD_UNEX_FR_CHX_FX is possible:
Note that unexpected frame errors MD_UNEX_FR_CHx_F[4...6] are flagged if 2 valid start bits are decoded with 2nd start bit occures in T[4...6]_LEN (error condition, either frame too late, unexpected frame or TX_LEN configured wrong).

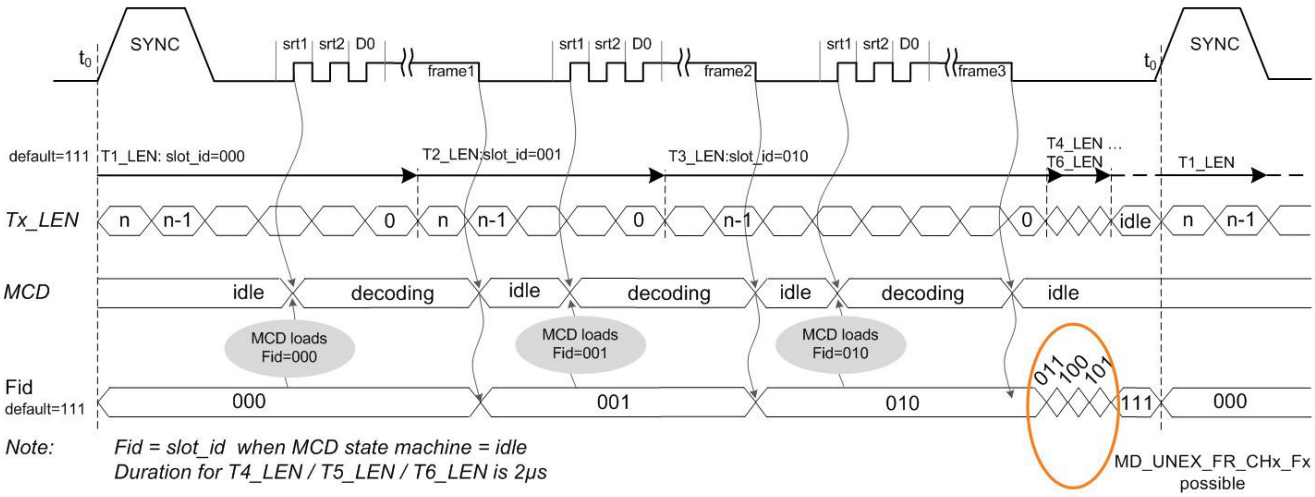


Figure 6.2.6.2.1-2: Example2: TxLEN Configuration

For active Tx_LEN counter any SYNC pulse trigger is masked to prevent an abort of Tx_LEN counter. This allows a faster ECU-2-sensor communication w/o change of register configuration.
The time slot ends with the last edge of the Data protocol.

Note: Decoded Manchester data will be discarded for a SYNC pulse trigger during active Tx_LEN counter to avoid storage / upload of corrupted data to uC. Error will be flagged in ERROR_STATUS_x[SYNC_DATA_INV_CH1]. With next regular SYNC trigger - after Tx_LEN counter is again in idle state - sensor data is stored / uploaded to uC.

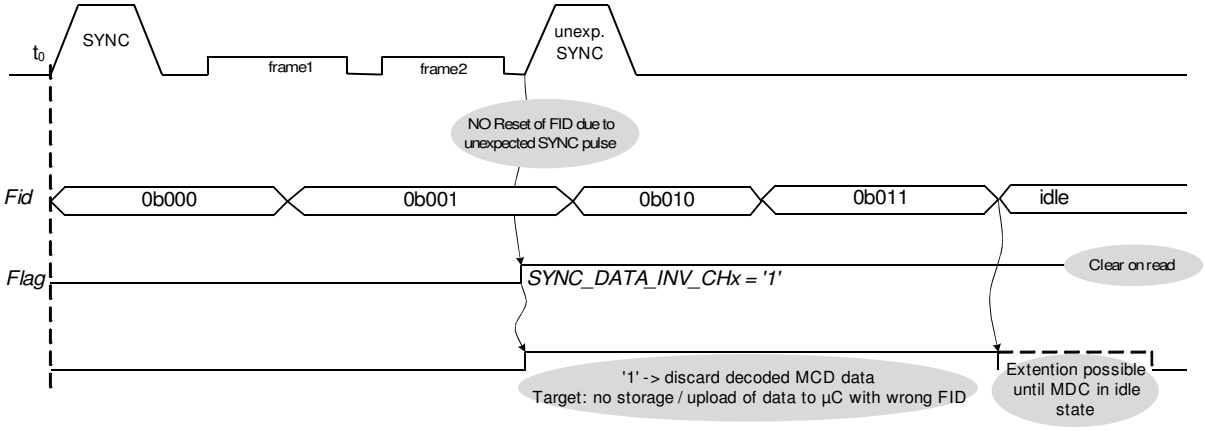


Figure 6.2.6.2.1-3: Example2: TxLEN Configuration: Unexptected Sync Pulse

6.2.6.3 Error Registers

There are ten error status registers available for reading, which are cleared on read (clear on read, RC).
The following error information is available:

- MD Unexpected frame for each frame and channel
- MD No frames for each frame and channel
- MD Frame error for each frame and channel
- MD Parity error for each frame and channel
- Reverse current status of each channel
- Buffer configuration error of each channel
- Diagnosis status of each channel
- Over current status of each channel
- UART/SPI status information (invalid address, invalid command, SPI clock erreor, UART read request collision)

Details are described in the following register table.

Table 6.2.6.3-1: Error Status Register

Register Name	*Address*	*Description*
ERROR_STATUS_1	0x25	Global ASIC errors
ERROR_STATUS_2	0x26	Channel errors
ERROR_STATUS_3	0x27	Four error bits per frame (1-4) channel 1
ERROR_STATUS_4	0x28	Four error bits per frame (5-6) channel 1 and analog errors
ERROR_STATUS_5	0x29	Four error bits per frame (1-4)channel 2
ERROR_STATUS_6	0x2A	Four error bits per frame (5-6)channel 2 and analog errors
ERROR_STATUS_7	0x2B	Four error bits per frame (1-4)channel 3
ERROR_STATUS_8	0x2C	Four error bits per frame (5-6)channel 3 and analog errors
ERROR_STATUS_9	0x2D	Four error bits per frame (1-4)channel 4
ERROR_STATUS_10	0x2E	Four error bits per frame (5-6)channel 4 and analog errors

Reading of unused bits will always return '0' and writing of unused bits don't care. Writing to read only or read on clear registers don't care. The SPI echo response to a write request is independently of register type (R/W, R, RC).

Table 6.2.6.3-2: Register **ERROR_STATUS_1** (0x25) Global ASIC errors

	MSB															***LSB***
Content	-	-	-	-	-	-	-	-	UART_SPI_INV_ADDRESS	VBUS_OV	DIAG_OT	SPI_CLK_ERR	UART_SPI_COL-LI-SION	UART_SPI_INV_CMD	UART_FERR	UART_PERR
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C1	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**UART_SPI_INV_ADDRESS** : UART/SPI address check 0b0: valid address 0b1: invalid address **VBUS_OV** : VBUS over voltage bit 0b0: no over voltage; signal vbus_ov_f = 0 0b1: over voltage; signal vbus_ov_f = 1 **DIAG_OT** : Overtemperatur bit 0b0: no overtemperature; signal i_ot = 0 0b1: overtemperature; signal i_ot = 1 **SPI_CLK_ERR** : SPI clock error 0b0: no clock error 0b1: SPI clock error (number of clock cycles ≠ 16) **UART_SPI_COLLISION** : UART/SPI read request collision status latch (clear on read) 0b0: no collision happend 0b1: UART/SPI read request received while last read was not completed yet **UART_SPI_INV_CMD** : UART/SPI command error status latch (clear on read) 0b0: no command error 0b1: invalid command **UART_FERR** : UART frame error status latch (clear on read) 0b0: no frame error seen 0b1: frame error detected **UART_PERR** : UART parity error status latch (clear on read) 0b0: no parity error seen 0b1: parity error detected															

Table 6.2.6.3-3: Register **ERROR_STATUS_2** (0x26) Channel errors

	MSB															***LSB***
Content	-	-	-	-	-	-	-	-	-	-	-	-	CH_ERR_4	CH_ERR_3	CH_ERR_2	CH_ERR_1
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**CH_ERR_4** : Channel 4 error status (overall) 0b000: all bits of ERROR_STATUS_3 + ERROR_STATUS_4 are equal to '0' (= OR combination of these bits) 0b001: number of bits with '1' of ERROR_STATUS_3 + ERROR_STATUS_4 is higher or equal to 1 (= OR combination of these bits) **CH_ERR_3** : Channel 3 error status (overall) 0b000: all bits of ERROR_STATUS_7 + ERROR_STATUS_8 are equal to '0' (= OR combination of these bits) 0b001: number of bits with '1' of ERROR_STATUS_7 + ERROR_STATUS_8 is higher or equal to 1 (= OR combination of these bits) **CH_ERR_2** : Channel 2 error status (overall) 0b000: all bits of ERROR_STATUS_5 + ERROR_STATUS_6 are equal to '0' (= OR combination of these bits) 0b001: number of bits with '1' of ERROR_STATUS_5 + ERROR_STATUS_6 is higher or equal to 1 (= OR combination of these bits) **CH_ERR_1** : Channel 1 error status (overall) 0b000: all bits of ERROR_STATUS_3 + ERROR_STATUS_4 are equal to '0' (= OR combination of these bits) 0b001: number of bits with '1' of ERROR_STATUS_3 + ERROR_STATUS_4 is higher or equal to 1 (= OR combination of these bits)															

Table 6.2.6.3-4: Register **ERROR_STATUS_3** (0x27) Four error bits per frame (1-4) channel 1

	MSB															***LSB***
Content	MD_UNEX_FR_CH1_F4	MD_NO_FR_CH1_F4	MD_FERR_FR_CH1_F4	MD_PERR_FR_CH1_F4	MD_UNEX_FR_CH1_F3	MD_NO_FR_CH1_F3	MD_FERR_FR_CH1_F3	MD_PERR_FR_CH1_F3	MD_UNEX_FR_CH1_F2	MD_NO_FR_CH1_F2	MD_FERR_FR_CH1_F2	MD_PERR_FR_CH1_F2	MD_UNEX_FR_CH1_F1	MD_NO_FR_CH1_F1	MD_FERR_FR_CH1_F1	MD_PERR_FR_CH1_F1
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**MD_UNEX_FR_CH1_F4** : Manchester Decoder unexpected frame received 0b0: no unexpected frame received 0b1: unexpected frame received **MD_NO_FR_CH1_F4** : Manchester Decoder no frame received (clear on read) 0b0: frame received (in expected time slot) 0b1: no frame received (in expected time slot) **MD_FERR_FR_CH1_F4** : Manchester Decoder frame error status latch (clear on read) 0b0: no frame error seen 0b1: frame error detected **MD_PERR_FR_CH1_F4** : Manchester Decoder Parity/CRC error status latch (clear on read) 0b0: no parity/CRC error seen 0b1: parity/CRC error detected **MD_UNEX_FR_CH1_F3** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH1_F3** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH1_F3** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH1_F3** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH1_F2** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH1_F2** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH1_F2** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH1_F2** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH1_F1** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH1_F1** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH1_F1** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH1_F1** : see MD_PERR_FR_CH1_F4															

Table 6.2.6.3-5: Register **ERROR_STATUS_4** (0x28) Four error bits per frame (5-6) channel 1 and analog errors

	MSB															***LSB***
Content	-	-	SYNC_DATA_INV_CH1	REV_CUR_CH1	BUFF_ERR_CH1	OC_CH1	DIAG_CH1[1:0]		MD_UNEX_FR_CH1_F6	MD_NO_FR_CH1_F6	MD_FERR_FR_CH1_F6	MD_PERR_FR_CH1_F6	MD_UNEX_FR_CH1_F5	MD_NO_FR_CH1_F5	MD_FERR_FR_CH1_F5	MD_PERR_FR_CH1_F5
Reset value	0	0	0	0	0	0	00		0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C		R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**SYNC_DATA_ INV_CH1** : Reverse current status of channel 1 0b0: no SYNC pulse trigger during active Tx_LEN counter 0b1: SYNC pulse trigger during active Tx_LEN counter occurred **REV_CUR_CH1** : Reverse current status of channel 1 0b0: no reverse current detected 0b1: reverse current detected **BUFF_ERR_CH1** : Data buffer (96bit) configuration error 0b0: no configuration error 0b1: configuration error **OC_CH1** : Channel 1 over current status 0b0: no over current 0b1: over current **DIAG_CH1[1:0]** : Channel 1 diagnosis status code (clear on read) 0b00: no error 0b01 leakage to GND 0b10: leakage to VBAT (soft short) / open load **MD_UNEX_FR_CH1_F6** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH1_F6** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH1_F6** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH1_F6** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH1_F5** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH1_F5** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH1_F5** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH1_F5** : see MD_PERR_FR_CH1_F4															

Table 6.2.6.3-6: Register **ERROR_STATUS_5** (0x29) Four error bits per frame (1-4)channel 2

	MSB															***LSB***
Content	MD_UNEX_FR_CH2_F4	MD_NO_FR_CH2_F4	MD_FERR_FR_CH2_F4	MD_PERR_FR_CH2_F4	MD_UNEX_FR_CH2_F3	MD_NO_FR_CH2_F3	MD_FERR_FR_CH2_F3	MD_PERR_FR_CH2_F3	MD_UNEX_FR_CH2_F2	MD_NO_FR_CH2_F2	MD_FERR_FR_CH2_F2	MD_PERR_FR_CH2_F2	MD_UNEX_FR_CH2_F1	MD_NO_FR_CH2_F1	MD_FERR_FR_CH2_F1	MD_PERR_FR_CH2_F1
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**MD_UNEX_FR_CH2_F4** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH2_F4** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH2_F4** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH2_F4** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH2_F3** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH2_F3** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH2_F3** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH2_F3** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH2_F2** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH2_F2** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH2_F2** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH2_F2** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH2_F1** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH2_F1** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH2_F1** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH2_F1** : see MD_PERR_FR_CH1_F4															

Table 6.2.6.3-7: Register **ERROR_STATUS_6** (0x2A) Four error bits per frame (5-6)channel 2 and analog errors

	MSB															***LSB***
Content	-	-	SYNC_DATA_INV_CH2	REV_CUR_CH2	BUF-FER_ERR_CH2	OC_CH2	DIAG_CH2[1:0]		MD_UNEX_FR_CH2_F6	MD_NO_FR_CH2_F6	MD_FERR_FR_CH2_F6	MD_PERR_FR_CH2_F5	MD_UNEX_FR_CH2_F5	MD_NO_FR_CH2_F5	MD_FERR_FR_CH2_F5	MD_PERR_FR_CH2_F5
Reset value	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C		R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**SYNC_DATA_ INV_CH2** : Reverse current status of channel 2 0b0: no SYNC pulse trigger during active Tx_LEN counter 0b1: SYNC pulse trigger during active Tx_LEN counter occurred **REV_CUR_CH2** : Reverse current status of channel 2 0b0: no reverse current detected 0b1: reverse current detected **BUFFER_ERR_CH2** : Data buffer (96bit) configuration error 0b0: no configuration error 0b1: configuration error **OC_CH2** : Channel 2 over current status 0b0: no over current 0b1: over current **DIAG_CH2[1:0]** : Channel 1 diagnosis status code (clear on read) 0b00: no error 0b01 leakage to GND 0b10: leakage to VBAT (soft short) / open load **MD_UNEX_FR_CH2_F6** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH2_F6** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH2_F6** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH2_F5** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH2_F5** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH2_F5** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH2_F5** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH2_F5** : see MD_PERR_FR_CH1_F4															

Table 6.2.6.3-8: Register **ERROR_STATUS_7** (0x2B) Four error bits per frame (1-4)channel 3

	MSB															***LSB***
Content	MD_UNEX_FR_CH3_F4	MD_NO_FR_CH3_F4	MD_FERR_FR_CH3_F4	MD_PERR_FR_CH3_F4	MD_UNEX_FR_CH3_F3	MD_NO_FR_CH3_F3	MD_FERR_FR_CH3_F3	MD_PERR_FR_CH3_F3	MD_UNEX_FR_CH3_F2	MD_NO_FR_CH3_F2	MD_FERR_FR_CH3_F2	MD_PERR_FR_CH3_F2	MD_UNEX_FR_CH3_F1	MD_NO_FR_CH3_F1	MD_FERR_FR_CH3_F1	MD_PERR_FR_CH3_F1
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**MD_UNEX_FR_CH3_F4** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH3_F4** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH3_F4** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH3_F4** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH3_F3** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH3_F3** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH3_F3** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH3_F3** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH3_F2** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH3_F2** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH3_F2** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH3_F2** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH3_F1** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH3_F1** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH3_F1** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH3_F1** : see MD_PERR_FR_CH1_F4															

Table 6.2.6.3-9: Register **ERROR_STATUS_8** (0x2C) Four error bits per frame (5-6)channel 3 and analog errors

	MSB															***LSB***
Content	-	-	SYNC_DATA_INV_CH3	REV_CUR_CH3	BUFF_ERR_CH3	OC_CH3	DIAG_CH3[1:0]		MD_UNEX_FR_CH3_F6	MD_NO_FR_CH3_F6	MD_FERR_FR_CH3_F6	MD_PERR_FR_CH3_F6	MD_UNEX_FR_CH3_F5	MD_NO_FR_CH3_F5	MD_FERR_FR_CH3_F5	MD_PERR_FR_CH3_F5
Reset value	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C		R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**SYNC_DATA_ INV_CH3** : Reverse current status of channel 3 0b0: no SYNC pulse trigger during active Tx_LEN counter 0b1: SYNC pulse trigger during active Tx_LEN counter occurred **REV_CUR_CH3** : Reverse current status of channel 3 0b0: no reverse current detected 0b1: reverse current detected **BUFF_ERR_CH3** : Data buffer (96bit) configuration error 0b0: no configuration error 0b1: configuration error **OC_CH3** : Channel 3 over current status 0b0: no over current 0b1: over current **DIAG_CH3[1:0]** : Channel 3 diagnosis status code (clear on read) 0b00: no error 0b01 leakage to GND 0b10: leakage to VBAT (soft short) / open load **MD_UNEX_FR_CH3_F6** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH3_F6** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH3_F6** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH3_F6** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH3_F5** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH3_F5** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH3_F5** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH3_F5** : see MD_PERR_FR_CH1_F4															

Table 6.2.6.3-10: Register **ERROR_STATUS_9** (0x2D) Four error bits per frame (1-4)channel 4

	MSB															***LSB***
Content	MD_UNEX_FR_CH4_F4	MD_NO_FR_CH4_F4	MD_FERR_FR_CH4_F4	MD_PERR_FR_CH4_F4	MD_UNEX_FR_CH4_F3	MD_NO_FR_CH4_F3	MD_FERR_FR_CH4_F3	MD_PERR_FR_CH4_F3	MD_UNEX_FR_CH4_F2	MD_NO_FR_CH4_F2	MD_FERR_FR_CH4_F2	MD_PERR_FR_CH4_F2	MD_UNEX_FR_CH4_F1	MD_NO_FR_CH4_F1	MD_FERR_FR_CH4_F1	- MD_PERR_FR_CH4_F1
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access																
Bit Description	**MD_UNEX_FR_CH4_F4** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH4_F4** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH4_F4** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH4_F4** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH4_F3** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH4_F3** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH4_F3** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH4_F3** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH4_F2** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH4_F2** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH4_F2** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH4_F2** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH4_F1** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH4_F1** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH4_F1** : see MD_FERR_FR_CH1_F4 **-MD_PERR_FR_CH4_F1** : see MD_PERR_FR_CH1_F4															

Table 6.2.6.3-11: Register **ERROR_STATUS_10** (0x2E) Four error bits per frame (5-6)channel 4 and analog errors

	MSB															***LSB***
Content	-	-	SYNC_DATA_INV_CH4	REV_CUR_CH4	BUFF_ERR_CH4	OC_CH4	DIAG_CH4[1:0]		MD_UNEX_FR_CH4_F6	MD_NO_FR_CH4_F6	MD_FERR_FR_CH4_F6	MD_PERR_FR_CH4_F6	MD_UNEX_FR_CH4_F5	MD_NO_FR_CH4_F5	MD_FERR_FR_CH4_F5	MD_PERR_FR_CH4_F5
Reset value	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C		R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
Bit Description	**SYNC_DATA_ INV_CH4** : Reverse current status of channel 4 0b0: no SYNC pulse trigger during active Tx_LEN counter 0b1: SYNC pulse trigger during active Tx_LEN counter occurred **REV_CUR_CH4** : Reverse current status of channel 4 0b0: no reverse current detected 0b1: reverse current detected **BUFF_ERR_CH4** : Data buffer (96bit) configuration error 0b0: no configuration error 0b1: configuration error **OC_CH4** : Channel 4 over current status 0b0: no over current 0b1: over current **DIAG_CH4[1:0]** : Channel 4 diagnosis status code (clear on read) 0b00: no error 0b01 leakage to GND 0b10: leakage to VBAT (soft short) / open load **MD_UNEX_FR_CH4_F6** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH4_F6** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH4_F6** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH4_F6** : see MD_PERR_FR_CH1_F4 **MD_UNEX_FR_CH4_F5** : see MD_UNEX_FR_CH1_F4 **MD_NO_FR_CH4_F5** : see MD_NO_FR_CH1_F4 **MD_FERR_FR_CH4_F5** : see MD_FERR_FR_CH1_F4 **MD_PERR_FR_CH4_F5** : see MD_PERR_FR_CH1_F4															

6.2.6.4 Diagnosis Registers

There are 8 (read only, R) registers available for diagnosis purposes.
Following diagnosis informations are available:

- Voltages VDD,VBUS,VSYNC,VDD_INT
- Voltages SIFX

Table 6.2.6.4-1: Diagnosis register

Register Name	*Address*	*Description*
DIAGNOSIS_ADC_1_2	0x2F	ADC data:VDD_INT,VDD
DIAGNOSIS_ADC_3_4	0x30	ADC data:VSIF2,VSIF1
DIAGNOSIS:_ADC_5_6	0x31	ADC data:VSIF4,VSIF3
DIAGNOSIS_ADC_7_8	0x32	ADC data:VSYNC,VBUS
DIAGNOSIS_ADC_9_10	0x33	ADC data:VCP_GATE

Reading of unused bits will always return '0' and writing of unused bits don't care. Writing to read only or read on clear registers don't care. The SPI echo response to a write request is independently of register type (R/W, R, RC).

Table 6.2.6.4-2: Register **DIAGNOSIS_ADC_1_2** (0x2F) ADC data:VDD_INT,VDD

	MSB															***LSB***
Content	ADC_DATA_2[7:0]								ADC_DATA_1[7:0]							
Reset value	0								0							
Access	R								R							
Bit Description	**ADC_DATA_2[7:0]** : ADC data Voltage level VDD_INT **ADC_DATA_1[7:0]** : ADC data Voltage level VDD															

Table 6.2.6.4-3: Register **DIAGNOSIS_ADC_3_4** (0x30) ADC data:VSIF2,VSIF1

	MSB															***LSB***
Content	ADC_DATA_4[7:0]								ADC_DATA_3[7:0]							
Reset value	0								0							
Access	R								R							
Bit Description	**ADC_DATA_4[7:0]** : ADC data Voltage level VSIF2 **ADC_DATA_3[7:0]** : ADC data Voltage level VSIF1															

Table 6.2.6.4-4: Register **DIAGNOSIS:_ADC_5_6** (0x31) ADC data:VSIF4,VSIF3

	MSB															***LSB***
Content	ADC_DATA_6[7:0]								ADC_DATA_5[7:0]							
Reset value	0								0							
Access	R								R							
Bit Description	**ADC_DATA_6[7:0]** : ADC data Voltage level VSIF4 **ADC_DATA_5[7:0]** : ADC data Voltage level VSIF3															

Table 6.2.6.4-5: Register **DIAGNOSIS_ADC_7_8** (0x32) ADC data:VSYNC,VBUS

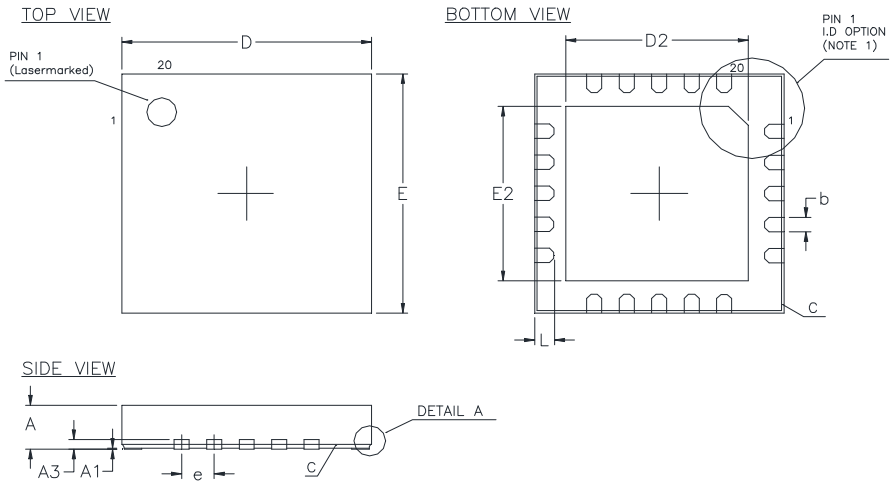
	MSB															***LSB***
Content	ADC_DATA_8[7:0]								ADC_DATA_7[7:0]							
Reset value	0								0							
Access	R								R							
Bit Description	**ADC_DATA_8[7:0]** : ADC data Voltage level VSYNC **ADC_DATA_7[7:0]** : ADC data Voltage level VBUS															

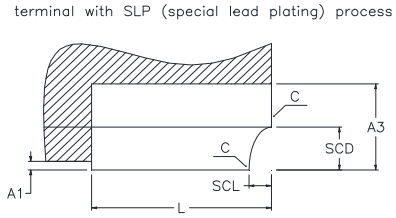
Table 6.2.6.4-6: Register **DIAGNOSIS_ADC_9_10** (0x33) ADC data:VCP_GATE

	MSB															***LSB***
Content	-	-	-	-	-	-	-	-	ADC_DATA_9[7:0]							
Reset value	0	0	0	0	0	0	0	0	0							
Access	R	R	R	R	R	R	R	R	R							
Bit Description	**ADC_DATA_9[7:0]** : ADC data Voltage level VCP_GATE															

7 Package Information

7.1 QFN20L5





Note: the letter "C" indicates the sawing line edge @ packages with SLP

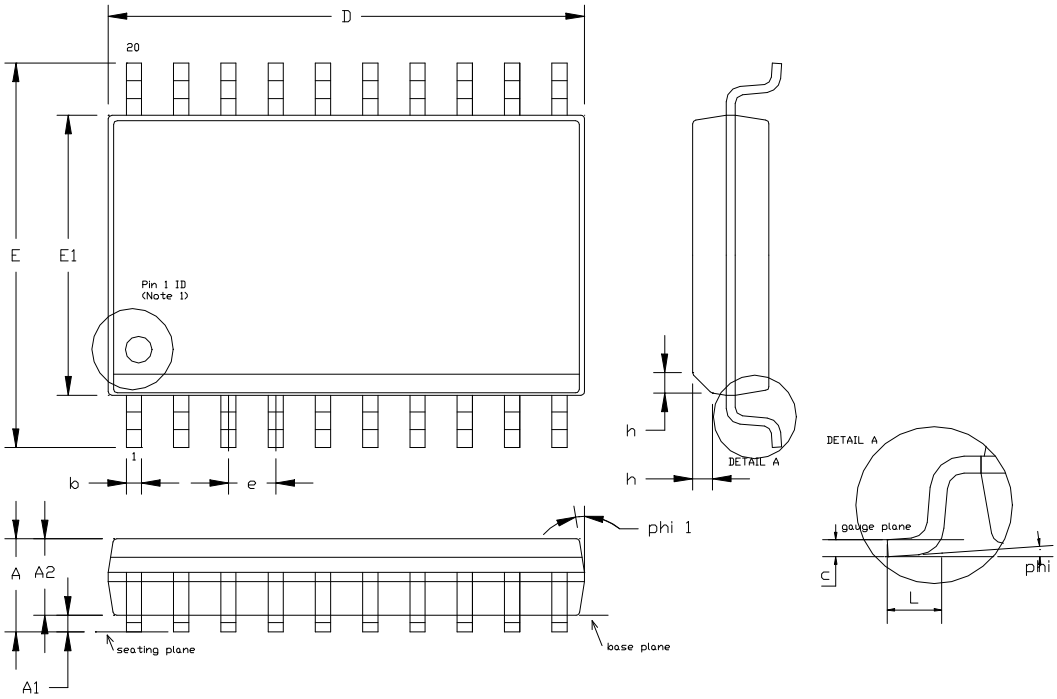
All devices are available in a Pb free, RoHs compliant QFN20L5 plastic package according to JEDEC MO-220 K, variant VHHC-2. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.

Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.25	0.30	0.35	0.010	0.012	0.014
Package length / width	D / E	--	5.00 BSC	--	--	0.197 BSC	--
Length / width of exposed pad	D2 / E2	3.50	3.65	3.80	0.138	0.144	0.150
Lead pitch	e	--	0.65 BSC	--	--	0.026 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Step cut depth (incl. plating layer)	SCD	0.075	0.100	0.125	0.003	0.004	0.005
Step cut length (incl. plating layer)	SCL	0.025	0.050	0.075	0.001	0.002	0.003
Number of terminal positions	N		20			20	

Note: the mm values are valid, the inch values contains rounding errors

7.2 SOIC20

All devices are available in a Pb free, RoHs compliant SOIC20 plastic package according to JEDEC MS-013-E, variant AC. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	--	--	2.65	--	--	0.104
Stand off	A1	0.10	--	0.30	0.004	--	0.012
Package body thickness	A2	2.05	--	--	0.081	--	--
Width of terminal leads, inclusive lead finish	b	0.31	--	0.51	0.012	--	0.020
Thickness of terminal leads, inclusive lead finish	c	0.20	--	0.33	0.008	--	0.013
Package length	D	12.80 BSC			0.504 BSC		
Package width	E	10.30 BSC			0.406 BSC		
Package body width	E1	7.50 BSC			0.295 BSC		
Lead pitch	e	1.27 BSC			0.050 BSC		
Length of terminal for soldering to substrate	L	0.4	--	1.27	0.016	--	0.050
body chamfer (45°)	h	0.25	--	0.75	0.010	--	0.030
Angle of lead mounting area	phi [°]	0	--	8	0	--	8
mold release angle	phi1 [°]	5	--	15	5	--	15
Number of terminal positions	N	20			20		

Note: the mm values are valid, the inch values contains rounding errors

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8 Index

Table of Content

Features....1
Applications....1
General Description....1
Ordering Information....1
Typical Application Circuit....1
Functional Diagram....2
1 Package Pinout QFN20L5,SO20....3
1.1 Pin Description QFN20L5....4
1.2 Pin Description SO20....5
2 Application Description....6
2.1 Application Circuits....6
2.1.1 Application Circuits....6
3 Functional Safety....9
3.1 Functional Safety Requirements....9
3.2 FMEDA....9
3.2.1 Safety Measures mandatory to reach ASIL Level C....9
4 Operating Conditions....10
4.1 Absolute Maximum Ratings....10
4.2 Recommended Operating Conditions....11
5 Detailed Electrical Specification....13
5.1 ANALOG PART....13
5.1.1 SUPPLY....13
5.1.1.1 LDO Control Block....13
5.1.1.1.1 Electrical Parameter of LDO....13
5.1.1.1.2 Electrical Parameter Control Voltage....15
5.1.1.2 Charge Pump for Sync Voltage....15
5.1.2 POR AND POWER-UP SEQUENCE....15
5.1.3 PSI5 INTERFACE....16
5.1.3.1 Interface Driver....16
5.1.3.2 Over Current Detection and Limitation....17
5.1.3.3 Reverse Current Detection and Limitation....17
5.1.3.3.1 Reverse Current Flow from SIFx to VBUS....17
5.1.3.3.2 Reverse Current Flow from SIFx to CSYNC....18
5.1.3.4 Data Comparator....18
5.1.3.5 Sync Pulse Generation....18
5.1.3.5.1 Sync Pulse Generation DC-Parameter....18
5.1.3.5.2 Sync Pulse Generation AC Parameter....19
5.1.3.6 Sync Pulse Generation by Pin TRIG....19
5.1.4 CLOCK GENERATION....20
5.1.5 DIAGNOSIS....21
5.1.5.1 ADC Voltage Measurements....21
5.1.5.2 Over Temperature Monitoring (OT)....21
5.1.5.3 VBUS Over Voltage Monitoring....22
5.2 DIGITAL PART....23
5.2.1 SPI....23
5.2.1.1 DC Electrical Parameter Table of SPI IOs....23
5.2.1.2 AC Electrical Parameter Table of SPI I/Os....23
6 Functional Description....24
6.1 ANALOG PART....24
6.1.1 SUPPLY....24
6.1.1.1 LDO Control Block....24
6.1.1.2 Charge Pump for Sync Voltage....24

6.1.2 POR AND POWER-UP SEQUENCE....25
6.1.3 PSI5 INTERFACE....25
6.1.3.1 Interface Driver....25
6.1.3.2 Over Current Detection and Limitation....25
6.1.3.3 Reverse Current Detection and Limitation....25
6.1.3.3.1 Reverse Current Flow from SIFx to VBUS....25
6.1.3.3.2 Reverse Current Flow from SIFx to CSYNC....26
6.1.3.4 Quiescent Current Threshold Tracking....26
6.1.3.5 Data Comparator....26
6.1.3.6 Sync Pulse Generation....27
6.1.3.7 Sync Pulse Generation by Pin TRIG....28
6.1.3.8 Sync Pulse Generation by UART/SPI Command....29
6.1.4 CLOCK GENERATION....29
6.1.5 DIAGNOSIS....30
6.1.5.1 ADC Voltage Measurements....30
6.1.5.2 Over Temperature Monitoring (OT)....30
6.1.5.3 VBUS Over Voltage Monitoring....31
6.1.5.4 Leakage to GND, Leakage to VBAT and Open Load....31
6.1.5.5 GND Loss Detection....31
6.1.5.6 Transfer of Error- and Diagnosis Information to μController....31
6.1.5.6.1 Error Information....31
6.2 DIGITAL PART....35
6.2.1 COMMUNICATION INTERFACE TO MICRO CONTROLLER....35
6.2.2 MANCHESTER DECODER....35
6.2.2.1 Manchester Data Handling and Buffer Architecture....35
6.2.2.1.1 UART DATA BUFFER....36
6.2.2.1.2 SPI DATA BUFFER....36
6.2.2.2 Manchester Bit Encoding....38
6.2.2.2.1 Definition of data edge / compensation edge....38
6.2.2.2.2 Interpretation with Manchester Decoder....38
6.2.2.2.3 Definition of Duty Cycle....38
6.2.2.2.4 Decoder Error Flags....39
6.2.3 SPI....39
6.2.3.1 Error Handling....41
6.2.3.2 Overview of Communication Frames....43
6.2.3.3 Overview of SPI commands....44
6.2.3.4 No Operation Command....44
6.2.3.5 Write Configuration Register Command....44
6.2.3.6 Software Reset Command....45
6.2.3.7 Read Configuration Register Command....45
6.2.3.8 SYNC Pulse Command....45
6.2.3.9 Read Sensor Data....46
6.2.3.9.1 Read of 16bit (11bit sensor data)....48
6.2.3.9.2 Read of 24bit (19bit sensor data)....49
6.2.3.9.3 Read of 32bit (27bit sensor data)....49
6.2.3.9.4 Read of 48bit (43bit sensor data)....49
6.2.4 UART....50
6.2.4.1 Error Handling 50
6.2.4.2 Packet Frame Definition....52
6.2.4.3 UART Frame Definition....52
6.2.4.4 Overview of Communication Frames....53
6.2.4.5 Overview of UART Commands....53
6.2.4.6 Write Register Command....54
6.2.4.7 Read Register Command....54
6.2.4.8 Short SYNC Pulse Command....55

6.2.4.9 Long SYNC Pulse Command....55
6.2.4.10 No SYNC Pulse Command....55
6.2.4.11 Software Reset Command....56
6.2.4.12 Response to Read Register Command....56
6.2.4.13 Transfer PSI5 Data....57
6.2.5 XCRC[5:0] Calculation....58
6.2.6 CONFIGURATION....59
6.2.6.1 ASIC Configuration....59
6.2.6.1.1 Asynchronous mode....63
6.2.6.2 Timeslot Configuration....63
6.2.6.2.1 Timeslot Length....73
6.2.6.3 Error Registers....75
6.2.6.4 Diagnosis Registers....82
7 Package Information....84
7.1 QFN20L5....84
7.2 SOIC20....85
8 Index....87

Illustration Index

Figure 2.1.1-1: Application Circuit with LDO....6
Figure 2.1.1-2: Application Circuit with VBUS Supplied from ECU....7
Figure 6.1.3.5-1: Current Modulation....25
Figure 6.1.3.6-1: Sync Pulse Timing Diagram....26
Figure 6.1.3.7-1: Long SYNC Pulse Trigger via Pin TRIG....27
Figure 6.1.3.7-2: Short SYNC Pulse Trigger via Pin TRIG....27
Figure 6.1.3.8-1: Short SYNC Ptrigger via UART....28
Figure 6.1.3.8-2: Short SYNC Pulse Trigger via SPI....28
Figure 6.2.2.1-1: Buffer Architecture Overview....34
Figure 6.2.2.1.1-1: UART Data Buffer....35
Figure 6.2.2.1.2-1: SPI Data Buffer....36
Figure 6.2.2.1.2-2: SPI Data Buffer incl. 4 Frames....36
Figure 6.2.2.2.3-1: Example MCD Duty Cycle....37
Figure 6.2.2.2.4-1: MD_FERR_CHx_F1....38
Figure 6.2.2.2.4-2: Set Of Error Flags (2errors; data=0x3FF)....38
Figure 6.2.3-1: Data Flow Graphic....39
Figure 6.2.3.1-1: SPI Error Handling Example 1....40
Figure 6.2.3.1-2: SPI Error Handling Example 2....40
Figure 6.2.3.1-3: SPI Error Handling Example 3....40
Figure 6.2.3.1-4: SPI Error Handling Example 4....40
Figure 6.2.3.4-1: SPI NOP Command....43
Figure 6.2.3.5-1: SPI Write Register Command....44
Figure 6.2.3.6-1: SPI Software Reset Command....44
Figure 6.2.3.7-1: SPI Read Register Command....44
Figure 6.2.3.8-1: SPI SYNC Pulse Command....45
Figure 6.2.3.9-1: Valid read sensor data window 1....46
Figure 6.2.3.9-2: Valid read sensor data window 2....46
Figure 6.2.3.9.1-1: SPI Read Sensor Data 16bit....47
Figure 6.2.3.9.1-2: SPI Read Sensor Data 16bit-request at SDI_RXD -1st SPI frame-....47
Figure 6.2.3.9.1-3: Response to SPI Read Sensor Data 16bit at SDO_TXD -2nd SPI frame-....47
Figure 6.2.3.9.2-1: Read Sensor Data 24bit command....48
Figure 6.2.3.9.3-1: Read Sensor Data 32bit command....48
Figure 6.2.3.9.4-1: Read Sensor Data 48bit command....48
Figure 6.2.4.1-1: UART Error Handling Example 1....49
Figure 6.2.4.1-2: UART Error Handling Example 2....49
Figure 6.2.4.1-3: Syncpulse staggering....50

Figure 6.2.4.3-1: UART Data Transmission....52
Figure 6.2.4.6-1: Write Register Command Packet Frame....53
Figure 6.2.4.7-1: Read Register Command Packet Frame....53
Figure 6.2.4.8-1: Short SYNC Command Packet Frame....54
Figure 6.2.4.9-1: Long SYNC Command Packet Frame....54
Figure 6.2.4.10-1: No SYNC Pulse Command Packet Frame....55
Figure 6.2.4.11-1: Software Reset Command Frame....55
Figure 6.2.4.12-1: Response to Read Register Command Packet Frame....56
Figure 6.2.4.13-1: Example: Upload PSI5 Data Minimum Packet Frame....56
Figure 6.2.4.13-2: Example: Upload PSI5 Data Maximum Packet Frame....56
Figure 6.2.5-1: XCRC-calculation for SPI frames....57
Figure 6.2.5-2: XCRC: Example Transfer PSI5 Data....57
Figure 6.2.5-3: XCRC: Example Response to Read Command....58
Figure 6.2.5-4: XCRC Example Read Sensor Data 24bit....58
Figure 6.2.6.2.1-1: Example1: TxLEN Configuration....72
Figure 6.2.6.2.1-2: Example2: TxLEN Configuration....72
Figure 6.2.6.2.1-3: Example2: TxLEN Configuration: Unexptected Sync Pulse....73