Semicustom Products

# UT90nHBD Hardened-by-Design (HBD) Standard Cell

Preliminary Data Sheet
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www.aeroflex.com/RadHardASIC

## FEATURES

❑ Up to 50,000,000 2-input NAND equivalent gates with a 1.0V Core using standard cell architecture

❑ Toggle rates up to 5.0 GHz

❑ Advanced 90nm silicon gate CMOS processed in a commercial fab

❑ Operating voltages: 2.5V and 1.8V I/O; 1.0V core

❑ Radiation hardened from 100 krads(Si) to 1 Mrads(Si) total dose available

❑ Comprehensive set of core standard cells with multiple $V_t$ options for optimizing speed and power

❑ Design support for Mentor Graphics®, Synopsys®, Verilog and VHDL design languages on Sun$^{(TM)}$ and Linux workstations

❑ Power dissipation of 7nW/MHz/gate at $V_{DDCORE}$ 1.0V and 20% duty cycle

❑ External chip capacitor attachment option available to space quality levels (for improved SSO response)

❑ UT90nHBD ASIC technology is available under Aeroflex's Accreditation of Trust Category 1A from design through device qualification and delivery.

❑ QML Class Y non-hermetic Flip Chip ceramic packaging

❑ Standard Microelectronics Drawing - 5962-14B01

## PRODUCT DESCRIPTION

The high-performance UT90nHBD Hardened-by-Design ASIC standard cell family features densities up to, and beyond 50,000,000 equivalent NAND2 gates.

The deep submicron ASIC family uses a highly efficient standard cell architecture for the internal cell instantiation. Combined with state-of-the-art place and route tools, the area utilization and signal interconnect of transistors is maximized using eight levels of copper metal interconnect.

### Extensive Cell Library

The UT90nHBD standard cell family is supported by an extensive cell library with over 900 elements. User selectable options for cell configurations include scan for all register elements, output drive strengths (1x to 30x) and transistor threshold voltages ($LV_t$, $RV_t$). Refer to Aeroflex's UT90nHBD Design Manual for complete cell listing and details.

### Aeroflex Gaisler IP

We offer Aeroflex Gaisler Processor IP. A complete library of Aeroflex Gaisler IP can be reviewed at www.Aeroflex.com/Gaisler.

### I/O Buffers

The UT90nHBD library offers extensive I/O cell options. The I/O library contains 36 different general purpose CMOS functional I/O pads. A rich set of LVDS inputs and outputs support data rates up to 1.2Gbps with optional on-chip terminations. The LVDS family of buffers include several drive strengths for point-to-point, multi-point, and Bus-LVDS applications. The LVDS buffers have programmable slew rate control. 2.5V and 1.8V LVDS cells are available to optimize for speed and power in the system design.

Other I/O buffer features and options include:

- Basic Input, Output, and Bi-directional

- 9mA and 18mA drive strength

- Slew rate control

- Schmitt Trigger

- Tri-State

- Open Drain

- SSTL 1.8V/2.5V

### Cold Sparing

The UT90nHBDI/O library includes a set of cold sparing I/O cells that enables the user to design for system redundancy. These cold sparing cells present a high input impedance to the system interface when powered off assuring that the cold spared redundant device does not draw power.

### Macro Cells

The UT90nHBD library includes a macro cell library that enables system-on-a-chip (SOC) design. The following macros are currently available:

- Clock Generator PLL

- 3.125 Gbps SerDes Tx/Rx lane

- 1, 2 and 4-lane 10 Gbps SerDes Macro

- Embedded die temperature resistor

### Embedded SRAM

Aeroflex offers a comprehensive set of compiled embedded memories to meet your ASIC architectural needs. Features include:

- Single and Dual Port SRAM compiler

- Single and Two Port Register File compiler

- Operating frequencies of 400MHz and higher

- Optional EDAC RTL generation: 1 or 2 bit detect, 1 bit correct

- Configurable word write mask

- Optional integrated BIST Mux/Collar

- All standard EDA views supported

### Clock Driver Distribution

Aeroflex design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices. The UT90nHBD PLL's all include optional external clock feedback to support clock de-skew applications.

### Speed and Performance

Aeroflex specializes in high-performance circuits designed to operate in harsh military and radiation environments. The UT90nHBD library offers cells in both regular Vt and low Vt allowing the user to trade speed for power. The cells can be mixed on the same die providing local solutions for critical paths without sacrificing full chip power consumption.

### Power Dissipation and Power Estimation Tools

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. Radiation-tolerant processes exhibit power dissipation that is typical of CMOS processes. A power estimation spreadsheet that is useful for architecture trade-off analysis is available in the customer toolkit. For a more rigorous power estimating methodology, the synthesis library in the customer design toolkit supports pre-layout and post-layout power analysis. For additional information, refer to the Aeroflex UT90nHBD Design Manual or consult with an Aeroflex Applications Engineer.

### Packaging

Both Flip Chip and Wire Bond packaging is available for the UT90nHBD ASICs. Standard pin counts range from 624 to 1752 in both ceramic CGAand Column attach options. Heat sink and decoupling capacitors are available in the Class Y package.

# *Aeroflex Colorado Springs - Datasheet Definition*

## Advanced Datasheet - Product In Development

## Preliminary Datasheet - Shipping Prototype

## Datasheet - Shipping QML & Reduced Hi-Rel

**This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Government is required prior to the export of this product from the United States.**

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