Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics

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Summary

The Xilinx® Zynq® UltraScale+™ MPSoCs are available in -3, -2, -1 speed grades, with -3E devices having the highest performance. The -2LE and -1LI devices can operate at a V_{CCINT} voltage at 0.85V or 0.72V and are screened for lower maximum static power. When operated at V_{CCINT} = 0.85V, using -2LE and -1LI devices, the speed specification for the L devices is the same as the -2I or -1I speed grades. When operated at V_{CCINT} = 0.72V, the -2LE and -1LI performance and static and dynamic power is reduced.

DC and AC characteristics are specified in extended (E) and industrial (I) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Zynq UltraScale+ MPSoCs, is available on the Xilinx website at www.xilinx.com/documentation.

DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description	Min	Max	Units
Processor System (PS)				
$V_{CC\_PSINTFP}$	PS primary logic full-power domain supply voltage.	–0.500	1.000	V
$V_{CC\_PSINTLP}$	PS primary logic low-power domain supply voltage.	–0.500	1.000	V
V_{CC_PSAUX}	PS auxiliary supply voltage.	–0.500	1.980	V
$V_{CC\_PSINTFP\_DDR}$	PS DDR controller and PHY supply voltage.	–0.500	1.000	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC.	–0.500	1.980	V
V_{CC_PSPLL}	PS PLL supply voltage.	–0.500	1.320	V
$V_{PS\_MGTRAVCC}$	PS-GTR supply voltage.	–0.500	1.000	V
$V_{PS\_MGTRAVTT}$	PS-GTR termination voltage.	–0.500	1.980	V
$V_{PS\_MGTREFCLK}$	PS-GTR reference clock input voltage.	–0.500	1.100	V
V_{PS_MGTRIN}	PS-GTR receiver input voltage.			V
V_{CCO_PSDDR}	PS DDR I/O supply voltage.	–0.500	1.650	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	–0.500	1.980	V

Table 1: **Absolute Maximum Ratings[1] *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{CCO_PSIO}	PS I/O supply.	–0.500	3.630	V
V_{PSIN}	PS I/O input voltage.	–0.500	V_{CCOPIO} + 0.550	V
	PS DDR I/O input voltage.	–0.500	V_{CCODDR} + 0.550	V
V_{CC_PSBATT}	PS battery-backed RAM and real time clock supply voltage.	–0.500	2.000	V
Programmable Logic (PL)				
V_{CCINT}	Internal supply voltage.	–0.500	1.000	V
V_{CCINT_IO}[2]	Internal supply voltage for the I/O banks.	–0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage.	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories.	–0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks.	–0.500		V
	Output drivers supply voltage for HP I/O banks.	–0.500		V
V_{CCAUX_IO}[3]	Auxiliary supply voltage for the I/O banks.	–0.500	2.000	V
V_{REF}	Input reference voltage.			V
V_{IN}[4][6][7]	I/O input voltage for HD I/O banks[5].	–0.500		V
	I/O input voltage for HP I/O banks.	–0.500	V_{CCO} + 0.550	V
I_{DC}	Available output current at the pad.			mA
I_{RMS}	Available RMS output current at the pad.			mA
GTH or GTY Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTH or GTY transmitter and receiver circuits.	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTH or GTY transceivers.	–0.500	1.900	V
$V_{MGTREFCLK}$	GTH or GTY transceiver reference clock absolute input voltage.	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating.	–		mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	–	0[8]	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND.	–	0[8]	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable.	–	0[8]	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	–		mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	–		mA
Video Codec Unit				
V_{CCINT_VCU}	Internal supply voltage for the video codec unit.	–0.500	1.000	V

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
PL System Monitor				
V_{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V_{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient).	–65	150	°C
T_{SOL}	Maximum soldering temperature(9).	–	260	°C
T_j	Maximum junction temperature(9).	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
6. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
7. The maximum limit applied to DC signals. For maximum undershoot and overshoot AC specifications, see Table 6 and Table 7.
8. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578)
9. For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* (UG1075).

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
Processor System					
$V_{CC\_PSINTFP}$(3)	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (0.72V only) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (0.72V only) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
V_{CC_PSAUX}	PS auxiliary supply voltage.	1.710	1.800	1.890	V
$V_{CC\_PSINTFP\_DDR}$(3)	PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (0.72V only) devices: PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS DDR controller and PHY supply voltage.	0.873	0.900	0.927	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC.	1.710	1.800	1.890	V
V_{CC_PSPLL}	PS PLL supply voltage.	1.164	1.200	1.236	V
$V_{PS\_MGTRAVCC}$	PS-GTR supply voltage.	0.825	0.850	0.875	V
	For -1LI and -2LE (0.72V only) devices: PS-GTR supply voltage.	0.825	0.850	0.875	V
	For -3E devices: PS-GTR supply voltage.	0.873	0.900	0.927	V
$V_{PS\_MGTRAVTT}$	PS-GTR termination voltage.	1.746	1.800	1.854	V
V_{CCO_PSDDR}(4)	PS DDR I/O supply voltage.	1.045	–	1.575	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	1.710	1.800	1.890	V
V_{CCO_PSIO}(5)	PS I/O supply.	1.710	–	3.465	V
V_{PSIN}	PS I/O input voltage.	–0.200	–	V_{CCODDR} + 0.200 V_{CCOPIO} + 0.200	V
V_{CC_PSBATT}(6)	PS battery-backed RAM and battery-backed real-time clock supply voltage.	1.200	–	1.500	V
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 3.3V.	20	–	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 2.5V.	20	–	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 1.8V.	15	–	65	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	20	–	80	µA
	Pad pull-down (when selected) at V_{IN} = 2.5V.	20	–	80	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	15	–	65	µA

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (0.72V only) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}(7)	PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE devices (0.85V only): PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: PL internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V_{CCO}(8)	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(9)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(10)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(11)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–		mA
GTH or GTY Transceiver					
$V_{MGTAVCC}$(12)	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(12)	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.20	1.236	V
$V_{MGTVCCAUX}$(12)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
$V_{MGTAVTTRCAL}$(12)	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.20	1.236	V

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
PL System Monitor					
V_{CCADC}	PL System Monitor supply relative to GNDADC.	1.746	1.800	1.854	V
V_{REFP}	PL System Monitor externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T_j	Junction temperature operating range for extended (E) temperature devices.(13)	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. $V_{CC\_PSINTFP\_DDR}$ must be tied to $V_{CC\_PSINTFP}$.
4. Includes V_{CCO_PSDDR} of 1.1V, 1.2V, 1.35V, 1.5V at ±5%.
5. Applies to all PS I/O supply banks.
6. If the battery-backed RAM or RTC is not used, connect V_{CC_PSBATT} to GND.
7. V_{CCINT_IO} must be connected to V_{CCBRAM}.
8. Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
9. V_{CCAUX_IO} must be connected to V_{CCAUX}.
10. The lower absolute voltage specification always applies.
11. A total of 200 mA per 52-pin bank should not be exceeded.
12. Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
13. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.

Table 3: **PS MIO Pull-up and Pull-down Current**

Symbol	Description	Min	Max	Units
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 3.3V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 2.5V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 1.8V.	15	65	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 2.5V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	15	65	µA

Table 4 describes the speed grades per device and the V_{CCINT} operating supply voltages for the full-power, low-power, and DDR domains. For more information on selecting devices and speed grades, see the *UltraScale Architecture and Product Overview* (DS890).

Table 4: **Available Speed Grades and Operating Voltages per Device**

Device	Speed Grade	V_{CCINT}	$V_{CC\_PSINTLP}$	$V_{CC\_PSINTFP}$	$V_{CC\_PSINTFP\_DDR}$	Units
XCZU2EG, XCZU3EG, XCZU4EV, XCZU5EV, XCZU6EG, XCZU7EV, XCZU9EG, XCZU11EG, XCZU15EG, XCZU17EG, XCZU19EG	-3E	0.90	0.90	0.90	0.90	V
	-2I	0.85	0.85	0.85	0.85	V
	-2LE	0.85	0.85	0.85	0.85	V
	-1E	0.85	0.85	0.85	0.85	V
	-1I	0.85	0.85	0.85	0.85	V
	-1LI	0.85	0.85	0.85	0.85	V
	-2LE	0.72	0.85	0.85	0.85	V
	-1LI	0.72	0.85	0.85	0.85	V

Table 5: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).		–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).		–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–		µA
I_L	Input or output leakage current per pin (sample-tested).(2)	–	–		µA
C_{IN}(3)	Die input capacitance at the pad (HP I/O).	–	–		pF
	Die input capacitance at the pad (HD I/O).	–	–		pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V.		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V.		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V.		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V.		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V.		–		µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.		–		µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.		–		µA
$I_{CCADCON}$	Analog supply current, analog circuits in power-up state.	–	–		mA
$I_{CCADCOFF}$	Analog supply current, analog circuits in power-down state.		–	–	mA
I_{BATT}(4)(5)	Battery supply current.	150	–	250	nA
Calibrated programmable on-die termination (DCI) in HP I/O banks(7) (measured per JEDEC specification)					
R(8)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40.(6)		40		Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.(6)		48		Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60.(6)		60		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.(6)		40		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.(6)		48		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.(6)		60		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.(6)		120		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.(6)		240		Ω

Table 5: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
$R^{(8)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.		40		Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.		48		Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.		60		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.		40		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.		48		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.		60		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.		120		Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.		240		Ω
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
$R^{(8)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.		48		Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–	100	–	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–		–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{BATT} is measured when the battery-backed RAM (BBRAM) is enabled and the real-time clock is disabled.
6. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
7. VRP resistor tolerance is (240Ω ±1%)
8. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks(1)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30			
V_{CCO} + 0.35			
V_{CCO} + 0.40			
V_{CCO} + 0.45			
V_{CCO} + 0.50			
V_{CCO} + 0.55			
V_{CCO} + 0.60			
V_{CCO} + 0.65			
V_{CCO} + 0.70			
V_{CCO} + 0.75			
V_{CCO} + 0.80			
V_{CCO} + 0.85			
V_{CCO} + 0.90			
V_{CCO} + 0.95			

Notes:
1. A total of 200 mA per bank should not be exceeded.

Table 7: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.05			
V_{CCO} + 0.10			
V_{CCO} + 0.15			
V_{CCO} + 0.20			
V_{CCO} + 0.25			
V_{CCO} + 0.30			
V_{CCO} + 0.35			
V_{CCO} + 0.40			
V_{CCO} + 0.45			
V_{CCO} + 0.50			
V_{CCO} + 0.55			
V_{CCO} + 0.60			
V_{CCO} + 0.65			
V_{CCO} + 0.70			
V_{CCO} + 0.75			
V_{CCO} + 0.80			
V_{CCO} + 0.85			

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 8: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XCZU2EG						mA
		XCZU3EG						mA
		XCZU4EV						mA
		XCZU5EV						mA
		XCZU6EG						mA
		XCZU7EV						mA
		XCZU9EG	1690	1607	1607	1409	1409	mA
		XCZU11EG						mA
		XCZU15EG						mA
		XCZU17EG						mA
		XCZU19EG						mA
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current.	XCZU2EG						mA
		XCZU3EG						mA
		XCZU4EV						mA
		XCZU5EV						mA
		XCZU6EG						mA
		XCZU7EV						mA
		XCZU9EG	61	59	59	59	59	mA
		XCZU11EG						mA
		XCZU15EG						mA
		XCZU17EG						mA
		XCZU19EG						mA
I_{CCOQ}	Quiescent V_{CCO} supply current.	XCZU2EG						mA
		XCZU3EG						mA
		XCZU4EV						mA
		XCZU5EV						mA
		XCZU6EG						mA
		XCZU7EV						mA
		XCZU9EG	1	1	1	1	1	mA
		XCZU11EG						mA
		XCZU15EG						mA
		XCZU17EG						mA
		XCZU19EG						mA

Table 8: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XCZU2EG						mA
		XCZU3EG						mA
		XCZU4EV						mA
		XCZU5EV						mA
		XCZU6EG						mA
		XCZU7EV						mA
		XCZU9EG	273	273	273	273	273	mA
		XCZU11EG						mA
		XCZU15EG						mA
		XCZU17EG						mA
		XCZU19EG						mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current.	XCZU2EG						mA
		XCZU3EG						mA
		XCZU4EV						mA
		XCZU5EV						mA
		XCZU6EG						mA
		XCZU7EV						mA
		XCZU9EG	33	33	33	33	33	mA
		XCZU11EG						mA
		XCZU15EG						mA
		XCZU17EG						mA
		XCZU19EG						mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XCZU2EG						mA
		XCZU3EG						mA
		XCZU4EV						mA
		XCZU5EV						mA
		XCZU6EG						mA
		XCZU7EV						mA
		XCZU9EG	48	45	45	45	45	mA
		XCZU11EG						mA
		XCZU15EG						mA
		XCZU17EG						mA
		XCZU19EG						mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power system must operate before the full-power system can function. The low-power and full-power domains can be powered simultaneously. To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTLP}$
2. V_{CC_PSAUX}, V_{CC_PSADC}, and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTFP}$ and $V_{CC\_PSINTFP\_DDR}$ driven from the same supply source.
2. $V_{PS\_MGTRAVCC}$ and $V_{CC\_PSDDR\_PLL}$ in any order or simultaneously.
3. $V_{PS\_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 9 shows the minimum current, in addition to I_{CCQ}, that are required by Zynq UltraScale+ MPSoC for proper power-on and configuration. If the current minimums shown in Table 8 and Table 9 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 9: **Power-on Current by Device**

Device	$I_{CCINTMIN}$	$I_{CCINT\_IOMIN} + I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN} + I_{CCAUX\_IOMIN}$	Units
XCZU2EG	I_{CCINTQ} + 464	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 155	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 111	mA
XCZU3EG	I_{CCINTQ} + 464	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 155	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 111	mA
XCZU4EV	I_{CCINTQ} + 770	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 257	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 386	mA
XCZU5EV	I_{CCINTQ} + 770	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 257	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 386	mA
XCZU6EG	I_{CCINTQ} + 1554	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 505	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 362	mA
XCZU7EV	I_{CCINTQ} + 1554	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 505	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 362	mA
XCZU9EG	I_{CCINTQ} + 1800	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 600	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 650	mA
XCZU11EG	I_{CCINTQ} + 1961	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 654	I_{CCOQ} + 55	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 709	mA
XCZU15EG	I_{CCINTQ} + 2242	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 748	I_{CCOQ} + 63	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 810	mA
XCZU17EG	I_{CCINTQ} + 3433	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1145	I_{CCOQ} + 96	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1240	mA
XCZU19EG	I_{CCINTQ} + 3433	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1145	I_{CCOQ} + 96	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1240	mA

Table 10 shows the power supply ramp time.

Table 10: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}.	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}.	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}.	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}.	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}.	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 11: **PS MIO and CONFIG DC Input and Output Levels(1)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	–0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	–12
LVCMOS25	–0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	–12
LVCMOS18	–0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} – 0.45	12	–12

Notes:
1. Tested according to relevant specifications.

Table 12: **PS DDR DC Input and Output Levels(1)**

DDR Standard	V_{IL}		V_{IH}		V_{OL}(2)	V_{OH}(2)	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} – 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	–0.1
LPDDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} – 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	–10
DDR3	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	–8
LPDDR3	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8
DDR3L	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8

Notes:
1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

PL I/O Levels

Table 13: **SelectIO DC Input and Output Levels For HD I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL135_II	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL15_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.0	–8.0
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 15, Table 19, Table 20, and Table 21.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 14: **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 15, Table 19, Table 20, and Table 21.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 15: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 16: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)(1)			V_{ID}(V)(2)			V_{ILHS}(3)	V_{IHHS}(3)	V_{OCM}(V)(4)			V_{OD}(V)(5)		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS(8)	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS(9)	0.070		0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 22.
7. LVDS is specified in Table 23.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 17: **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

I/O Standard	V_{ICM} (V)(1)			V_{ID} (V)(2)		V_{OL} (V)(3)	V_{OH} (V)(4)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 18: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks(1)**

I/O Standard	V_{ICM} (V)(2)			V_{ID} (V)(3)		V_{OL} (V)(4)	V_{OH} (V)(5)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	0.400	V_{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	$V_{CCO}/2$	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSTL_I_18	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	0.400	V_{CCO} – 0.400	6.2	–6.2
DIFF_HSUL_12	($V_{CCO}/2$) – 0.120	$V_{CCO}/2$	($V_{CCO}/2$) + 0.120	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	8.0	–8.0
DIFF_SSTL135	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	9.0	–9.0
DIFF_SSTL15	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.175	($V_{CCO}/2$) + 0.175	10.0	–10.0
DIFF_SSTL18_I	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.470	($V_{CCO}/2$) + 0.470	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 19, Table 20, and Table 21.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 19: **DC Input Levels for Differential POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 20: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 21)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 21)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: **Table 20 Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V_{CCO}	V

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 22: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{CCO}(1)	Supply voltage.	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	100	350	600(2)	mV
V_{ICM}	Input common-mode voltage.	0.300	1.200	1.500	V

Notes:

1. HD I/O banks only support LVDS_25 inputs. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 23: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}(1)	Supply voltage.		1.710	1.800	1.890	V
V_{ODIFF}(2)	Differential output voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}(2)	Output common-mode voltage.	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}(3)	Differential input voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600(3)	mV
V_{ICM_DC}(4)	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
V_{ICM_AC}(5)	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 24.

Table 24: **Speed Specification Version By Device**

2016.1	Device
1.04	XCZU2EG, XCZU3EG, XCZU6EG, XCZU9EG, XCZU15EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 24 correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See Table 4 for operating voltages listed by speed grade and device.

Table 25: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU2EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU3EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EV	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5EV	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU6EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EV	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU9EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU11EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU15EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Table 25: **Speed Grade Designations by Device *(Cont'd)***

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU17EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU19EG	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 26 lists the production released Zynq UltraScale+ MPSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 26: **Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages				
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-1
XCZU2EG					
XCZU3EG					
XCZU4EV					
XCZU5EV					
XCZU6EG					
XCZU7EV					
XCZU9EG					
XCZU11EG					
XCZU15EG					
XCZU17EG					
XCZU19EG					

Notes:

1. See Table 4 for the complete list of operating voltages by speed grade and device.
2. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Processor System (PS) Performance Characteristics

Table 27: **Processor Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 28: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 29: **PS DDR Performance for 23 x 23 mm or Larger Packages**

Symbol	Description(1)	Speed Grade			Units
		-3	-2	-1	
$F_{DDR4MAX}$	Maximum DDR4 interface performance.	2400		2400	Mb/s
$F_{LPDDR4MAX}$	Maximum LPDDR4 interface performance.(2)	2400		2400	Mb/s
$F_{DDR3MAX}$	Maximum DDR3 interface performance.	2133		2133	Mb/s
$F_{DDR3LMAX}$	Maximum DDR3L interface performance.	1866		1866	Mb/s
$F_{LPDDR3MAX}$	Maximum LPDDR3 interface performance.(3)	1600		1600	Mb/s

Notes:

1. DDR performance values are only for soldered single-rank memory with a single electrical load.
2. LPDDR4 support is only available as a 32-bit interface.
3. 64-bit LPDDR3 interface performance values are defined without ECC support.

Table 30: **PS DDR Performance for 21 x 21 mm Packages**

Symbol	Description(1)	Speed Grade			Units
		-3	-2	-1	
$F_{DDR4MAX}$	Maximum DDR4 interface performance.	2133		2133	Mb/s
$F_{LPDDR4MAX}$	Maximum LPDDR4 interface performance.(2)	2133		2133	Mb/s
$F_{DDR3MAX}$	Maximum DDR3 interface performance.	1866		1866	Mb/s
$F_{DDR3LMAX}$	Maximum DDR3L interface performance.	1600		1600	Mb/s
$F_{LPDDR3MAX}$	Maximum LPDDR3 interface performance.(3)	1600		1600	Mb/s

Notes:
1. DDR performance values are only for soldered single-rank memory with a single electrical load.
2. LPDDR4 support is only available as a 32-bit interface.
3. 64-bit LPDDR3 interface performance values are defined without ECC support.

Table 31: **PS DDR Performance for 19 x 19 mm Packages**

Symbol	Description(1)	Speed Grade			Units
		-3	-2	-1	
$F_{LPDDR4MAX}$	Maximum LPDDR4 interface performance.	1066		1066	Mb/s
$F_{DDR3MAX}$	Maximum DDR3 interface performance.	1066		1066	Mb/s
$F_{DDR3LMAX}$	Maximum DDR3L interface performance.	1066		1066	Mb/s
$F_{LPDDR3MAX}$	Maximum LPDDR3 interface performance.	1066		1066	Mb/s

Notes:
1. DDR performance values are only for soldered single-rank memory with a single electrical load.

Table 32: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency.	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency.	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency.	–	25	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency.	–	125	MHz
F_{FTMCLK}	Programmable logic trace monitor maximum frequency.	–	125	MHz
$F_{FCIDMACLK}$	FCI DMA maximum frequency.	–	333	MHz
F_{AXICLK}	Maximum AXI interface performance.	–	333	MHz
$F_{DPLIVEVIDEO}$	DisplayPort controller live video interface maximum frequency.	–	300	MHz

PS Switching Characteristics

PS Clocks

Table 33: **PS Reference Clock Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance.	–	–		%
$T_{DCPSCLK}$	PS_CLK duty cycle.		–		%
$T_{RFPSCLK}$	PS_CLK rise and fall time.	–	–		ns
F_{PSCLK}	PS_CLK frequency.	27	–	60	MHz

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs.

Table 34: **PS Crystal Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:

1. Required board components: Feedback resistor = 4.7 MΩ, PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 35: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	µs
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

Table 36: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time.(1)	10	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time.		–	–	PS_CLK Clock Cycles

Notes:

1. The time PS_POR_B must be asserted Low after all the PS supply voltages reach minimum levels.

Table 37: **PS Clocks Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{TOPSW\_MAINMAX}$	TOPSW_MAIN maximum frequency.	600		533	MHz
$F_{TOPSW\_LSBUSMAX}$	TOPSW_LSBUS maximum frequency.	100		100	MHz
$F_{GDMAMAX}$	GDMA maximum frequency.	600		600	MHz
$F_{DPDMAMAX}$	DPDMA maximum frequency.	600		600	MHz
$F_{LPD\_SWITCH\_CTRLMAX}$	LPD_SWITCH_CTRL maximum frequency.	600		500	MHz
$F_{LPD\_LSBUS\_CTRLMAX}$	LPD_LSBUS_CTRL maximum frequency.	100		100	MHz
$F_{ADMAMAX}$	ADMA maximum frequency.	600		500	MHz
$F_{APLL\_TO\_LPDMAX}$	APLL_TO_LPD maximum frequency.	533		533	MHz
$F_{DPLL\_TO\_LPDMAX}$	DPLL_TO_LPD maximum frequency.	533		533	MHz
$F_{VPLL\_TO\_LPDMAX}$	VPLL_TO_LPD maximum frequency.	533		533	MHz
$F_{IOPLL\_TO\_LPDMAX}$	IOPLL_TO_LPD maximum frequency.	533		533	MHz
$F_{RPLL\_TO\_FPDMAX}$	RPLL_TO_FPD maximum frequency.	533		533	MHz

PS Configuration

Table 38: **Processor Configuration Access Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency.	200	200	200	166	166	MHz

Table 39: **Boundary-Scan Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{TCK}	JTAG clock maximum frequency.	25	25	25	15	15	MHz
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup and hold.	4.0/2.0	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	16.1	16.1	16.1	24	24	ns, Max

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS NAND Memory Controller Interface

Table 40: **ONFI (SDR Mode 5) Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{ONFIALH5}$	ALE hold time	10.2	–	ns
$T_{ONFIALS5}$	ALE setup time	40.6	–	ns
$T_{ONFIAR5}$	ALE to RE_n delay	83.3	–	ns
$T_{ONFIADL5}$	Address cycle to data loading time	142.8	–	ns
$T_{ONFICLH5}$	CLE hold time	40.9	–	ns
$T_{ONFICLR5}$	CLE to RE_n delay	379.0	–	ns
$T_{ONFICLS5}$	CLE setup time	9.8	–	ns
$T_{ONFICS5}$	CE_n setup time	19.8	–	ns
$T_{ONFICH5}$	CE_n hold time	10.7	–	ns
$T_{ONFIDH5}$	Data hold time	10.1	–	ns
$T_{ONFIDS5}$	Data setup time	9.9	–	ns
$T_{ONFIRC5}$	RE_n cycle time	36.0	–	ns
$T_{ONFIREH5}$	RE_n High hold time	12.0	–	ns
$T_{ONFIRHW5}$	RE_n High to WE_n Low	119.3	–	ns
$T_{ONFIRP5}$	RE_n pulse width	24.0	–	ns
$T_{ONFIWC5}$	WE_n cycle time	36.0	–	ns
$T_{ONFIWH5}$	WE_n High hold time	12.0	–	ns
$T_{ONFIWP5}$	WE_n pulse width	24.0	–	ns
$T_{ONFIWB5}$	WE_n to Ready_n Low time	–	100	ns
$T_{ONFIWHR5}$	Command, address, or data input cycle to data output cycle	93.6	–	ns

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 41: **ONFI (SDR Mode 0) Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{ONFIALH0}$	ALE hold time	61.3	–	ns
$T_{ONFIALS0}$	ALE setup time	91.6	–	ns
$T_{ONFIAR0}$	ALE to RE_n delay	144.5	–	ns
$T_{ONFIADL0}$	Address cycle to data loading time	3406.8	–	ns
$T_{ONFICLH0}$	CLE hold time	20.6	–	ns
$T_{ONFICLR0}$	CLE to RE_n delay	144.0	–	ns
$T_{ONFICLS0}$	CLE setup time	50.6	–	ns
$T_{ONFICS0}$	CE_n setup time	70.8	–	ns
$T_{ONFICH0}$	CE_n hold time	21.0	–	ns
$T_{ONFIDH0}$	Data hold time	51.4	–	ns
$T_{ONFIDS0}$	Data setup time	50.5	–	ns
$T_{ONFIRC0}$	RE_n cycle time	120.0	–	ns
$T_{ONFIREH0}$	RE_n High hold time	60.0	–	ns

Table 41: **ONFI (SDR Mode 0) Switching Characteristics(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
$T_{ONFIRHW0}$	RE_n High to WE_n Low	272.3	–	ns
$T_{ONFIRP0}$	RE_n pulse width	60.0	–	ns
$T_{ONFIWC0}$	WE_n cycle time	120.0	–	ns
$T_{ONFIWH0}$	WE_n High hold time	60.0	–	ns
$T_{ONFIWP0}$	WE_n pulse width	60.0	–	ns
$T_{ONFIWB0}$	WE_n to Ready_n Low time	–	100	ns
$T_{ONFIWHR0}$	Command, address, or data input cycle to data output cycle	178.6	–	ns

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard with an 8 mA drive strength, fast slew rate, and a 15 pF load.

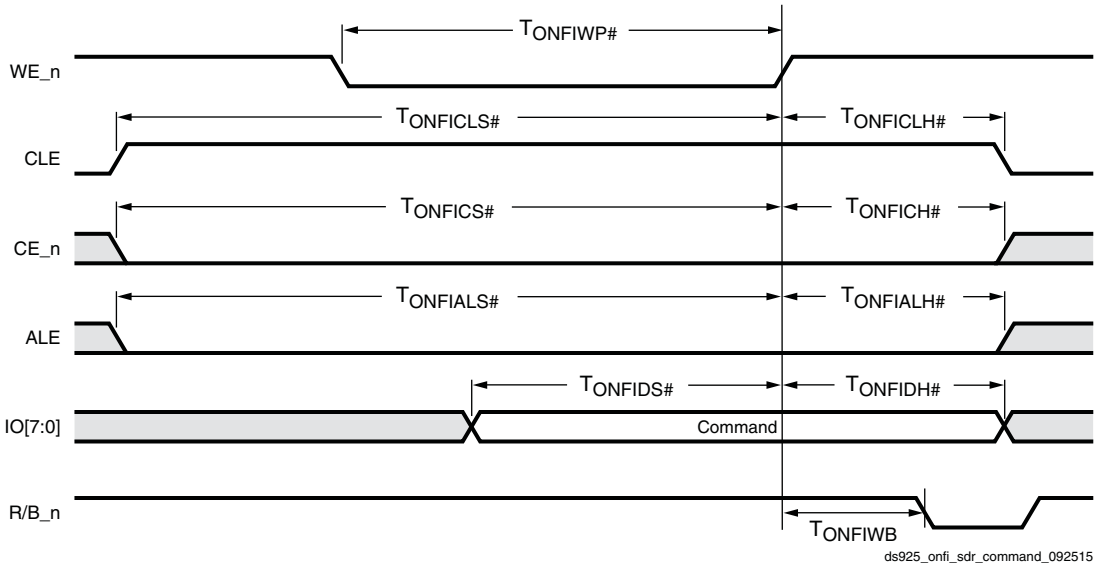

Figure 1: **ONFI SDR Command Latch Timing**

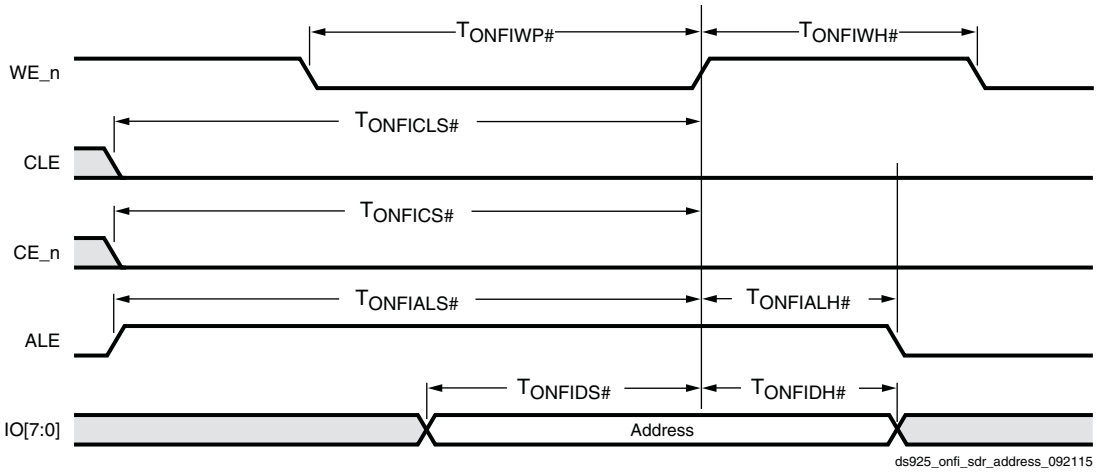

Figure 2: **ONFI SDR Address Latch Timing**

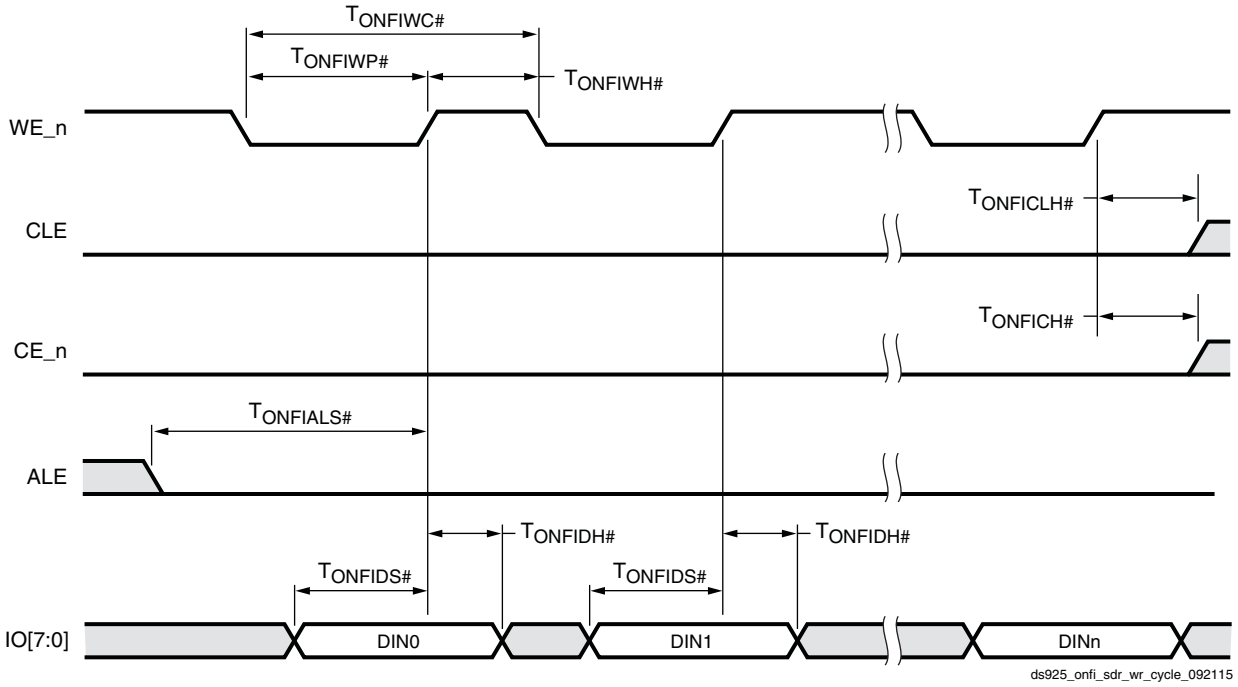

Figure 3: **ONFI SDR Data Write Cycle Timing**

Table 42: **ONFI NV-DDR (Mode 5) Switching Characteristics**

Symbol	Description	Min	Max	Units
$T_{ONFIDDRCK5}$	Clock cycle time	10	–	ns
$T_{ONFIDDRCKL5}$	Clock cycle Low time	0.43	0.57	$T_{ONFIDDRCK5}$
$T_{ONFIDDRCKH5}$	Clock cycle High time	0.43	0.57	$T_{ONFIDDRCK5}$
$T_{ONFIDDRCALS5}$	W/R_n, CLE, and ALE setup time	2.20	–	ns
$T_{ONFIDDRCALH5}$	W/R_n, CLE and ALE hold time	2.20	–	ns
$T_{ONFIDDRCS5}$	CE_n setup time	15.00	–	ns
$T_{ONFIDDRCH5}$	CE_n hold time	20.00	–	ns
$T_{ONFIDDRCAD5}$	Command, address, data delay time	25	–	ns
$T_{ONFIDDRDQSS5}$	Data input to first DQS latching transition	0.75	1.25	$T_{ONFIDDRCK5}$
$T_{ONFIDDRWPRE5}$	DQS write preamble	1.5	–	$T_{ONFIDDRCK5}$
$T_{ONFIDDRDSS5}$	DQS falling edge to CLK rising setup time	0.2	–	$T_{ONFIDDRCK5}$
$T_{ONFIDDRDSH5}$	DQS falling edge to CLK rising hold time	0.2	–	$T_{ONFIDDRCK5}$
$T_{ONFIDDRDQSH5}$	DQS input High pulse width	0.4	0.6	$T_{ONFIDDRCK5}$
$T_{ONFIDDRDQSL5}$	DQS input Low pulse width	0.4	0.6	$T_{ONFIDDRCK5}$
$T_{ONFIDDRDS5}$	Data setup time	0.9	–	ns
$T_{ONFIDDRDH5}$	Data hold time	0.9	–	ns
$T_{ONFIDDRWPST5}$	DQS write post-amble	1.5	–	$T_{ONFIDDRCK5}$
$T_{ONFIDDRDSC5}$	Average DQS cycle time	10	–	ns
$T_{ONFIDDRDQSCK5}$	Access window of DQS from CLK	3	25	ns
$T_{ONFIDDRCLK5}$	NAND clock frequency	-	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V and LVCMOS 3.3V I/O standards with a 12 mA drive strength, fast slew rate, and a 30 pF load.

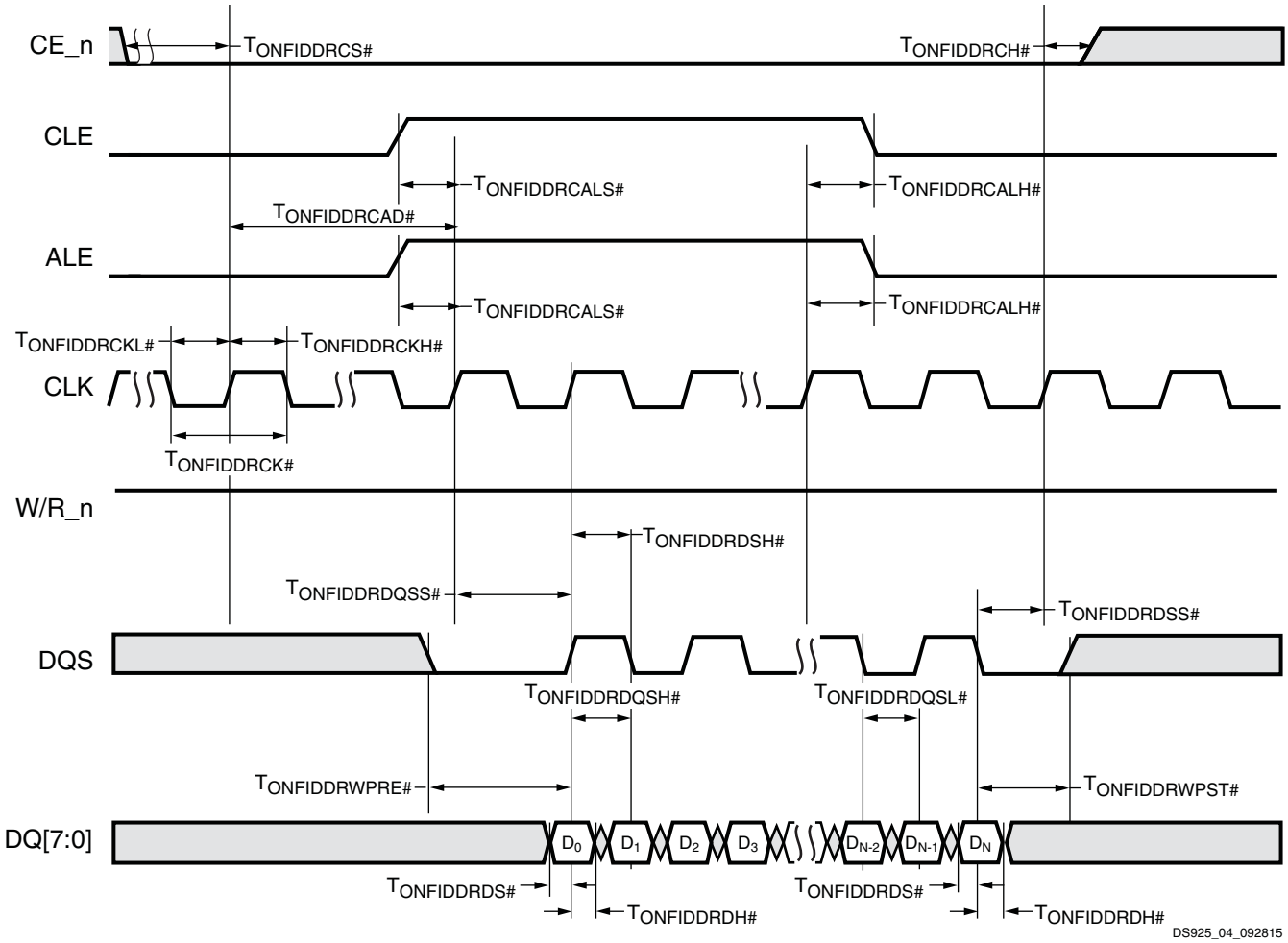

Figure 4: **ONFI NV-DDR (Mode 5) Write Timing**

PS Quad-SPI Controller Interface

Table 43: **Generic Quad-SPI Interface(1)**

Symbol	Description	Load Conditions(2)	Min	Max	Units
Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standards.					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
$T_{QSPISSSCLK1}$	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
$T_{QSPISCLKSS1}$	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
$T_{QSPICKO1}$	Clock to output delay, all outputs.	15 pF	2.9	4.5	ns
$T_{QSPIDCK1}$	Setup time, all inputs.	15 pF	0.4	–	ns
$T_{QSPICKD1}$	Hold time, all inputs.	15 pF	1.0	–	ns
$F_{QSPICLK1}$	Quad-SPI device clock frequency.	15 pF	–	150	MHz
$F_{QSPIREFCLK1}$	Quad-SPI reference clock frequency.	15 pF	–	300	MHz
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standards.					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK2}$	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPISCLKSS2}$	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPICKO2}$	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
$T_{QSPIDCK2}$	Setup time, all inputs.	15 pF	1.8	–	ns
		30 pF	1.8	–	ns
$T_{QSPICKD2}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPICLK2}$	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz
$F_{QSPIREFCLK2}$	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK3}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK3}$	Slave select asserted to next clock edge.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS3}$	Clock edge to slave select deasserted.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO3}$	Clock to output delay, all outputs.	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns

Table 43: **Generic Quad-SPI Interface(1) *(Cont'd)***

Symbol	Description	Load Conditions(2)	Min	Max	Units
$T_{QSPIDCK3}$	Setup time, all inputs.	15 pF	13.4	–	ns
		30 pF	14.1	–	ns
$T_{QSPICKD3}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK3}$	Quad-SPI reference clock frequency.	15 pF	–	160	MHz
		30 pF	–	160	MHz
$F_{QSPICLK3}$	Quad-SPI clock frequency.	15 pF	–	40	MHz
		30 pF	–	40	MHz
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 3.3V I/O standard.					
$T_{DCQSPICLK4}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK4}$	Slave select asserted to next clock edge.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS4}$	Clock edge to slave select deasserted.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO4}$	Clock to output delay, all outputs.	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns
$T_{QSPIDCK4}$	Setup time, all inputs.	15 pF	13.9	–	ns
		30 pF	14.9	–	ns
$T_{QSPICKD4}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK4}$	Quad-SPI reference clock frequency.	15 pF	–	160	MHz
		30 pF	–	160	MHz
$F_{QSPICLK4}$	Quad-SPI clock frequency.	15 pF	–	40	MHz
		30 pF	–	40	MHz

Notes:

1. The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate. The test conditions are configured for the generic Quad-SPI interface at 40 MHz with an 8 mA drive strength and fast slew rate.
2. 30 pF loads are for dual-parallel stacked or stacked modes.

Table 44: **Linear Quad-SPI Interface(1)**

Symbol	Description	Load Conditions(2)	Min	Max	Units
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standards.					
$T_{DCQSPICLK5}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK5}$	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPISCLKSS5}$	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPICKO5}$	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
$T_{QSPIDCK5}$	Setup time, all inputs.	15 pF	1.9	–	ns
		30 pF	1.9	–	ns
$T_{QSPICKD5}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK5}$	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz
$F_{QSPICLK5}$	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK6}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK6}$	Slave select asserted to next clock edge.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS6}$	Clock edge to slave select deasserted.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO6}$	Clock to output delay, all outputs.	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns
$T_{QSPIDCK6}$	Setup time, all inputs.	15 pF	13.4	–	ns
		30 pF	13.4	–	ns
$T_{QSPICKD6}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK6}$	Quad-SPI reference clock frequency.	15 pF	–	160	MHz
		30 pF	–	160	MHz
$F_{QSPICLK6}$	Quad-SPI device clock frequency.	15 pF	–	40	MHz
		30 pF	–	40	MHz

Table 44: **Linear Quad-SPI Interface(1) *(Cont'd)***

Symbol	Description	Load Conditions(2)	Min	Max	Units
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 3.3V I/O standard.					
$T_{DCQSPICLK7}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK7}$	Slave select asserted to next clock edge.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS7}$	Clock edge to slave select deasserted.	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO7}$	Clock to output delay, all outputs.	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns
$T_{QSPIDCK7}$	Setup time, all inputs.	15 pF	14.0	–	ns
		30 pF	14.0	–	ns
$T_{QSPICKD7}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK7}$	Quad-SPI reference clock frequency.	15 pF	–	160	MHz
		30 pF	–	160	MHz
$F_{QSPICLK7}$	Quad-SPI device clock frequency.	15 pF	–	40	MHz
		30 pF	–	40	MHz

Notes:

1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate. The test conditions are configured for the linear Quad-SPI interface at 40 MHz with an 8 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.

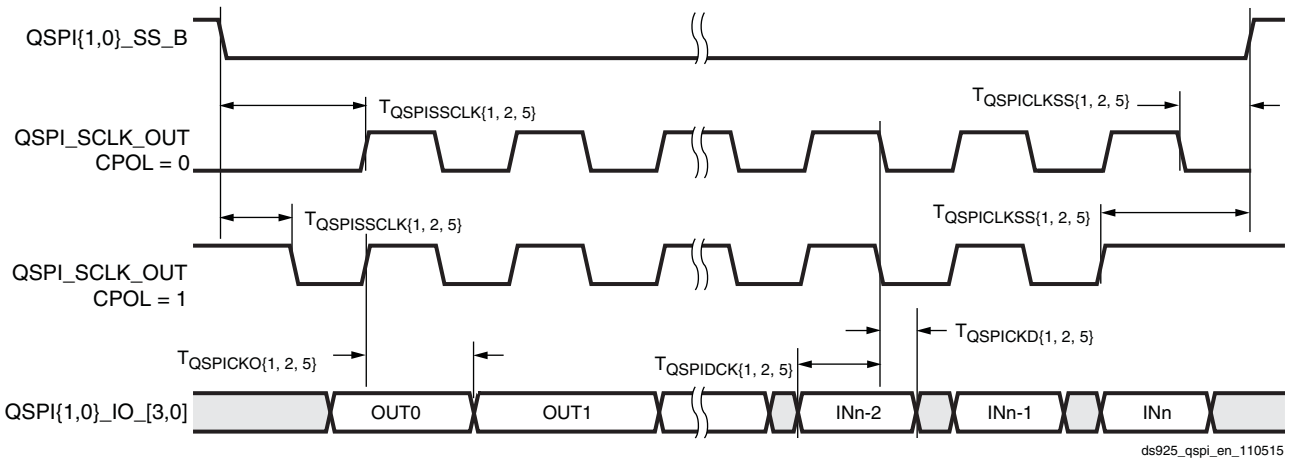

Figure 5: **Quad-SPI Interface (Feedback Clock Enabled) Timing**

PS USB Interface

Table 45: **ULPI Interface(1)**

Symbol	Description	Min	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs.	4.5	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs.	0	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs.	2.0	8.86	ns
$F_{ULPICLK}$	ULPI reference clock frequency.	–	60	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

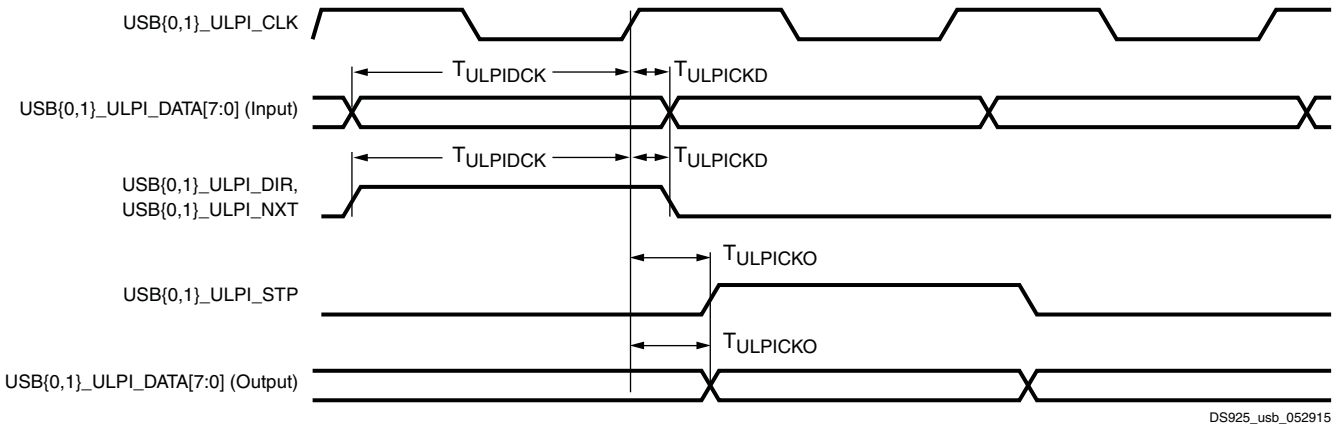

Figure 6: **ULPI Interface Timing**

PS Gigabit Ethernet Controller Interface

Table 46: **RGMII Interface(1)**

Symbol	Description	Min	Max	Units
$T_{DCGEMTXCLK}$	Transmit clock duty cycle.	45	55	%
$T_{GEMTXCKO}$	TXD output clock to out time.	–0.5	0.5	ns
$T_{GEMRXDCK}$	RXD input setup time.	0.8	–	ns
$T_{GEMRXCKD}$	RXD input hold time.	0.8	–	ns
$T_{MDIOCLK}$	MDC output clock period.	400	–	ns
$T_{MDIOCKL}$	MDC low time.	160	–	ns
$T_{MDIOCKH}$	MDC high time.	160	–	ns
$T_{MDIODCK}$	MDIO input data setup time.	80	–	ns
$T_{MDIOCKD}$	MDIO input data hold time.	0.0	–	ns
$T_{MDIOCKO}$	MDIO output data delay time.	–1.0	15	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency.	–	125	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency.	–	125	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency.	–	125	MHz
$F_{TSU\_REF\_CLK}$	Time stamp unit reference clock frequency.	–	250	MHz

Notes:

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

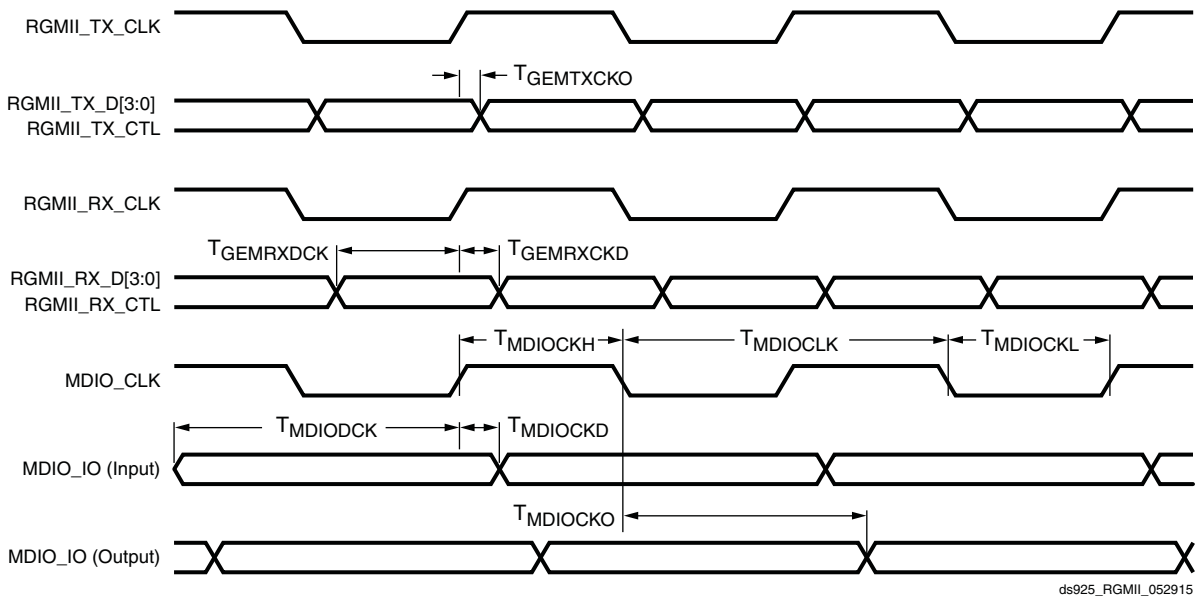

Figure 7: **RGMII Interface Timing**

PS SD/SDIO Controller Interface

Table 47: **SD/SDIO Interface(1)**

Symbol	Description	Min	Max	Units
SD/SDIO Interface DDR50 Mode				
$T_{DCDDRCLK}$	SD device clock duty cycle.	45	55	%
$T_{SDDDRCKO1}$	Clock to output delay, data.	1.0	6.8	ns
$T_{SDDDRDCK1}$	Input setup time, data.	1.4	–	ns
$T_{SDDDRCKD1}$	Input hold time, data.	1.5	–	ns
$T_{SDDDRDCK2}$	Input setup time, command.	4.7	–	ns
$T_{SDDDRCKD2}$	Input hold time, command.	1.5	–	ns
$T_{SDDDRCKO2}$	Clock to output delay, command.	1.0	13.8	ns
$F_{SDDDRCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface SDR104				
$T_{DCSDHSCLK1}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO1}$	Clock to output delay, all outputs.	1.0	3.2	ns
$T_{SDSDRDCK1}$	Input setup time, all inputs.	0.4	–	ns
$T_{SDSDRCKD1}$	Input hold time, all inputs.	0.4	–	ns
$F_{SDSDRCLK1}$	SDR104 mode device clock frequency.	–	200	MHz
SD/SDIO Interface SDR50/25				
$T_{DCSDHSCLK2}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO2}$	Clock to output delay, all outputs.	1.0	6.8	ns
$T_{SDSDRDCK2}$	Input setup time, all inputs.	0.76	–	ns
$T_{SDSDRCKD2}$	Input hold time, all inputs.	1.5	–	ns
$F_{SDSDRCLK2}$	SDR50/25 mode device clock frequency.	–	100	MHz
SD/SDIO Interface SDR12				
$T_{DCSDHSCLK3}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO3}$	Clock to output delay, all outputs.	1.0	36.8	ns
$T_{SDSDRDCK3}$	Input setup time, all inputs.	24.0	–	ns
$T_{SDSDRCKD3}$	Input hold time, all inputs.	1.5	–	ns
$F_{SDSDRCLK3}$	SDR12 mode device clock frequency.	–	25	MHz
SD/SDIO Interface High-Speed Mode				
$T_{DCSDHSCLK}$	SD device clock duty cycle.	47	53	%
$T_{SDHSCKO}$	Clock to output delay, all outputs.	2.2	13.8	ns
$T_{SDHSDCK}$	Input setup time, all inputs.	4.4	–	ns
$T_{SDHSCKD}$	Input hold time, all inputs.	2.5	–	ns
$F_{SDHSCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface Standard Mode				
$T_{DCSDSCLK}$	SD device clock duty cycle.	44	55	%
T_{SDSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T_{SDSDCK}	Input setup time, all inputs.	2.0	–	ns
T_{SDSCKD}	Input hold time, all inputs.	2.0	–	ns

Table 47: **SD/SDIO Interface(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
$F_{SDIDCLK}$	Clock frequency in identification mode.	–	400	KHz
F_{SDSCLK}	Standard SD device clock frequency.	–	19	MHz

Notes:

1. The test conditions are configured for all SD/SDIO modes except SD/SDIO standard mode with a 12 mA drive strength and a 30 pF load. For SD/SDIO standard mode, the test conditions use a 8 mA drive strength and a 30 pF load.

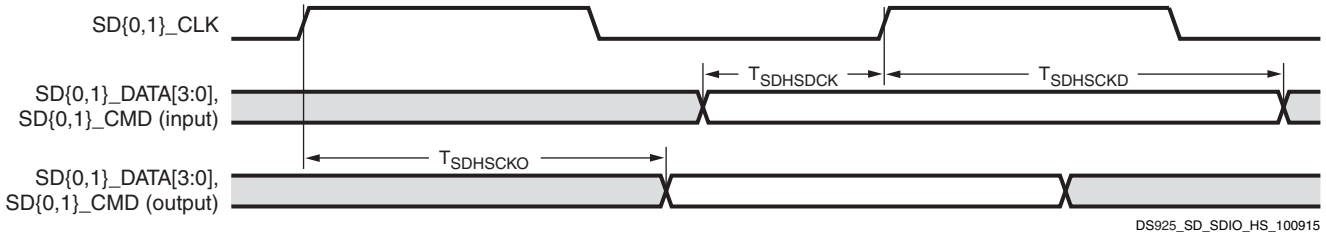

Figure 8: **SD/SDIO Interface High Speed Mode Timing Diagram**

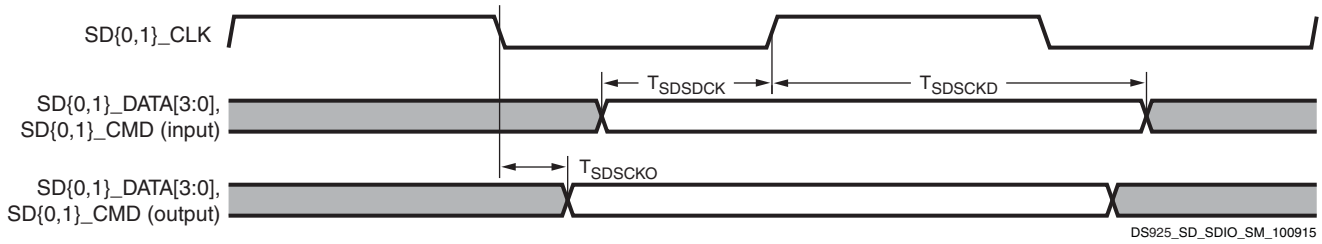

Figure 9: **SD/SDIO Interface Standard Mode Timing Diagram**

PS eMMC Standard Interface

Table 48: **eMMC Standard Interface(1)**

Symbol	Description	Min	Max	Units
eMMC Standard Interface				
$T_{DCEMMCHSCLK}$	eMMC clock duty cycle.	45	55	%
$T_{EMMCHSCKO}$	Clock to output delay, all outputs.	–2.0	4.5	ns
$T_{EMMCHSDCK}$	Input setup time, all inputs.	2.0	–	ns
$T_{EMMCHSCKD}$	Input hold time, all inputs.	2.0	–	ns
$F_{EMMCHSCLK}$	eMMC clock frequency.	–	25	MHz
eMMC High-Speed SDR Interface				
$T_{DCEMMCHSCLK}$	eMMC high-speed SDR clock duty cycle.	45	55	%
$T_{EMMCHSCKO}$	Clock to output delay, all outputs.	3.2	16.8	ns
$T_{EMMCHSDCK}$	Input setup time, all inputs.	4.7	–	ns
$T_{EMMCHSCKD}$	Input hold time, all inputs.	2.5	–	ns
$F_{EMMCHSCLK}$	eMMC high speed SDR clock frequency.	–	50	MHz
eMMC High-Speed DDR Interface				
$T_{DCEMMCDDRCLK}$	eMMC high-speed DDR clock duty cycle.	45	55	%
$T_{EMMCDDRSCKO1}$	Data clock to output delay.	2.7	7.3	ns
$T_{EMMCDDRDCK1}$	Data input setup time.	1.4	–	ns
$T_{EMMCDDRCKD1}$	Data input hold time.	1.5	–	ns
$T_{EMMCDDRSCKO2}$	Command clock to output delay.	3.2	16	ns
$T_{EMMCDDRDCK2}$	Command input setup time.	3.9	–	ns
$T_{EMMCDDRCKD2}$	Command input hold time.	2.5	–	ns
$F_{EMMCDDRCLK}$	eMMC high-speed DDR clock frequency.	–	50	MHz
eMMC HS200 Interface				
$T_{DCEMMCHS200CLK}$	eMMC HS200 clock duty cycle.	45	55	%
$T_{EMMCHS200CKO}$	Clock to output delay, all outputs.	1.0	3.4	ns
$T_{EMMCHS200DCK}$	Input setup time, all inputs.	0.4	–	ns
$T_{EMMCHS200CKD}$	Input hold time, all inputs.	0.4	–	ns
$F_{EMMCHS200CLK}$	eMMC HS200 clock frequency.	–	200	MHz

Notes:

1. The test conditions for eMMC standard mode use an 8 mA drive strength, fast slew rate, and a 30 pF load. For eMMC high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other eMMC modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS I2C Controller Interface

Table 49: **I2C Interface(1)**

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	µs
$T_{I2CFCKH}$	SCL High time.	0.6	–	µs
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	µS
$T_{I2CSCKH}$	SCL High time.	4.0	–	µS
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

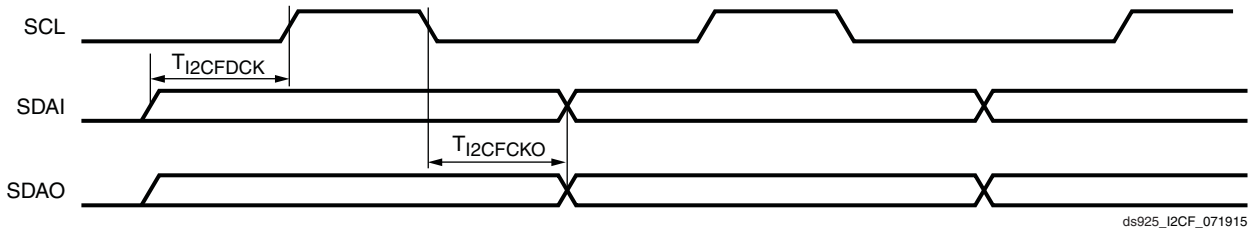

Figure 10: **I2C Fast Mode Interface Timing**

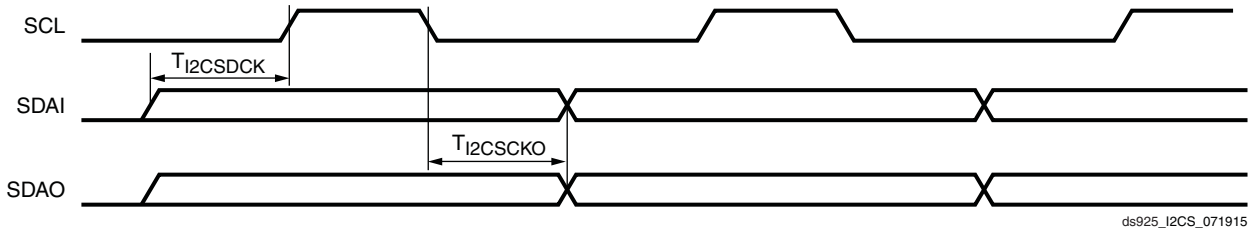

Figure 11: **I2C Standard Mode Interface Timing**

PS SPI Controller Interface

Table 50: **SPI Interfaces**(1)

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSSCLK}$	Slave select asserted to first active clock edge.	1(2)	–	F_{SPI_REFCLK} cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1(2)	–	F_{SPI_REFCLK} cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–1.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	5.0(3)	–	ns
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPIDCK}$	Slave select asserted to first active clock edge.	5	–	F_{SPI_REFCLK} cycles
$T_{SSPICKD}$	Last active clock edge to slave select deasserted.	5	–	F_{SPI_REFCLK} cycles
$T_{SSPICKO}$	Input setup time for MOSI and slave select.	5.0	–	ns
$T_{SSPISSCLK}$	Input hold time for MOSI and slave select.	5.0	–	ns
$T_{SSPICLKSS}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.
3. The $T_{MSPICKD}$ Min = $(1/F_{SPI\_REF\_CLK})$ for frequencies below 50 MHz.

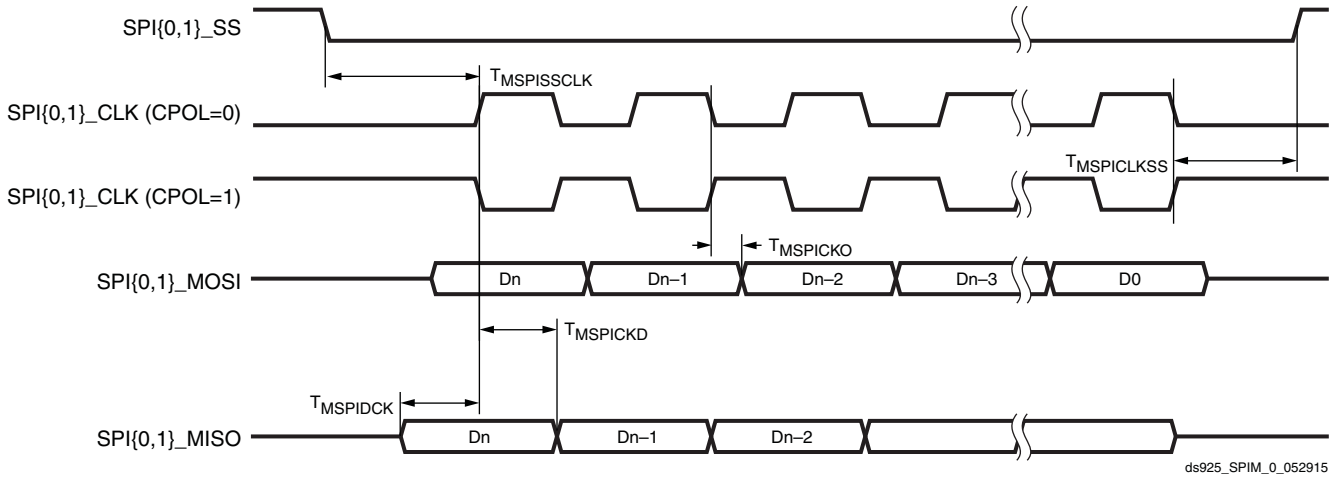

Figure 12: **SPI Master (CPHA = 0) Interface Timing**

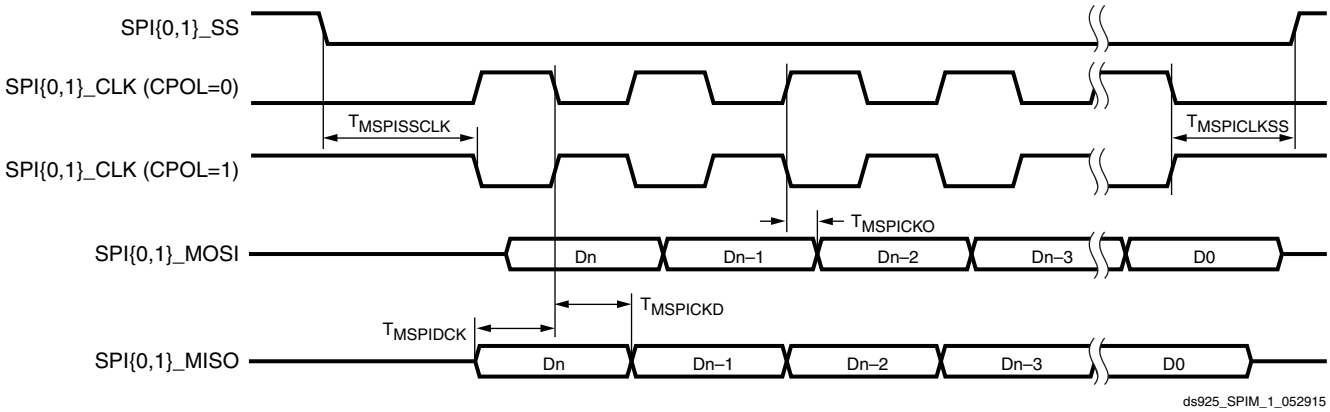

Figure 13: **SPI Master (CPHA = 1) Interface Timing**

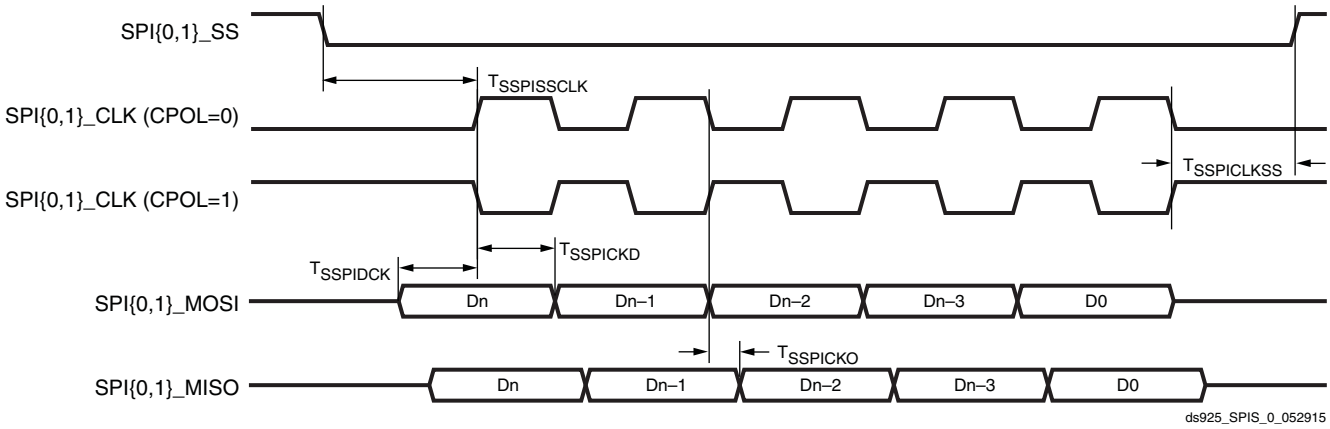

Figure 14: **SPI Slave (CPHA = 0) Interface Timing**

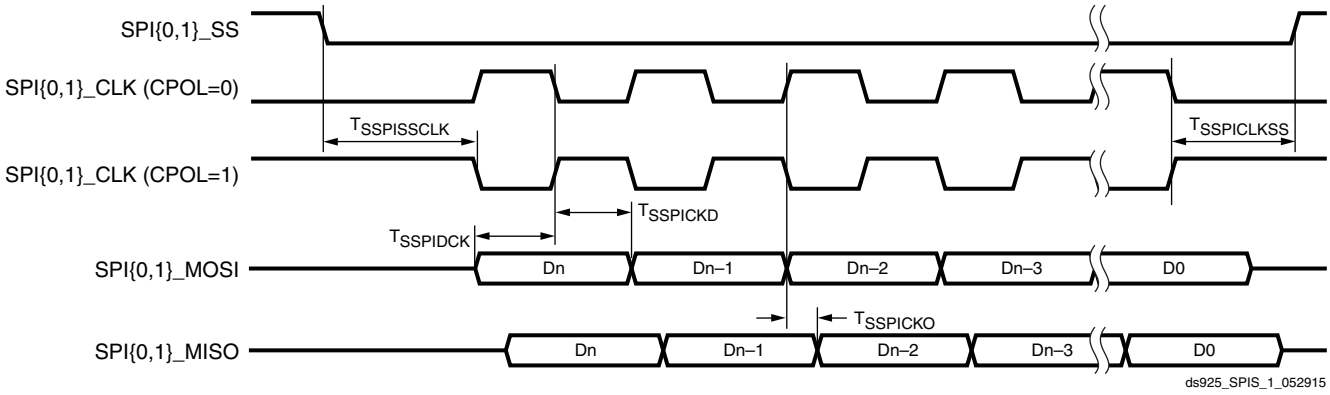

Figure 15: **SPI Slave (CPHA = 1) Interface Timing**

PS CAN Controller Interface

Table 51: **CAN Interface(1)**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	µs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS DAP Interface

Table 52: **DAP Interface(1)**

Symbol	Description(2)	Min	Max	Units
$T_{PDAPDCK}$	PS DAP input setup time.	3.0	–	ns
$T_{PDAPCKD}$	PS DAP input hold time.	2.0	–	ns
$T_{PDAPCKO}$	PS DAP clock to out delay.	–	10.86	ns
$T_{PDAPCLK}$	PS DAP clock frequency.	–	44	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

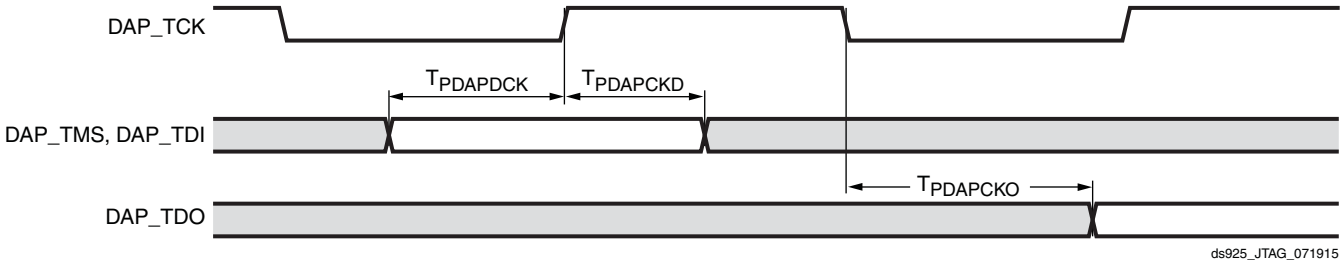

Figure 16: **Processor JTAG Interface Timing**

PS UART Interface

Table 53: **UART Interface(1)**

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Transmit baud rate.	–	6.25(2)	Mb/s
$BAUD_{RXMAX}$	Receive baud rate.	–	6.25(2)	Mb/s
$F_{UARTCLK}$	UART clock frequency.	–	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. An additional reference clock (uart_clk) is needed.

PS General Purpose I/O Interface

Table 54: **General Purpose I/O (GPIO) Interface**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input High pulse width.	1.0	–	µs
$T_{PWGPIOL}$	Input Low pulse width.	1.0	–	µs

PS Trace Interface

Table 55: **Trace Interface(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs.	–0.5	0.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle.	45	55	%
F_{TCECLK}	Trace clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Triple Timer Counter Interface

Table 56: **Triple Timer Counter Interface**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple time counter output clock pulse width.		–	ns
$F_{TTCOCLK}$	Triple time counter output clock frequency.	–		MHz
$T_{TTCICLKL}$	Triple time counter input clock high pulse width.	5.1	–	ns
$T_{TTCICLKH}$	Triple time counter input clock low pulse width.	4.9	–	ns
$F_{TTCICLK}$	Triple time counter input clock frequency.	–	100	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 57: **Watchdog Timer Interface**

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	–	100	MHz

PS GTR Transceiver

Table 58: **PS-GTR Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled).		100	–	1200	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.			–	$V_{PS\_MGTRAVCC}$	mV
V_{CMIN}	Common mode input voltage.		–	2/3 $V_{PS\_MGTRAVCC}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage.(1)	Transmitter output swing is set to maximum value.		1000	–	mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based).		$V_{PS\_MGTRAVCC} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance.		–	100	–	Ω
R_{OUT}	Differential output resistance.		–	100	–	Ω
$R_{MGTRREF}$	Resistor value between calibration resistor pin to GND.		497.5	500	502.5	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages).		–	–		ps
C_{EXT}	Recommended external AC coupling capacitor.(2)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 59: **PS-GTR Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 60: **PS-GTR Transceiver Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{GTRMAX}	GTR maximum line rate.	6.0	6.0	6.0	Gb/s
F_{GTRMIN}	GTR minimum line rate.	1.25	1.25	1.25	Gb/s

Table 61: **PS-GTR Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Min	Typ	Max	Units
T_{LOCK}	Initial PLL lock.	–	–	0.11	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	–	–	24×10^6	UI

Table 62: **PS-GTR Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.	PCI Express	–	100	–	MHz
		SATA	25	125	150	MHz
		USB 3.0	24	40/48/50/52	100	MHz
		DisplayPort	27	54	108	MHz
		SGMII	–	125	–	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only.	40	–	60	%
		USB 3.0 with reference clock <40 MHz.	47.5	–	52.5	%

Table 63: **PS-GTR Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T_{RTX}	TX rise time.	20%–80%	0.2	–	0.41	UI
T_{FTX}	TX fall time.	80%–20%	0.2	–	0.41	UI
$V_{TXOOBVDPP}$	Electrical idle amplitude.		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time.		–	–	8	ns
$T_{J6.0}$	Total jitter(1)	6 Gb/s	–	–		UI
$D_{J6.0}$	Deterministic jitter(1)		–	–		UI
$T_{J5.4}$	Total jitter(1)	5.4 Gb/s	–	–		UI
$D_{J5.4}$	Deterministic jitter(1)		–	–		UI
$T_{J5.0}$	Total jitter(1)	5 Gb/s	–	–		UI
$D_{J5.0}$	Deterministic jitter(1)		–	–		UI
$T_{J3.0}$	Total jitter(1)	3 Gb/s	–	–		UI
$D_{J3.0}$	Deterministic jitter(1)		–	–		UI
$T_{J2.7}$	Total jitter(1)	2.7 Gb/s	–	–		UI
$D_{J2.7}$	Deterministic jitter(1)		–	–		UI
$T_{J2.5}$	Total jitter(1)	2.5 Gb/s	–	–		UI
$D_{J2.5}$	Deterministic jitter(1)		–	–		UI
$T_{J1.62}$	Total jitter(1)	1.62 Gb/s	–	–		UI
$D_{J1.62}$	Deterministic jitter(1)		–	–		UI
$T_{J1.5}$	Total jitter(1)	1.5 Gb/s	–	–		UI
$D_{J1.5}$	Deterministic jitter(1)		–	–		UI
$T_{J1.25}$	Total jitter(1)	1.25 Gb/s	–	–		UI
$D_{J1.25}$	Deterministic jitter(1)		–	–		UI

Notes:

1. All jitter values are based on a bit-error ratio of 10^{-12}.

Table 64: **PS-GTR Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRRX}	Serial data rate.		1.25	–	6	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data.	PCIe SATA	2	–	11	ns
		USB 3.0	31	–	64	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak.		65	–	175	mV
RX_{SST}	Receiver spread-spectrum tracking.	Modulated at 33 KHz	–5000	–	0	ppm
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance.	All data rates	–350	–	350	ppm
SJ Jitter Tolerance(1)						
$J_{T\_SJ6.6}$	Sinusoidal jitter(2)	6.0 Gb/s		–	–	UI
$J_{T\_SJ5.4}$	Sinusoidal jitter(2)	5.4 Gb/s		–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter(2)	5.0 Gb/s		–	–	UI
J_{T_SJ3}	Sinusoidal jitter(2)	3.0 Gb/s		–	–	UI
$J_{T\_SJ2.7}$	Sinusoidal jitter(2)	2.7 Gb/s		–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter(2)	2.5 Gb/s		–	–	UI
$J_{T\_SJ1.62}$	Sinusoidal jitter(2)	1.62 Gb/s		–	–	UI
$J_{T\_SJ1.5}$	Sinusoidal jitter(2)	1.5 Gb/s		–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter(2)	1.25 Gb/s		–	–	UI
SJ Jitter Tolerance with Stressed Eye(1)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye.(3)	3.2 Gb/s		–	–	UI
J_{T_TJSE6}		6.0 Gb/s		–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye.(3)	3.2 Gb/s		–	–	UI
J_{T_SJSE6}		6.0 Gb/s		–	–	UI

Notes:
1. All jitter values are based on a bit-error ratio of 10^{-12}.
2. The frequency of the injected sinusoidal jitter is 10 MHz.
3. Composite jitter with RX equalizer enabled.

Table 65: **PCI Express Protocol Characteristics (GTR Transceivers)(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter.	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter.	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance.	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error.	5000	0.4	–	UI
	Receiver inherent deterministic timing error.		0.3	–	UI

Notes:
1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 66: **Serial ATA (SATA) Protocol Characteristics (GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter.	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter.	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter.	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance.	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	3000	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	6000	0.16	–	UI

Table 67: **DisplayPort Protocol Characteristics (GTR Transceivers)(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter.	1620	–	0.42	UI
HBR	Total transmitter jitter.	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter.	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter.	5400	–	0.58	UI

Notes:
1. Only the transmitter is supported.

Table 68: **USB 3.0 Protocol Characteristics (GTR Transceivers)**

Standard	Description	Line Rate (Gb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 69: **Serial-GMII Protocol Characteristics (GTR Transceivers)**

Standard	Description	Line Rate (Gb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1.25	–	0.375	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1.25	0.25	–	UI

PS System Monitor Specifications

Table 70: **PS SYSMON Specifications**

Parameter	Comments	Conditions	Min	Typ	Max	Units
V_{CC_PSADC} = 1.8V ±3%, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy (T_j = –55°C to 125°C) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		T_j = –40°C to 100°C	–	–	±5	°C
		T_j = –40°C to 125°C	–	–	±6.5	°C
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	T_j = –40°C to 125°C	–	–		%

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Zynq UltraScale+ MPSoC. These values are subject to the same guidelines as the AC Switching Characteristics, page 21. In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 71: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	1250	1250	1250	1250	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	710	710	625	710	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	1250	1250	1250	1250	1250	Mb/s
	HD						Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	710	710	625	710	625	Mb/s
	HD						Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

Table 72: **LVDS Native Mode Performance(1)**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
LVDS TX DDR (TX_BITSLICE 4:1, 8:1)	HP	1600	1600	1250	1600	1250	Mb/s
LVDS TX SDR (TX_BITSLICE 2:1, 4:1)	HP	800	800	625	800	625	Mb/s
LVDS RX DDR (RX_BITSLICE 1:4, 1:8)(2)	HP	1600	1600	1250	1600	1250	Mb/s
LVDS RX SDR (RX_BITSLICE 1:2, 1:4)(2)	HP	800	800	625	800	625	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

Table 73: **LVDS Native-Mode 1000BASE-X Support(1)**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* (UG583), electrical analysis, and characterization of the system.

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	Package(1)	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM(2)(3)	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM(2)(4)	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM(2)(5)	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM(2)(3)	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM(2)(4)	1866	1866	1600	1600	1333	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM(2)(3)	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM(2)(4)	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM(2)(5)	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(4)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(5)	800	800	800	800	606	Mb/s
DDR3L	All FFV packages and FBVB900	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(4)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(5)	800	800	800	800	606	Mb/s
	SFVC784	Single rank component	1600	1600	1600	1600	1600	Mb/s
		1 rank DIMM(2)(3)	1333	1333	1333	1333	1333	Mb/s
		2 rank DIMM(2)(4)	1066	1066	1066	1066	1066	Mb/s
		4 rank DIMM(2)(5)	606	606	606	606	606	Mb/s
QDR II+	All	Single rank component(6)	633	633	600	600	550	MHz
RLDRAM 3	All FFV packages and FBVB900	Single rank component	1200	1200	1066	1066	933	MHz
	SFVC784	Single rank component	1066	1066	933	933	800	MHz
QDR IV XP	All	Single rank component(7)	1066	1066	1066	933	933	MHz
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:

1. The SBVA484 and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
5. Includes: 2 rank 2 slot, 4 rank 1 slot.
6. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.
7. This memory interface is not production qualified and specification is subject to change.

IOB Pad Input, Output, and 3-State

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the INTERMDISABLE pin is used.

Table 75: **IOB High Density (HD) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.569	0.577	0.638	0.577	0.558	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
DIFF_HSTL_I_18_S	0.569	0.577	0.638	0.577	0.558	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
DIFF_HSTL_I_F	0.566	0.56	0.633	0.56	0.552	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
DIFF_HSTL_I_S	0.566	0.56	0.633	0.56	0.552	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
DIFF_HSUL_12_F	0.562	0.547	0.599	0.547	0.522	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns
DIFF_HSUL_12_S	0.562	0.547	0.599	0.547	0.522	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns
DIFF_SSTL12_F	0.566	0.552	0.609	0.552	0.522	1.463	1.561	1.704	1.561	1.555	1.463	1.561	1.704	1.561	1.555	ns
DIFF_SSTL12_S	0.566	0.552	0.609	0.552	0.522	1.707	1.747	1.909	1.747	1.716	1.707	1.747	1.909	1.747	1.716	ns
DIFF_SSTL135_F	0.577	0.560	0.613	0.56	0.527	1.473	1.590	1.728	1.590	1.585	1.473	1.590	1.728	1.590	1.585	ns
DIFF_SSTL135_II_F	0.577	0.560	0.613	0.56	0.527	1.406	1.498	1.636	1.498	1.491	1.406	1.498	1.636	1.498	1.491	ns
DIFF_SSTL135_II_S	0.577	0.560	0.613	0.56	0.527	1.576	1.649	1.789	1.649	1.618	1.576	1.649	1.789	1.649	1.618	ns
DIFF_SSTL135_S	0.577	0.560	0.613	0.56	0.527	1.817	1.887	2.046	1.887	1.846	1.817	1.887	2.046	1.887	1.846	ns
DIFF_SSTL15_F	0.566	0.560	0.633	0.56	0.552	1.474	1.592	1.734	1.592	1.597	1.474	1.592	1.734	1.592	1.597	ns
DIFF_SSTL15_II_F	0.566	0.560	0.633	0.56	0.552	1.406	1.511	1.659	1.511	1.505	1.406	1.511	1.659	1.511	1.505	ns
DIFF_SSTL15_II_S	0.566	0.560	0.633	0.56	0.552	1.618	1.700	1.856	1.700	1.668	1.618	1.700	1.856	1.700	1.668	ns
DIFF_SSTL15_S	0.566	0.560	0.633	0.56	0.552	1.734	1.804	1.957	1.804	1.775	1.734	1.804	1.957	1.804	1.775	ns
DIFF_SSTL18_II_F	0.569	0.577	0.638	0.577	0.558	1.357	1.473	1.604	1.473	1.469	1.357	1.473	1.604	1.473	1.469	ns
DIFF_SSTL18_II_S	0.569	0.577	0.638	0.577	0.558	1.511	1.629	1.784	1.629	1.616	1.511	1.629	1.784	1.629	1.616	ns
DIFF_SSTL18_I_F	0.569	0.577	0.638	0.577	0.558	1.335	1.431	1.563	1.431	1.429	1.335	1.431	1.563	1.431	1.429	ns
DIFF_SSTL18_I_S	0.569	0.577	0.638	0.577	0.558	1.692	1.802	1.961	1.802	1.760	1.692	1.802	1.961	1.802	1.760	ns
HSTL_I_18_F	0.596	0.606	0.668	0.606	0.571	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
HSTL_I_18_S	0.596	0.606	0.668	0.606	0.571	1.359	1.452	1.587	1.452	1.456	1.359	1.452	1.587	1.452	1.456	ns
HSTL_I_F	0.597	0.601	0.604	0.601	0.566	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
HSTL_I_S	0.597	0.601	0.604	0.601	0.566	1.464	1.575	1.725	1.575	1.574	1.464	1.575	1.725	1.575	1.574	ns
HSUL_12_F	0.604	0.598	0.615	0.598	0.538	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns
HSUL_12_S	0.604	0.598	0.615	0.598	0.538	1.395	1.508	1.634	1.508	1.506	1.395	1.508	1.634	1.508	1.506	ns

Table 75: **IOB High Density (HD) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVCMOS12_F_12	0.515	0.558	0.618	0.558	0.568	1.465	1.574	1.733	1.574	1.566	1.465	1.574	1.733	1.574	1.566	ns
LVCMOS12_F_4	0.515	0.558	0.618	0.558	0.568	1.628	1.705	1.883	1.705	1.714	1.628	1.705	1.883	1.705	1.714	ns
LVCMOS12_F_8	0.515	0.558	0.618	0.558	0.568	1.480	1.540	1.690	1.540	1.533	1.480	1.540	1.690	1.540	1.533	ns
LVCMOS12_S_12	0.515	0.558	0.618	0.558	0.568	1.874	1.975	2.142	1.975	1.931	1.874	1.975	2.142	1.975	1.931	ns
LVCMOS12_S_4	0.515	0.558	0.618	0.558	0.568	1.935	1.959	2.162	1.959	1.949	1.935	1.959	2.162	1.959	1.949	ns
LVCMOS12_S_8	0.515	0.558	0.618	0.558	0.568	2.042	2.081	2.273	2.081	2.041	2.042	2.081	2.273	2.081	2.041	ns
LVCMOS15_F_12	0.468	0.513	0.588	0.513	0.530	1.374	1.422	1.573	1.422	1.439	1.374	1.422	1.573	1.422	1.439	ns
LVCMOS15_F_16	0.468	0.513	0.588	0.513	0.530	1.352	1.430	1.564	1.430	1.427	1.352	1.430	1.564	1.430	1.427	ns
LVCMOS15_F_4	0.468	0.513	0.588	0.513	0.530	1.539	1.626	1.747	1.626	1.636	1.539	1.626	1.747	1.626	1.636	ns
LVCMOS15_F_8	0.468	0.513	0.588	0.513	0.530	1.461	1.529	1.661	1.529	1.503	1.461	1.529	1.661	1.529	1.503	ns
LVCMOS15_S_12	0.468	0.513	0.588	0.513	0.530	1.778	1.859	1.999	1.859	1.823	1.778	1.859	1.999	1.859	1.823	ns
LVCMOS15_S_16	0.468	0.513	0.588	0.513	0.530	2.060	2.089	2.300	2.089	2.026	2.060	2.089	2.300	2.089	2.026	ns
LVCMOS15_S_4	0.468	0.513	0.588	0.513	0.530	2.160	2.204	2.368	2.204	2.115	2.160	2.204	2.368	2.204	2.115	ns
LVCMOS15_S_8	0.468	0.513	0.588	0.513	0.530	2.081	2.088	2.311	2.088	2.063	2.081	2.088	2.311	2.088	2.063	ns
LVCMOS18_F_12	0.437	0.502	0.512	0.502	0.497	1.393	1.487	1.618	1.487	1.460	1.393	1.487	1.618	1.487	1.460	ns
LVCMOS18_F_16	0.437	0.502	0.512	0.502	0.497	1.356	1.459	1.568	1.459	1.429	1.356	1.459	1.568	1.459	1.429	ns
LVCMOS18_F_4	0.437	0.502	0.512	0.502	0.497	1.572	1.650	1.780	1.650	1.634	1.572	1.650	1.780	1.650	1.634	ns
LVCMOS18_F_8	0.437	0.502	0.512	0.502	0.497	1.478	1.546	1.704	1.546	1.540	1.478	1.546	1.704	1.546	1.540	ns
LVCMOS18_S_12	0.437	0.502	0.512	0.502	0.497	1.993	2.038	2.232	2.038	1.999	1.993	2.038	2.232	2.038	1.999	ns
LVCMOS18_S_16	0.437	0.502	0.512	0.502	0.497	1.935	2.012	2.189	2.012	1.966	1.935	2.012	2.189	2.012	1.966	ns
LVCMOS18_S_4	0.437	0.502	0.512	0.502	0.497	2.123	2.154	2.358	2.154	2.100	2.123	2.154	2.358	2.154	2.100	ns
LVCMOS18_S_8	0.437	0.502	0.512	0.502	0.497	2.100	2.123	2.328	2.123	2.076	2.100	2.123	2.328	2.123	2.076	ns
LVCMOS25_F_12	0.516	0.542	0.588	0.542	0.539	1.961	2.012	2.296	2.012	2.001	1.961	2.012	2.296	2.012	2.001	ns
LVCMOS25_F_16	0.516	0.542	0.588	0.542	0.539	1.893	1.967	2.251	1.967	1.958	1.893	1.967	2.251	1.967	1.958	ns
LVCMOS25_F_4	0.516	0.542	0.588	0.542	0.539	2.100	2.213	2.413	2.213	2.155	2.100	2.213	2.413	2.213	2.155	ns
LVCMOS25_F_8	0.516	0.542	0.588	0.542	0.539	2.052	2.101	2.423	2.101	2.093	2.052	2.101	2.423	2.101	2.093	ns
LVCMOS25_S_12	0.516	0.542	0.588	0.542	0.539	2.455	2.589	2.878	2.589	2.501	2.455	2.589	2.878	2.589	2.501	ns
LVCMOS25_S_16	0.516	0.542	0.588	0.542	0.539	2.360	2.478	2.775	2.478	2.382	2.360	2.478	2.775	2.478	2.382	ns
LVCMOS25_S_4	0.516	0.542	0.588	0.542	0.539	2.622	2.723	3.016	2.723	2.630	2.622	2.723	3.016	2.723	2.630	ns
LVCMOS25_S_8	0.516	0.542	0.588	0.542	0.539	2.538	2.643	2.943	2.643	2.567	2.538	2.643	2.943	2.643	2.567	ns
LVCMOS33_F_12	0.577	0.622	0.675	0.622	0.624	1.942	2.047	2.248	2.047	2.024	1.942	2.047	2.248	2.047	2.024	ns
LVCMOS33_F_16	0.577	0.622	0.675	0.622	0.624	1.976	2.072	2.266	2.072	2.048	1.976	2.072	2.266	2.072	2.048	ns
LVCMOS33_F_4	0.577	0.622	0.675	0.622	0.624	1.925	2.049	2.232	2.049	2.019	1.925	2.049	2.232	2.049	2.019	ns
LVCMOS33_F_8	0.577	0.622	0.675	0.622	0.624	2.101	2.189	2.375	2.189	2.149	2.101	2.189	2.375	2.189	2.149	ns
LVCMOS33_S_12	0.577	0.622	0.675	0.622	0.624	2.450	2.533	2.856	2.533	2.515	2.450	2.533	2.856	2.533	2.515	ns
LVCMOS33_S_16	0.577	0.622	0.675	0.622	0.624	2.424	2.495	2.782	2.495	2.430	2.424	2.495	2.782	2.495	2.430	ns
LVCMOS33_S_4	0.577	0.622	0.675	0.622	0.624	2.632	2.684	2.991	2.684	2.613	2.632	2.684	2.991	2.684	2.613	ns
LVCMOS33_S_8	0.577	0.622	0.675	0.622	0.624	2.561	2.644	2.946	2.644	2.578	2.561	2.644	2.946	2.644	2.578	ns
LVDS_25	0.597	0.587	0.671	0.587	0.598	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	0.597	0.587	0.671	0.587	0.598	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	0.577	0.622	0.675	0.622	0.624	1.942	2.047	2.248	2.047	2.024	1.942	2.047	2.248	2.047	2.024	ns

Table 75: **IOB High Density (HD) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVTTL_F_16	0.577	0.622	0.675	0.622	0.624	1.994	2.144	2.379	2.144	2.081	1.994	2.144	2.379	2.144	2.081	ns
LVTTL_F_4	0.577	0.622	0.675	0.622	0.624	1.925	2.049	2.232	2.049	2.019	1.925	2.049	2.232	2.049	2.019	ns
LVTTL_F_8	0.577	0.622	0.675	0.622	0.624	2.093	2.190	2.365	2.190	2.144	2.093	2.190	2.365	2.190	2.144	ns
LVTTL_S_12	0.577	0.622	0.675	0.622	0.624	2.450	2.533	2.856	2.533	2.515	2.450	2.533	2.856	2.533	2.515	ns
LVTTL_S_16	0.577	0.622	0.675	0.622	0.624	2.424	2.495	2.782	2.495	2.430	2.424	2.495	2.782	2.495	2.430	ns
LVTTL_S_4	0.577	0.622	0.675	0.622	0.624	2.632	2.684	2.991	2.684	2.613	2.632	2.684	2.991	2.684	2.613	ns
LVTTL_S_8	0.577	0.622	0.675	0.622	0.624	2.561	2.644	2.946	2.644	2.578	2.561	2.644	2.946	2.644	2.578	ns
SLVS_400_25	0.597	0.587	0.671	0.587	0.598	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.604	0.598	0.615	0.598	0.538	1.463	1.561	1.704	1.561	1.555	1.463	1.561	1.704	1.561	1.555	ns
SSTL12_S	0.604	0.598	0.615	0.598	0.538	1.707	1.747	1.909	1.747	1.716	1.707	1.747	1.909	1.747	1.716	ns
SSTL135_F	0.605	0.598	0.642	0.598	0.552	1.473	1.590	1.728	1.59	1.585	1.473	1.590	1.728	1.590	1.585	ns
SSTL135_II_F	0.605	0.598	0.642	0.598	0.552	1.406	1.498	1.636	1.498	1.491	1.406	1.498	1.636	1.498	1.491	ns
SSTL135_II_S	0.605	0.598	0.642	0.598	0.552	1.576	1.649	1.789	1.649	1.618	1.576	1.649	1.789	1.649	1.618	ns
SSTL135_S	0.605	0.598	0.642	0.598	0.552	1.817	1.887	2.046	1.887	1.846	1.817	1.887	2.046	1.887	1.846	ns
SSTL15_F	0.597	0.601	0.604	0.601	0.566	1.474	1.592	1.734	1.592	1.597	1.474	1.592	1.734	1.592	1.597	ns
SSTL15_II_F	0.597	0.601	0.604	0.601	0.566	1.406	1.511	1.659	1.511	1.505	1.406	1.511	1.659	1.511	1.505	ns
SSTL15_II_S	0.597	0.601	0.604	0.601	0.566	1.618	1.700	1.856	1.700	1.668	1.618	1.700	1.856	1.700	1.668	ns
SSTL15_S	0.597	0.601	0.604	0.601	0.566	1.734	1.804	1.957	1.804	1.775	1.734	1.804	1.957	1.804	1.775	ns
SSTL18_II_F	0.596	0.606	0.668	0.606	0.571	1.357	1.473	1.604	1.473	1.469	1.357	1.473	1.604	1.473	1.469	ns
SSTL18_II_S	0.596	0.606	0.668	0.606	0.571	1.511	1.629	1.784	1.629	1.616	1.511	1.629	1.784	1.629	1.616	ns
SSTL18_I_F	0.596	0.606	0.668	0.606	0.571	1.335	1.431	1.563	1.431	1.429	1.335	1.431	1.563	1.431	1.429	ns
SSTL18_I_S	0.596	0.606	0.668	0.606	0.571	1.692	1.802	1.961	1.802	1.76	1.692	1.802	1.961	1.802	1.760	ns
SUB_LVDS	0.638	0.600	0.626	0.600	0.579	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Table 76: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_HSTL_I_12_M	0.277	0.335	0.342	0.335	0.321	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
DIFF_HSTL_I_12_S	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_HSTL_I_18_F	0.285	0.314	0.334	0.314	0.328	0.388	0.396	0.413	0.396	0.388	0.388	0.396	0.413	0.396	0.388	ns
DIFF_HSTL_I_18_M	0.285	0.314	0.334	0.314	0.328	0.388	0.393	0.413	0.393	0.389	0.388	0.393	0.413	0.393	0.389	ns
DIFF_HSTL_I_18_S	0.285	0.314	0.334	0.314	0.328	0.388	0.394	0.413	0.391	0.387	0.388	0.394	0.413	0.391	0.387	ns
DIFF_HSTL_I_DCI_12_F	0.277	0.335	0.342	0.335	0.321	0.422	0.420	0.444	0.421	0.414	0.422	0.420	0.444	0.421	0.414	ns
DIFF_HSTL_I_DCI_12_M	0.277	0.335	0.342	0.335	0.321	0.422	0.420	0.444	0.422	0.412	0.422	0.420	0.444	0.422	0.412	ns
DIFF_HSTL_I_DCI_12_S	0.277	0.335	0.342	0.335	0.321	0.422	0.421	0.442	0.421	0.412	0.422	0.421	0.442	0.421	0.412	ns
DIFF_HSTL_I_DCI_18_F	0.284	0.314	0.331	0.314	0.331	0.418	0.425	0.440	0.424	0.417	0.418	0.425	0.440	0.424	0.417	ns
DIFF_HSTL_I_DCI_18_M	0.284	0.314	0.331	0.314	0.331	0.418	0.424	0.443	0.423	0.416	0.418	0.424	0.443	0.423	0.416	ns
DIFF_HSTL_I_DCI_18_S	0.284	0.314	0.331	0.314	0.331	0.418	0.424	0.443	0.424	0.417	0.418	0.424	0.443	0.424	0.417	ns
DIFF_HSTL_I_DCI_F	0.294	0.313	0.330	0.313	0.320	0.420	0.423	0.438	0.421	0.415	0.420	0.423	0.438	0.421	0.415	ns
DIFF_HSTL_I_DCI_M	0.294	0.313	0.330	0.313	0.320	0.420	0.423	0.440	0.423	0.416	0.420	0.423	0.440	0.423	0.416	ns
DIFF_HSTL_I_DCI_S	0.294	0.313	0.330	0.313	0.320	0.420	0.421	0.440	0.417	0.414	0.420	0.421	0.440	0.417	0.414	ns
DIFF_HSTL_I_F	0.295	0.330	0.341	0.330	0.320	0.393	0.391	0.411	0.394	0.385	0.393	0.391	0.411	0.394	0.385	ns
DIFF_HSTL_I_M	0.295	0.330	0.341	0.330	0.320	0.392	0.393	0.413	0.397	0.386	0.392	0.393	0.413	0.397	0.386	ns
DIFF_HSTL_I_S	0.295	0.330	0.341	0.330	0.320	0.393	0.393	0.413	0.394	0.384	0.393	0.393	0.413	0.394	0.384	ns
DIFF_HSUL_12_DCI_F	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_HSUL_12_DCI_M	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_HSUL_12_DCI_S	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_HSUL_12_F	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_HSUL_12_M	0.277	0.335	0.342	0.335	0.321	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
DIFF_HSUL_12_S	0.277	0.335	0.342	0.335	0.321	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
DIFF_POD10_DCI_F	0.286	0.325	0.340	0.325	0.334	0.438	0.431	0.451	0.431	0.418	0.438	0.431	0.451	0.431	0.418	ns
DIFF_POD10_DCI_M	0.286	0.325	0.340	0.325	0.334	0.592	0.627	0.660	0.627	0.622	0.592	0.627	0.660	0.627	0.622	ns
DIFF_POD10_DCI_S	0.286	0.325	0.340	0.325	0.334	0.823	0.900	0.974	0.900	0.888	0.823	0.900	0.974	0.900	0.888	ns
DIFF_POD10_F	0.277	0.314	0.331	0.314	0.317	0.412	0.406	0.426	0.406	0.392	0.412	0.406	0.426	0.406	0.392	ns
DIFF_POD10_M	0.277	0.314	0.331	0.314	0.317	0.570	0.593	0.627	0.593	0.588	0.570	0.593	0.627	0.593	0.588	ns
DIFF_POD10_S	0.277	0.314	0.331	0.314	0.317	0.800	0.853	0.914	0.853	0.835	0.800	0.853	0.914	0.853	0.835	ns
DIFF_POD12_DCI_F	0.275	0.314	0.333	0.314	0.318	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_POD12_DCI_M	0.275	0.314	0.333	0.314	0.318	0.586	0.628	0.662	0.628	0.623	0.586	0.628	0.662	0.628	0.623	ns
DIFF_POD12_DCI_S	0.275	0.314	0.333	0.314	0.318	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
DIFF_POD12_F	0.275	0.323	0.341	0.323	0.316	0.402	0.396	0.414	0.395	0.383	0.402	0.396	0.414	0.395	0.383	ns
DIFF_POD12_M	0.275	0.323	0.341	0.323	0.316	0.562	0.595	0.629	0.595	0.589	0.562	0.595	0.629	0.595	0.589	ns
DIFF_POD12_S	0.275	0.323	0.341	0.323	0.316	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
DIFF_SSTL12_DCI_F	0.283	0.327	0.344	0.327	0.317	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
DIFF_SSTL12_DCI_M	0.283	0.327	0.344	0.327	0.317	0.584	0.630	0.664	0.628	0.624	0.584	0.630	0.664	0.628	0.624	ns
DIFF_SSTL12_DCI_S	0.283	0.327	0.344	0.327	0.317	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
DIFF_SSTL12_F	0.277	0.335	0.342	0.335	0.321	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
DIFF_SSTL12_M	0.277	0.335	0.342	0.335	0.321	0.561	0.597	0.631	0.597	0.591	0.561	0.597	0.631	0.597	0.591	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_S	0.277	0.335	0.342	0.335	0.321	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
DIFF_SSTL135_DCI_F	0.278	0.312	0.339	0.312	0.319	0.426	0.420	0.439	0.422	0.414	0.426	0.420	0.439	0.422	0.414	ns
DIFF_SSTL135_DCI_M	0.278	0.312	0.339	0.312	0.319	0.586	0.630	0.666	0.630	0.626	0.586	0.630	0.666	0.630	0.626	ns
DIFF_SSTL135_DCI_S	0.278	0.312	0.339	0.312	0.319	0.814	0.902	0.966	0.895	0.896	0.814	0.902	0.966	0.895	0.896	ns
DIFF_SSTL135_F	0.289	0.313	0.336	0.313	0.315	0.397	0.392	0.412	0.394	0.385	0.397	0.392	0.412	0.394	0.385	ns
DIFF_SSTL135_M	0.289	0.313	0.336	0.313	0.315	0.565	0.599	0.633	0.598	0.593	0.565	0.599	0.633	0.598	0.593	ns
DIFF_SSTL135_S	0.289	0.313	0.336	0.313	0.315	0.789	0.850	0.907	0.849	0.841	0.789	0.850	0.907	0.849	0.841	ns
DIFF_SSTL15_DCI_F	0.294	0.313	0.330	0.313	0.320	0.424	0.421	0.439	0.423	0.422	0.424	0.421	0.439	0.423	0.422	ns
DIFF_SSTL15_DCI_M	0.294	0.313	0.330	0.313	0.320	0.591	0.632	0.667	0.632	0.627	0.591	0.632	0.667	0.632	0.627	ns
DIFF_SSTL15_DCI_S	0.294	0.313	0.330	0.313	0.320	0.816	0.906	0.971	0.906	0.898	0.816	0.906	0.971	0.906	0.898	ns
DIFF_SSTL15_F	0.295	0.330	0.341	0.330	0.320	0.393	0.392	0.412	0.392	0.386	0.393	0.392	0.412	0.392	0.386	ns
DIFF_SSTL15_M	0.295	0.330	0.341	0.330	0.320	0.564	0.598	0.633	0.598	0.592	0.564	0.598	0.633	0.598	0.592	ns
DIFF_SSTL15_S	0.295	0.330	0.341	0.330	0.320	0.790	0.853	0.910	0.850	0.844	0.790	0.853	0.910	0.850	0.844	ns
DIFF_SSTL18_I_DCI_F	0.284	0.314	0.331	0.314	0.331	0.418	0.425	0.440	0.424	0.416	0.418	0.425	0.440	0.424	0.416	ns
DIFF_SSTL18_I_DCI_M	0.284	0.314	0.331	0.314	0.331	0.593	0.633	0.670	0.634	0.629	0.593	0.633	0.670	0.634	0.629	ns
DIFF_SSTL18_I_DCI_S	0.284	0.314	0.331	0.314	0.331	0.821	0.910	0.978	0.911	0.903	0.821	0.910	0.978	0.911	0.903	ns
DIFF_SSTL18_I_F	0.285	0.314	0.334	0.314	0.328	0.388	0.395	0.415	0.392	0.387	0.388	0.395	0.415	0.392	0.387	ns
DIFF_SSTL18_I_M	0.285	0.314	0.334	0.314	0.328	0.567	0.603	0.638	0.603	0.596	0.567	0.603	0.638	0.603	0.596	ns
DIFF_SSTL18_I_S	0.285	0.314	0.334	0.314	0.328	0.794	0.861	0.920	0.860	0.851	0.794	0.861	0.920	0.860	0.851	ns
HSLVDCI_15_F	0.343	0.364	0.384	0.364	0.360	0.424	0.422	0.440	0.421	0.418	0.424	0.422	0.440	0.421	0.418	ns
HSLVDCI_15_M	0.343	0.364	0.384	0.364	0.360	0.424	0.420	0.441	0.424	0.413	0.424	0.420	0.441	0.424	0.413	ns
HSLVDCI_15_S	0.343	0.364	0.384	0.364	0.360	0.424	0.421	0.440	0.421	0.417	0.424	0.421	0.440	0.421	0.417	ns
HSLVDCI_18_F	0.343	0.365	0.386	0.365	0.361	0.420	0.425	0.440	0.424	0.416	0.420	0.425	0.440	0.424	0.416	ns
HSLVDCI_18_M	0.343	0.365	0.386	0.365	0.361	0.423	0.424	0.440	0.423	0.418	0.423	0.424	0.440	0.423	0.418	ns
HSLVDCI_18_S	0.343	0.365	0.386	0.365	0.361	0.420	0.423	0.443	0.425	0.414	0.420	0.423	0.443	0.425	0.414	ns
HSTL_I_12_F	0.342	0.363	0.384	0.363	0.360	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
HSTL_I_12_M	0.342	0.363	0.384	0.363	0.360	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
HSTL_I_12_S	0.342	0.363	0.384	0.363	0.360	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
HSTL_I_18_F	0.343	0.365	0.386	0.365	0.361	0.388	0.396	0.413	0.396	0.388	0.388	0.396	0.413	0.396	0.388	ns
HSTL_I_18_M	0.343	0.365	0.386	0.365	0.361	0.388	0.393	0.413	0.393	0.389	0.388	0.393	0.413	0.393	0.389	ns
HSTL_I_18_S	0.343	0.365	0.386	0.365	0.361	0.388	0.394	0.413	0.391	0.387	0.388	0.394	0.413	0.391	0.387	ns
HSTL_I_DCI_12_F	0.342	0.363	0.384	0.363	0.360	0.422	0.420	0.444	0.421	0.414	0.422	0.420	0.444	0.421	0.414	ns
HSTL_I_DCI_12_M	0.342	0.363	0.384	0.363	0.360	0.422	0.420	0.444	0.422	0.412	0.422	0.420	0.444	0.422	0.412	ns
HSTL_I_DCI_12_S	0.342	0.363	0.384	0.363	0.360	0.422	0.421	0.442	0.421	0.412	0.422	0.421	0.442	0.421	0.412	ns
HSTL_I_DCI_18_F	0.343	0.365	0.386	0.365	0.361	0.418	0.425	0.440	0.424	0.417	0.418	0.425	0.440	0.424	0.417	ns
HSTL_I_DCI_18_M	0.343	0.365	0.386	0.365	0.361	0.418	0.424	0.443	0.423	0.416	0.418	0.424	0.443	0.423	0.416	ns
HSTL_I_DCI_18_S	0.343	0.365	0.386	0.365	0.361	0.418	0.424	0.443	0.424	0.417	0.418	0.424	0.443	0.424	0.417	ns
HSTL_I_DCI_F	0.343	0.364	0.384	0.364	0.360	0.420	0.423	0.438	0.421	0.415	0.420	0.423	0.438	0.421	0.415	ns
HSTL_I_DCI_M	0.343	0.364	0.384	0.364	0.360	0.420	0.423	0.440	0.423	0.416	0.420	0.423	0.440	0.423	0.416	ns
HSTL_I_DCI_S	0.343	0.364	0.384	0.364	0.360	0.420	0.421	0.440	0.417	0.414	0.420	0.421	0.440	0.417	0.414	ns
HSTL_I_F	0.342	0.363	0.384	0.363	0.360	0.393	0.391	0.411	0.394	0.385	0.393	0.391	0.411	0.394	0.385	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_M	0.342	0.363	0.384	0.363	0.360	0.392	0.393	0.413	0.397	0.386	0.392	0.393	0.413	0.397	0.386	ns
HSTL_I_S	0.342	0.363	0.384	0.363	0.360	0.393	0.393	0.413	0.394	0.384	0.393	0.393	0.413	0.394	0.384	ns
HSUL_12_DCI_F	0.343	0.363	0.384	0.363	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
HSUL_12_DCI_M	0.343	0.363	0.384	0.363	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
HSUL_12_DCI_S	0.343	0.363	0.384	0.363	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
HSUL_12_F	0.342	0.363	0.384	0.363	0.360	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
HSUL_12_M	0.342	0.363	0.384	0.363	0.360	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
HSUL_12_S	0.342	0.363	0.384	0.363	0.360	0.402	0.395	0.414	0.395	0.383	0.402	0.395	0.414	0.395	0.383	ns
LVCMOS12_F_2	0.476	0.552	0.600	0.552	0.557	0.865	0.841	0.867	0.839	0.820	0.865	0.841	0.867	0.839	0.820	ns
LVCMOS12_F_4	0.476	0.552	0.600	0.552	0.557	0.640	0.642	0.665	0.635	0.624	0.640	0.642	0.665	0.635	0.624	ns
LVCMOS12_F_6	0.476	0.552	0.600	0.552	0.557	0.533	0.515	0.540	0.515	0.502	0.533	0.515	0.540	0.515	0.502	ns
LVCMOS12_F_8	0.476	0.552	0.600	0.552	0.557	0.476	0.472	0.498	0.477	0.461	0.476	0.472	0.498	0.477	0.461	ns
LVCMOS12_M_2	0.476	0.552	0.600	0.552	0.557	0.904	0.899	0.923	0.893	0.881	0.904	0.899	0.923	0.893	0.881	ns
LVCMOS12_M_4	0.476	0.552	0.600	0.552	0.557	0.740	0.741	0.773	0.741	0.733	0.740	0.741	0.773	0.741	0.733	ns
LVCMOS12_M_6	0.476	0.552	0.600	0.552	0.557	0.634	0.655	0.690	0.657	0.648	0.634	0.655	0.690	0.657	0.648	ns
LVCMOS12_M_8	0.476	0.552	0.600	0.552	0.557	0.633	0.672	0.712	0.672	0.665	0.633	0.672	0.712	0.672	0.665	ns
LVCMOS12_S_2	0.476	0.552	0.600	0.552	0.557	0.974	0.976	1.022	0.976	0.963	0.974	0.976	1.022	0.976	0.963	ns
LVCMOS12_S_4	0.476	0.552	0.600	0.552	0.557	0.861	0.902	0.956	0.902	0.888	0.861	0.902	0.956	0.902	0.888	ns
LVCMOS12_S_6	0.476	0.552	0.600	0.552	0.557	0.821	0.890	0.943	0.890	0.876	0.821	0.890	0.943	0.890	0.876	ns
LVCMOS12_S_8	0.476	0.552	0.600	0.552	0.557	0.871	0.947	1.020	0.947	0.939	0.871	0.947	1.020	0.947	0.939	ns
LVCMOS15_F_12	0.395	0.443	0.478	0.443	0.439	0.422	0.417	0.436	0.417	0.408	0.422	0.417	0.436	0.417	0.408	ns
LVCMOS15_F_2	0.395	0.443	0.478	0.443	0.439	0.847	0.837	0.861	0.832	0.819	0.847	0.837	0.861	0.832	0.819	ns
LVCMOS15_F_4	0.395	0.443	0.478	0.443	0.439	0.637	0.633	0.658	0.633	0.621	0.637	0.633	0.658	0.633	0.621	ns
LVCMOS15_F_6	0.395	0.443	0.478	0.443	0.439	0.517	0.511	0.532	0.511	0.501	0.517	0.511	0.532	0.511	0.501	ns
LVCMOS15_F_8	0.395	0.443	0.478	0.443	0.439	0.472	0.469	0.488	0.468	0.457	0.472	0.469	0.488	0.468	0.457	ns
LVCMOS15_M_12	0.395	0.443	0.478	0.443	0.439	0.669	0.73	0.775	0.73	0.723	0.669	0.73	0.775	0.73	0.723	ns
LVCMOS15_M_2	0.395	0.443	0.478	0.443	0.439	0.898	0.895	0.93	0.895	0.883	0.898	0.895	0.93	0.895	0.883	ns
LVCMOS15_M_4	0.395	0.443	0.478	0.443	0.439	0.726	0.743	0.774	0.743	0.731	0.726	0.743	0.774	0.743	0.731	ns
LVCMOS15_M_6	0.395	0.443	0.478	0.443	0.439	0.633	0.658	0.691	0.659	0.642	0.633	0.658	0.691	0.659	0.642	ns
LVCMOS15_M_8	0.395	0.443	0.478	0.443	0.439	0.635	0.673	0.714	0.673	0.669	0.635	0.673	0.714	0.673	0.669	ns
LVCMOS15_S_12	0.395	0.443	0.478	0.443	0.439	1.002	1.119	1.216	1.122	1.112	1.002	1.119	1.216	1.122	1.112	ns
LVCMOS15_S_2	0.395	0.443	0.478	0.443	0.439	0.967	0.979	1.022	0.977	0.965	0.967	0.979	1.022	0.977	0.965	ns
LVCMOS15_S_4	0.395	0.443	0.478	0.443	0.439	0.861	0.907	0.959	0.907	0.894	0.861	0.907	0.959	0.907	0.894	ns
LVCMOS15_S_6	0.395	0.443	0.478	0.443	0.439	0.825	0.898	0.950	0.898	0.885	0.825	0.898	0.950	0.898	0.885	ns
LVCMOS15_S_8	0.395	0.443	0.478	0.443	0.439	0.871	0.955	1.026	0.953	0.943	0.871	0.955	1.026	0.953	0.943	ns
LVCMOS18_F_12	0.352	0.388	0.414	0.388	0.377	0.412	0.418	0.440	0.418	0.410	0.412	0.418	0.440	0.418	0.410	ns
LVCMOS18_F_2	0.352	0.388	0.414	0.388	0.377	0.850	0.841	0.865	0.841	0.828	0.850	0.841	0.865	0.841	0.828	ns
LVCMOS18_F_4	0.352	0.388	0.414	0.388	0.377	0.643	0.637	0.660	0.637	0.624	0.643	0.637	0.660	0.637	0.624	ns
LVCMOS18_F_6	0.352	0.388	0.414	0.388	0.377	0.507	0.506	0.532	0.506	0.501	0.507	0.506	0.532	0.506	0.501	ns
LVCMOS18_F_8	0.352	0.388	0.414	0.388	0.377	0.468	0.468	0.491	0.468	0.459	0.468	0.468	0.491	0.468	0.459	ns
LVCMOS18_M_12	0.352	0.388	0.414	0.388	0.377	0.681	0.734	0.779	0.734	0.727	0.681	0.734	0.779	0.734	0.727	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVCMOS18_M_2	0.352	0.388	0.414	0.388	0.377	0.902	0.899	0.927	0.899	0.884	0.902	0.899	0.927	0.899	0.884	ns
LVCMOS18_M_4	0.352	0.388	0.414	0.388	0.377	0.731	0.745	0.778	0.745	0.731	0.731	0.745	0.778	0.745	0.731	ns
LVCMOS18_M_6	0.352	0.388	0.414	0.388	0.377	0.638	0.659	0.696	0.664	0.653	0.638	0.659	0.696	0.664	0.653	ns
LVCMOS18_M_8	0.352	0.388	0.414	0.388	0.377	0.632	0.678	0.717	0.678	0.667	0.632	0.678	0.717	0.678	0.667	ns
LVCMOS18_S_12	0.352	0.388	0.414	0.388	0.377	1.015	1.130	1.224	1.130	1.119	1.015	1.130	1.224	1.130	1.119	ns
LVCMOS18_S_2	0.352	0.388	0.414	0.388	0.377	0.967	0.983	1.024	0.984	0.967	0.967	0.983	1.024	0.984	0.967	ns
LVCMOS18_S_4	0.352	0.388	0.414	0.388	0.377	0.864	0.910	0.964	0.910	0.897	0.864	0.910	0.964	0.910	0.897	ns
LVCMOS18_S_6	0.352	0.388	0.414	0.388	0.377	0.836	0.900	0.957	0.900	0.888	0.836	0.900	0.957	0.900	0.888	ns
LVCMOS18_S_8	0.352	0.388	0.414	0.388	0.377	0.881	0.959	1.033	0.959	0.948	0.881	0.959	1.033	0.959	0.948	ns
LVDCI_15_F	0.392	0.436	0.476	0.436	0.437	0.424	0.422	0.441	0.418	0.415	0.424	0.422	0.441	0.418	0.415	ns
LVDCI_15_M	0.392	0.436	0.476	0.436	0.437	0.591	0.632	0.666	0.632	0.628	0.591	0.632	0.666	0.632	0.628	ns
LVDCI_15_S	0.392	0.436	0.476	0.436	0.437	0.815	0.906	0.972	0.905	0.898	0.815	0.906	0.972	0.905	0.898	ns
LVDCI_18_F	0.346	0.376	0.407	0.376	0.374	0.418	0.425	0.443	0.425	0.418	0.418	0.425	0.443	0.425	0.418	ns
LVDCI_18_M	0.346	0.376	0.407	0.376	0.374	0.594	0.633	0.670	0.633	0.628	0.594	0.633	0.670	0.633	0.628	ns
LVDCI_18_S	0.346	0.376	0.407	0.376	0.374	0.821	0.908	0.978	0.908	0.902	0.821	0.908	0.978	0.908	0.902	ns
LVDS	0.315	0.352	0.406	0.352	0.348	0.392	0.404	0.425	0.404	0.396	0.392	0.404	0.425	0.404	0.396	ns
MIPI_DPHY_DCI_HS	0.305	0.317	0.342	0.317	0.319	0.429	0.434	0.452	0.434	0.427	N/A	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.477	8.423	8.777	8.415	8.698	1.627	1.604	1.642	1.604	1.583	N/A	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.342	0.363	0.384	0.363	0.360	0.438	0.431	0.451	0.431	0.418	0.438	0.431	0.451	0.431	0.418	ns
POD10_DCI_M	0.342	0.363	0.384	0.363	0.360	0.592	0.627	0.660	0.627	0.622	0.592	0.627	0.660	0.627	0.622	ns
POD10_DCI_S	0.342	0.363	0.384	0.363	0.360	0.823	0.900	0.974	0.900	0.888	0.823	0.900	0.974	0.900	0.888	ns
POD10_F	0.343	0.363	0.384	0.363	0.360	0.412	0.406	0.426	0.406	0.392	0.412	0.406	0.426	0.406	0.392	ns
POD10_M	0.343	0.363	0.384	0.363	0.360	0.570	0.593	0.627	0.593	0.588	0.570	0.593	0.627	0.593	0.588	ns
POD10_S	0.343	0.363	0.384	0.363	0.360	0.800	0.853	0.914	0.853	0.835	0.800	0.853	0.914	0.853	0.835	ns
POD12_DCI_F	0.343	0.364	0.386	0.364	0.360	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
POD12_DCI_M	0.343	0.364	0.386	0.364	0.360	0.586	0.628	0.662	0.628	0.623	0.586	0.628	0.662	0.628	0.623	ns
POD12_DCI_S	0.343	0.364	0.386	0.364	0.360	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
POD12_F	0.343	0.364	0.386	0.364	0.360	0.402	0.396	0.414	0.395	0.383	0.402	0.396	0.414	0.395	0.383	ns
POD12_M	0.343	0.364	0.386	0.364	0.360	0.562	0.595	0.629	0.595	0.589	0.562	0.595	0.629	0.595	0.589	ns
POD12_S	0.343	0.364	0.386	0.364	0.360	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
SLVS_400_18	0.315	0.352	0.406	0.352	0.348	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.331	0.366	0.384	0.366	0.350	0.428	0.421	0.440	0.421	0.412	0.428	0.421	0.440	0.421	0.412	ns
SSTL12_DCI_M	0.331	0.366	0.384	0.366	0.350	0.584	0.630	0.664	0.628	0.624	0.584	0.630	0.664	0.628	0.624	ns
SSTL12_DCI_S	0.331	0.366	0.384	0.366	0.350	0.813	0.899	0.959	0.899	0.892	0.813	0.899	0.959	0.899	0.892	ns
SSTL12_F	0.333	0.377	0.375	0.377	0.343	0.402	0.396	0.414	0.396	0.383	0.402	0.396	0.414	0.396	0.383	ns
SSTL12_M	0.333	0.377	0.375	0.377	0.343	0.561	0.597	0.631	0.597	0.591	0.561	0.597	0.631	0.597	0.591	ns
SSTL12_S	0.333	0.377	0.375	0.377	0.343	0.789	0.844	0.899	0.844	0.835	0.789	0.844	0.899	0.844	0.835	ns
SSTL135_DCI_F	0.341	0.351	0.384	0.351	0.367	0.426	0.420	0.439	0.422	0.414	0.426	0.420	0.439	0.422	0.414	ns
SSTL135_DCI_M	0.341	0.351	0.384	0.351	0.367	0.586	0.630	0.666	0.630	0.626	0.586	0.630	0.666	0.630	0.626	ns
SSTL135_DCI_S	0.341	0.351	0.384	0.351	0.367	0.814	0.902	0.966	0.895	0.896	0.814	0.902	0.966	0.895	0.896	ns
SSTL135_F	0.331	0.352	0.373	0.352	0.356	0.397	0.392	0.412	0.394	0.385	0.397	0.392	0.412	0.394	0.385	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_M	0.331	0.352	0.373	0.352	0.356	0.565	0.599	0.633	0.598	0.593	0.565	0.599	0.633	0.598	0.593	ns
SSTL135_S	0.331	0.352	0.373	0.352	0.356	0.789	0.850	0.907	0.849	0.841	0.789	0.850	0.907	0.849	0.841	ns
SSTL15_DCI_F	0.332	0.349	0.362	0.349	0.346	0.424	0.421	0.439	0.423	0.422	0.424	0.421	0.439	0.423	0.422	ns
SSTL15_DCI_M	0.332	0.349	0.362	0.349	0.346	0.591	0.632	0.667	0.632	0.627	0.591	0.632	0.667	0.632	0.627	ns
SSTL15_DCI_S	0.332	0.349	0.362	0.349	0.346	0.816	0.906	0.971	0.906	0.898	0.816	0.906	0.971	0.906	0.898	ns
SSTL15_F	0.32	0.356	0.385	0.356	0.353	0.393	0.392	0.412	0.392	0.386	0.393	0.392	0.412	0.392	0.386	ns
SSTL15_M	0.32	0.356	0.385	0.356	0.353	0.564	0.598	0.633	0.598	0.592	0.564	0.598	0.633	0.598	0.592	ns
SSTL15_S	0.32	0.356	0.385	0.356	0.353	0.790	0.853	0.910	0.85	0.844	0.790	0.853	0.910	0.85	0.844	ns
SSTL18_I_DCI_F	0.333	0.353	0.360	0.353	0.347	0.418	0.425	0.440	0.424	0.416	0.418	0.425	0.440	0.424	0.416	ns
SSTL18_I_DCI_M	0.333	0.353	0.360	0.353	0.347	0.593	0.633	0.670	0.634	0.629	0.593	0.633	0.670	0.634	0.629	ns
SSTL18_I_DCI_S	0.333	0.353	0.360	0.353	0.347	0.821	0.910	0.978	0.911	0.903	0.821	0.910	0.978	0.911	0.903	ns
SSTL18_I_F	0.323	0.355	0.378	0.355	0.364	0.388	0.395	0.415	0.392	0.387	0.388	0.395	0.415	0.392	0.387	ns
SSTL18_I_M	0.323	0.355	0.378	0.355	0.364	0.567	0.603	0.638	0.603	0.596	0.567	0.603	0.638	0.603	0.596	ns
SSTL18_I_S	0.323	0.355	0.378	0.355	0.364	0.794	0.861	0.920	0.860	0.851	0.794	0.861	0.920	0.860	0.851	ns
SUB_LVDS	0.315	0.352	0.406	0.352	0.348	0.387	0.398	0.418	0.398	0.390	0.387	0.398	0.418	0.398	0.390	ns

Table 77 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 77: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for HD I/O banks						ns
	T input to pad high-impedance for HP I/O banks						ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks						ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks						ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 78 shows the test setup parameters used for measuring input delay.

Table 78: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	V_{REF} – 0.575	V_{REF} + 0.575	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.6	V_{REF} + 0.6	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.74	V_{REF} + 0.74	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.125	0.75 + 0.125	0 (6)	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.125	0.9 + 0.125	0 (6)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.125	0.675 + 0.125	0 (6)	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.125	0.75 + 0.125	0 (6)	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.125	0.9 + 0.125	0 (6)	–
DIFF_POD10, 1.0V	DIFF_POD10	0.7 – 0.125	0.7 + 0.125	0 (6)	–
DIFF_POD12, 1.2V	DIFF_POD12	0.84 – 0.125	0.84 + 0.125	0 (6)	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0 (6)	–

Table 78: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVDS_25, 2.5V	LVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 17.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 17 and Figure 18.

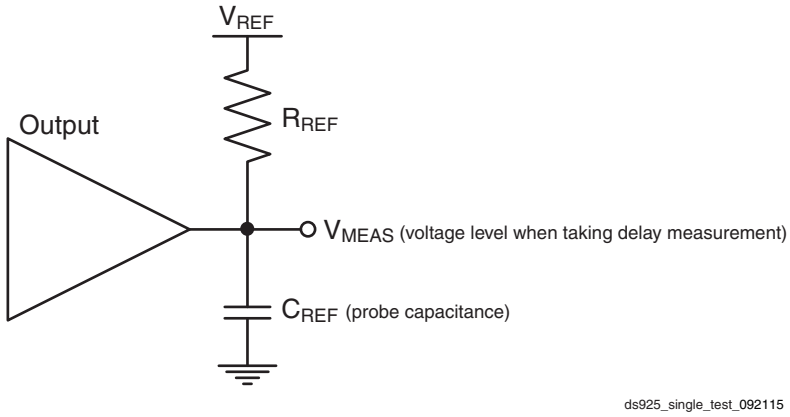

Figure 17: **Single-Ended Test Setup**

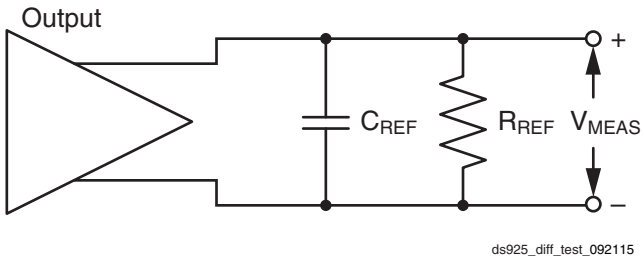

Figure 18: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 79.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 79: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V_{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V_{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V_{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 80: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	737	645	585	516	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	825	737	645	585	516	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	737	645	585	516	MHz
T_{PW}[(1)]	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T_{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.92	1.03	1.11	1.46	1.54	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register).	0.27	0.29	0.31	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoC that include this memory.

Table 81: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F_{MAX}	UltraRAM maximum frequency with OREG_B.	650	600	600	500	500	MHz
F_{MAX_ECC}	UltraRAM maximum frequency without OREG_B and EN_ECC_RD_B = True.	450	400	400	325	325	MHz
$F_{MAX\_NORPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	500	425	425	MHz
T_{PW} (1)	Minimum pulse width.	650	700	700	800	800	ps
T_{RSTPW}	Asynchronous reset minimum pulse width.	550	600	600	650	650	ps

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 82: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{REFCLK}	REFCLK frequency (component mode).	200 to 800					MHz
	REFCLK frequency (native mode).	200 to 2400	200 to 2400	200 to 2133			MHz
T_{MINPER_RST}	Minimum reset pulse width.	52.00					ns
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution.	2.5 to 15					ps

DSP48 Slice Switching Characteristics

Table 83: **DSP48 Slice Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F_{MAX}	With all registers used.	891	775	645	644	600	MHz
F_{MAX_PATDET}	With pattern detector.	794	687	571	562	524	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG.	635	544	456	440	413	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect.	577	492	410	395	371	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG.	655	565	468	453	423	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG).	483	410	338	323	304	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	280	MHz

Clock Buffers and Networks

Table 84: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)							
F_{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)							
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)							
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)							
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)							
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	512	MHz

MMCM Switching Characteristics

Table 85: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$MMCM\_F_{INMAX}$	Maximum input clock frequency.	1066	933	800	933	800	MHz
$MMCM\_F_{INMIN}$	Minimum input clock frequency.	10	10	10	10	10	MHz
$MMCM\_F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
$MMCM\_F_{INDUTY}$	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
$MMCM\_F_{MIN\_PSCLK}$	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	0.12	ns
$MMCM\_T_{OUTJITTER}$	MMCM output jitter.	Note 3					
$MMCM\_T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	0.20	ns
$MMCM\_T_{LOCKMAX}$	MMCM maximum lock time for $MMCM\_F_{PFDMIN}$.	100	100	100	100	100	µs
$MMCM\_F_{OUTMAX}$	MMCM maximum output frequency.	891	775	667	725	667	MHz
$MMCM\_F_{OUTMIN}$	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	6.25	MHz
$MMCM\_T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
$MMCM\_RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
$MMCM\_F_{PFDMAX}$	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
$MMCM\_F_{PFDMIN}$	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
$MMCM\_T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 86: **PLL Specification(1)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PLL_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	70	70	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	1500	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3					
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision.(4)	0.165	0.20	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time.	100					µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	2133	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.(5)	5.86	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500, 1 x VCO mode: 750 0.5 x VCO mode: 375					MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical.	14	14	14	14	14	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 87 through Table 89 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.								
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region).	XCZU2EG	4.40	4.82	5.22	5.67	5.97	ns
		XCZU3EG	4.40	4.82	5.22	5.67	5.97	ns
		XCZU4EV						ns
		XCZU5EV						ns
		XCZU6EG	5.42	5.76	6.16	7.10	7.16	ns
		XCZU7EV						ns
		XCZU9EG	5.42	5.76	6.16	7.10	7.16	ns
		XCZU11EG						ns
		XCZU15EG	5.49	6.05	6.57	7.28	7.82	ns
		XCZU17EG						ns
		XCZU19EG						ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 88: **Global Clock Input to Output Delay Without MMCM (Far Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.								
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM (far clock region).	XCZU2EG	4.69	5.16	5.61	6.13	6.49	ns
		XCZU3EG	4.69	5.16	5.61	6.13	6.49	ns
		XCZU4EV						ns
		XCZU5EV						ns
		XCZU6EG	5.62	5.98	6.38	7.39	7.46	ns
		XCZU7EV						ns
		XCZU9EG	5.62	5.98	6.38	7.39	7.46	ns
		XCZU11EG						ns
		XCZU15EG	5.69	6.30	6.83	7.60	8.17	ns
		XCZU17EG						ns
		XCZU19EG						ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 89: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.								
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM.	XCZU2EG	2.65	2.72	2.94	3.25	3.32	ns
		XCZU3EG	2.65	2.72	2.94	3.25	3.32	ns
		XCZU4EV						ns
		XCZU5EV						ns
		XCZU6EG	2.75	2.82	3.01	3.49	3.49	ns
		XCZU7EV						ns
		XCZU9EG	2.75	2.82	3.01	3.49	3.49	ns
		XCZU11EG						ns
		XCZU15EG	2.77	2.82	3.08	3.43	3.53	ns
		XCZU17EG						ns
		XCZU19EG						ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 90 and Table 91 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: **Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T_{PSFD_ZU2EG}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2EG	–0.67	–0.67	–0.67	–0.80	–0.80	ns
T_{PHFD_ZU2EG}		Hold		1.76	1.97	2.09	2.54	2.76	ns
T_{PSFD_ZU3EG}		Setup	XCZU3EG	–0.67	–0.67	–0.67	–0.80	–0.80	ns
T_{PHFD_ZU3EG}		Hold		1.76	1.97	2.09	2.54	2.76	ns
T_{PSFD_ZU4EV}		Setup	XCZU4EV						ns
T_{PHFD_ZU4EV}		Hold							ns
T_{PSFD_ZU5EV}		Setup	XCZU5EV						ns
T_{PHFD_ZU5EV}		Hold							ns
T_{PSFD_ZU6EG}		Setup	XCZU6EG	–1.06	–1.06	–1.06	–1.06	–1.06	ns
T_{PHFD_ZU6EG}		Hold		2.40	2.59	2.71	3.47	3.54	ns
T_{PSFD_ZU7EV}		Setup	XCZU7EV						ns
T_{PHFD_ZU7EV}		Hold							ns
T_{PSFD_ZU9EG}		Setup	XCZU9EG	–1.06	–1.06	–1.06	–1.06	–1.06	ns
T_{PHFD_ZU9EG}		Hold		2.40	2.59	2.71	3.47	3.54	ns
T_{PSFD_ZU11EG}		Setup	XCZU11EG						ns
T_{PHFD_ZU11EG}		Hold							ns
T_{PSFD_ZU15EG}		Setup	XCZU15EG	–1.07	–1.07	–1.07	–1.24	–1.24	ns
T_{PHFD_ZU15EG}		Hold		2.39	2.74	2.94	3.53	3.91	ns
T_{PSFD_ZU17EG}		Setup	XCZU17EG						ns
T_{PHFD_ZU17EG}		Hold							ns
T_{PSFD_ZU19EG}		Setup	XCZU19EG						ns
T_{PHFD_ZU19EG}		Hold							ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 91: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
$T_{PSMMCMCC\_ZU2EG}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2EG	1.71	1.98	2.16	2.16	2.16	ns
$T_{PHMMCMCC\_ZU2EG}$		Hold		0.33	0.33	0.33	0.45	0.45	ns
$T_{PSMMCMCC\_ZU3EG}$		Setup	XCZU3EG	1.71	1.98	2.16	2.16	2.16	ns
$T_{PHMMCMCC\_ZU3EG}$		Hold		0.33	0.33	0.33	0.45	0.45	ns
$T_{PSMMCMCC\_ZU4EV}$		Setup	XCZU4EV						ns
$T_{PHMMCMCC\_ZU4EV}$		Hold							ns
$T_{PSMMCMCC\_ZU5EV}$		Setup	XCZU5EV						ns
$T_{PHMMCMCC\_ZU5EV}$		Hold							ns
$T_{PSMMCMCC\_ZU6EG}$		Setup	XCZU6EG	1.88	2.04	2.19	2.19	2.19	ns
$T_{PHMMCMCC\_ZU6EG}$		Hold		0.42	0.42	0.42	0.71	0.71	ns
$T_{PSMMCMCC\_ZU7EV}$		Setup	XCZU7EV						ns
$T_{PHMMCMCC\_ZU7EV}$		Hold							ns
$T_{PSMMCMCC\_ZU9EG}$		Setup	XCZU9EG	1.88	2.04	2.19	2.19	2.19	ns
$T_{PHMMCMCC\_ZU9EG}$		Hold		0.42	0.42	0.42	0.71	0.71	ns
$T_{PSMMCMCC\_ZU11EG}$		Setup	XCZU11EG						ns
$T_{PHMMCMCC\_ZU11EG}$		Hold							ns
$T_{PSMMCMCC\_ZU15EG}$		Setup	XCZU15EG	1.88	2.08	2.26	2.29	2.29	ns
$T_{PHMMCMCC\_ZU15EG}$		Hold		0.36	0.36	0.36	0.50	0.64	ns
$T_{PSMMCMCC\_ZU17EG}$		Setup	XCZU17EG						ns
$T_{PHMMCMCC\_ZU17EG}$		Hold							ns
$T_{PSMMCMCC\_ZU19EG}$		Setup	XCZU19EG						ns
$T_{PHMMCMCC\_ZU19EG}$		Hold							ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 92: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
T_{SAMP_BUFG} (1)						ps
$T_{SAMP\_NATIVE\_DPA}$						ps
$T_{SAMP\_NATIVE\_BISC}$						ps

Notes:

1. This parameter indicates the total sampling error of the Zynq UltraScale+ MPSoC DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 93: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCZU2EG	SBVA484		ps
			SFVA625	108	ps
			SFVC784		ps
		XCZU3EG	SBVA484		ps
			SFVA625	108	ps
			SFVC784		ps
		XCZU4EV	SFVC784		ps
			FBVB900		ps
		XCZU5EV	SFVC784		ps
			FBVB900		ps
		XCZU6EG	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU7EV	FBVB900		ps
			FFVC1156		ps
			FFVC1517		ps
		XCZU9EG	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU11EG	FFVC1156		ps
			FFVB1517		ps
			FFVF1517		ps
			FFVC1760		ps
		XCZU15EG	FFVC900		ps
			FFVB1156	132	ps
		XCZU17EG	FFVB1517		ps
			FFVC1760		ps
			FFVD1760		ps
			FFVE1924		ps
		XCZU19EG	FFVB1517		ps
			FFVC1760		ps
			FFVD1760		ps
			FFVE1924		ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

Table 94 summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 94: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s		–		mV
		6.6 Gb/s to 10.3125 Gb/s		–		mV
		≤ 6.6 Gb/s		–		mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V		–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to 1010		–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based)		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages)		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor(3)		–		–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* (UG576), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

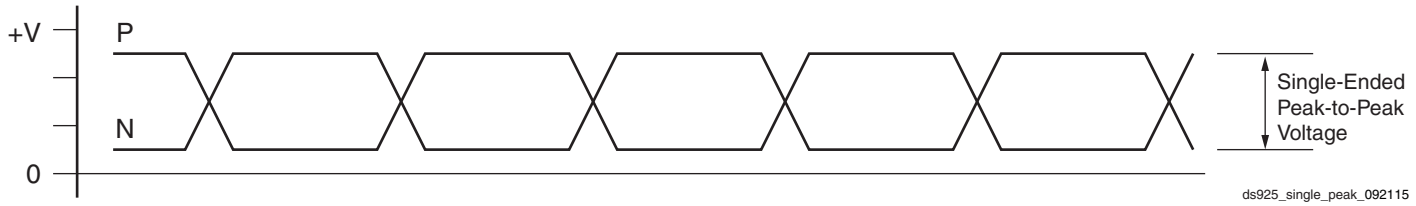

Figure 19: **Single-Ended Peak-to-Peak Voltage**

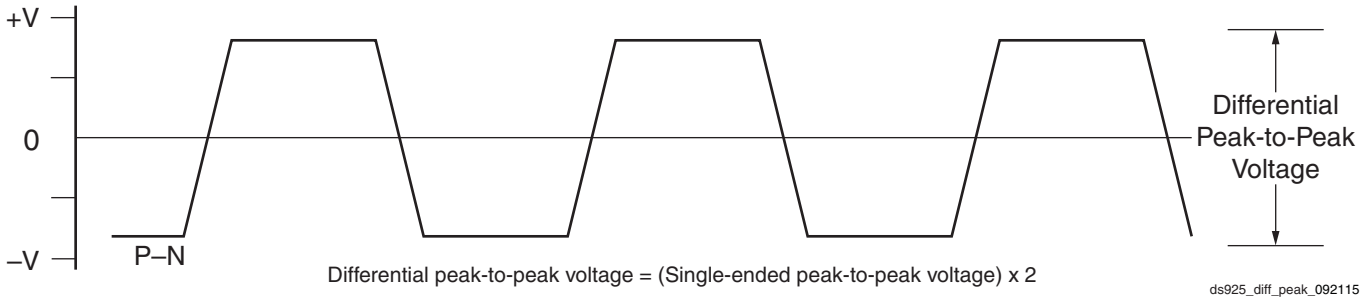

Figure 20: **Differential Peak-to-Peak Voltage**

Table 95 and Table 96 summarize the DC specifications of the GTH transceivers input and output clocks in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 95: **GTH Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 96: **GTH Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output high voltage for P and N	R_T = 100Ω across P and N signals	–		–	mV
V_{OH}	Output low voltage for P and N	R_T = 100Ω across P and N signals	–		–	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	–		–	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	–		–	mV

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

Table 97: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F_{GTHMAX}	GTH maximum line rate.		16.375(1)		16.375(1)		12.5		12.5		10.3125		Gb/s
F_{GTHMIN}	GTH minimum line rate.		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHCRANGE}$	CPLL line rate range(2).	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE1}$	QPLL0 line rate range(3).	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.075	2.45	4.09375	2.45	4.075	Gb/s
		8	1.225	2.04688	1.225	2.04688	1.225	2.0375	1.225	2.04688	1.225	2.0375	Gb/s
		16	0.6125	1.02344	0.6125	1.02344	0.6125	1.01875	0.6125	1.02344	0.6125	1.01875	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE2}$	QPLL1 line rate range(4).	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

1. GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 98: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency.		MHz

Table 99: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

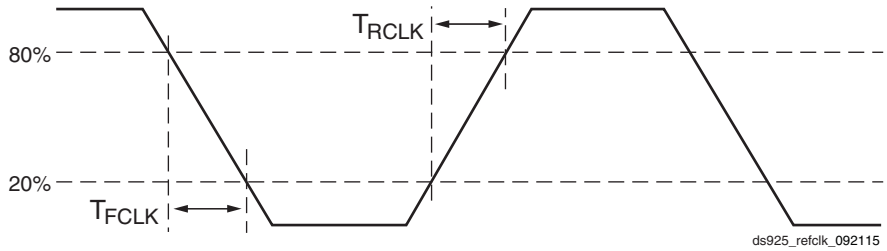

Figure 21: **Reference Clock Timing Parameters**

Table 100: **GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$ (1)(2)	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$ (1)(2)	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 x Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 101: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–			UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–			UI

Table 102: **GTH Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3(2)	-2(2)(3)	-1(4)	-2(3)	-1(3)(5)	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.

Table 103: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–		ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–		mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–		ns
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–		UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J15.1}$	Total jitter(2)(4)	15.1 Gb/s	–	–		UI
$D_{J15.1}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–		UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–		UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J12.5}$	Total jitter(2)(4)	12.5 Gb/s	–	–		UI
$D_{J12.5}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J11.3}$	Total jitter(2)(4)	11.3 Gb/s	–	–		UI
$D_{J11.3}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–		UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–		UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J9.953}$	Total jitter(2)(4)	9.953 Gb/s	–	–		UI
$D_{J9.953}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J8.0\_QPLL}$	Total jitter(2)(4)	8.0 Gb/s	–	–		UI
$D_{J8.0\_QPLL}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J8.0\_CPLL}$	Total jitter(3)(4)	8.0 Gb/s	–	–		UI
$D_{J8.0\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J6.6\_CPLL}$	Total jitter(3)(4)	6.6 Gb/s	–	–		UI
$D_{J6.6\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–		UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–		UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.75}$	Total jitter(3)(4)	3.75 Gb/s	–	–		UI
$D_{J3.75}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–		UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.20L}$	Total jitter(3)(4)	3.20 Gb/s(6)	–	–		UI
$D_{J3.20L}$	Deterministic jitter(3)(4)		–	–		UI

Table 103: **GTH Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(7)	–	–		UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(8)	–	–		UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–		UI
T_{J500}	Total jitter(3)(4)	500 Mb/s	–	–		UI
D_{J500}	Deterministic jitter(3)(4)		–	–		UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 104: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHRX}	Serial data rate		0.500	–	F_{GTHMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak			–		mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz		–	0	ppm
R_{XRL}	Run length (CID)		–	–		UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s		–		ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s		–		ppm
		Bit rates > 8.0 Gb/s		–		ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s		–	–	UI
$J_{T\_SJ15.1}$	Sinusoidal jitter (QPLL)(3)	15.1 Gb/s		–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)(3)	14.1 Gb/s		–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s		–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s		–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s		–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s		–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s		–	–	UI
$J_{T\_SJ9.953}$	Sinusoidal jitter (QPLL)(3)	9.953 Gb/s		–	–	UI
$J_{T\_SJ8.0\_QPLL}$	Sinusoidal jitter (QPLL)(3)	8.0 Gb/s		–	–	UI
$J_{T\_SJ8.0\_CPLL}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s		–	–	UI
$J_{T\_SJ6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s		–	–	UI

Table 104: **GTH Transceiver Receiver Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s		–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s		–	–	UI
$J_{T\_SJ3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s		–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)		–	–	UI
$J_{T\_SJ3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)		–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)		–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)		–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s		–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s		–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s		–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s		–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s		–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in Table 105. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 105: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI	SMPTE 424M-2006	0.27–2.97	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant

GTH Transceiver Protocol Jitter Characteristics

For Table 106 through Table 111, the *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended settings for optimal usage of protocol specific characteristics.

Table 106: **Gigabit Ethernet Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–		UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250		–	UI

Table 107: **XAUI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–		UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125		–	UI

Table 108: **PCI Express Protocol Characteristics (GTH Transceivers)(1)**

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–		UI
PCI Express Gen 2	Total transmitter jitter		5000	–		UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–		ps
	Deterministic transmitter jitter uncorrelated			–		ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500		–	UI
PCI Express Gen 2(2)	Receiver inherent timing error		5000		–	UI
	Receiver inherent deterministic timing error				–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000		–	UI
		1.0 MHz–10 MHz		Note 3	–	UI
		10 MHz–100 MHz			–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 109: **CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–		UI
		CEI-6G-LR	–		UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR		–	UI
		CEI-6G-LR		–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–		UI
		CEI-11G-LR/MR	–		UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR		–	UI
		CEI-11G-MR		–	UI
		CEI-11G-LR		–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 110: **SFP+ Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–		UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)		–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 111: **CPRI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–		UI
	1228.8	–		UI
	2457.6	–		UI
	3072.0	–		UI
	4915.2	–		UI
	6144.0	–		UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4		–	UI
	1228.8		–	UI
	2457.6		–	UI
	3072.0		–	UI
	4915.2		–	UI
	6144.0		–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 110.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 112 summarizes the DC specifications of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult www.xilinx.com/products/technology/high-speed-serial for further details.

Table 112: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s		–		mV
		6.6 Gb/s to 10.3125 Gb/s		–		mV
		≤ 6.6 Gb/s		–		mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V		–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to 1010		–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

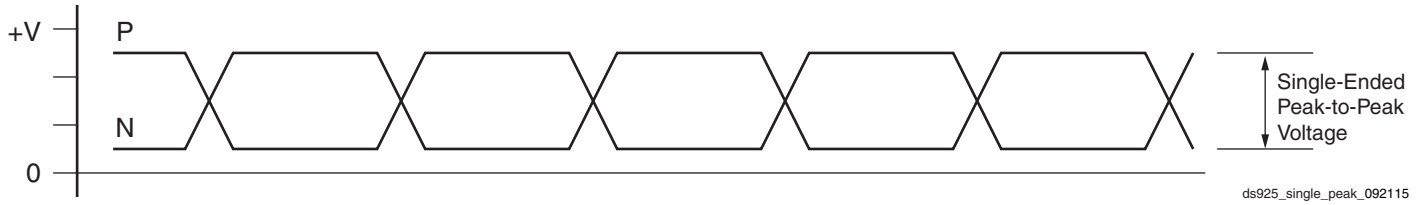

Figure 22: **Single-Ended Peak-to-Peak Voltage**

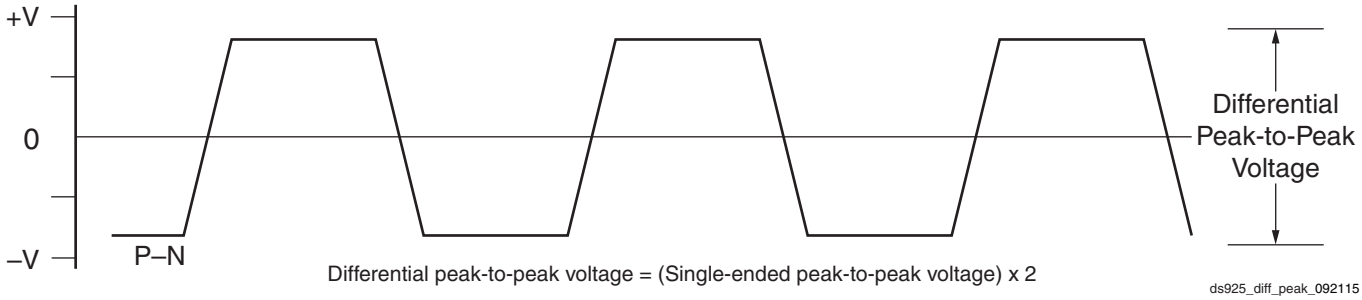

Figure 23: **Differential Peak-to-Peak Voltage**

Table 113 summarizes the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult www.xilinx.com/products/technology/high-speed-serial for further details.

Table 113: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 114: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output high voltage for P and N	R_T = 100Ω across P and N signals	–		–	mV
V_{OH}	Output low voltage for P and N	R_T = 100Ω across P and N signals	–		–	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	–		–	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	–		–	mV

GTY Transceiver Switching Characteristics

Consult www.xilinx.com/products/technology/high-speed-serial for further information.

Table 115: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F_{GTYMAX}	GTY maximum line rate		32.75		28.21		12.5		28.21		12.5		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range(1)	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range(2)	1	19.6	32.75	19.6	28.21	N/A		19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	Gb/s
		8	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	Gb/s
		16	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range(3)	1	16.0	26.0	16.0	26.0	N/A		16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
2. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 116: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.		MHz

Table 117: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

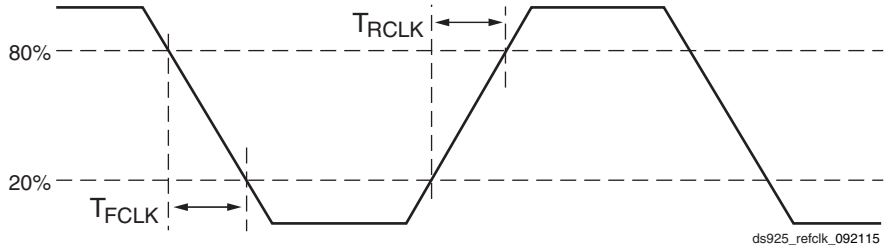

Figure 24: **Reference Clock Timing Parameters**

Table 118: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask(1)**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 119: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–			UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–			UI

Table 120: **GTY Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85		0.72		
		Internal Logic	Interconnect Logic	-3	-2	-1	-2	-1	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	511.719	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	511.719	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	195.313	402.813	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	156.250	352.625	156.250	MHz

Notes:

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).

Table 121: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–		–	ps
T_{FTX}	TX fall time	80%–20%	–		–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–		ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–		mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–		ns
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–		UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–		UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J12.5}$	Total jitter(2)(4)	12.5 Gb/s	–	–		UI
$D_{J12.5}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J11.3}$	Total jitter(2)(4)	11.3 Gb/s	–	–		UI
$D_{J11.3}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–		UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–		UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J9.953}$	Total jitter(2)(4)	9.953 Gb/s	–	–		UI
$D_{J9.953}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J9.8}$	Total jitter(2)(4)	9.8 Gb/s	–	–		UI
$D_{J9.8}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J8.0\_QPLL}$	Total jitter(2)(4)	8.0 Gb/s	–	–		UI
$D_{J8.0\_QPLL}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J8.0\_CPLL}$	Total jitter(3)(4)	8.0 Gb/s	–	–		UI
$D_{J8.0\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J6.6\_CPLL}$	Total jitter(3)(4)	6.6 Gb/s	–	–		UI
$D_{J6.6\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–		UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–		UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.75}$	Total jitter(3)(4)	3.75 Gb/s	–	–		UI
$D_{J3.75}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–		UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.20L}$	Total jitter(3)(4)	3.20 Gb/s(6)	–	–		UI
$D_{J3.20L}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(7)	–	–		UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–		UI

Table 121: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(8)	–	–		UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–		UI
T_{J500}	Total jitter(3)(4)	500 Mb/s	–	–		UI
D_{J500}	Deterministic jitter(3)(4)		–	–		UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 122: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–		–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak			–		mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz		–		ppm
R_{XRL}	Run length (CID)		–	–		UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s		–		ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s		–		ppm
		Bit rates > 8.0 Gb/s		–		ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ32.75}$	Sinusoidal jitter (CPLL)(3)	32.75 Gb/s		–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (CPLL)(3)	16.375 Gb/s		–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (CPLL)(3)	12.5 Gb/s		–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (CPLL)(3)	11.3 Gb/s		–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s		–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s		–	–	UI
$J_{T\_SJ9.8}$	Sinusoidal jitter (CPLL)(3)	9.8 Gb/s		–	–	UI
$J_{T\_SJ8.0\_QPLL}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s		–	–	UI
$J_{T\_SJ8.0\_CPLL}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s		–	–	UI
$J_{T\_SJ6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s		–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s		–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s		–	–	UI
$J_{T\_SJ3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s		–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)		–	–	UI
$J_{T\_SJ3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)		–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)		–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)		–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s		–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s		–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s		–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s		–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s		–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in Table 123. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 123: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
OTU4 (OTL4.4)	OIF-CEI-28G-VSR	27.952493	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI	SMPTE 424M-2006	0.27–2.97	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.

GTY Transceiver Protocol Jitter Characteristics

For Table 124 through Table 129, the *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended settings for optimal usage of protocol specific characteristics.

Table 124: **Gigabit Ethernet Protocol Characteristics (GTY Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–		UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250		–	UI

Table 125: **XAUI Protocol Characteristics (GTY Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–		UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125		–	UI

Table 126: **PCI Express Protocol Characteristics (GTY Transceivers)(1)**

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–		UI
PCI Express Gen 2	Total transmitter jitter		5000	–		UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–		ps
	Deterministic transmitter jitter uncorrelated			–		ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500		–	UI
PCI Express Gen 2(2)	Receiver inherent timing error		5000		–	UI
	Receiver inherent deterministic timing error				–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000		–	UI
		1.0 MHz–10 MHz		Note 3	–	UI
		10 MHz–100 MHz			–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 127: **CEI-6G and CEI-11G Protocol Characteristics (GTY Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–		UI
		CEI-6G-LR	–		UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR		–	UI
		CEI-6G-LR		–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–		UI
		CEI-11G-LR/MR	–		UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR		–	UI
		CEI-11G-MR		–	UI
		CEI-11G-LR		–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 128: **SFP+ Protocol Characteristics (GTY Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–		UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)		–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 129: **CPRI Protocol Characteristics (GTY Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter		–		UI
		–		UI
		–		UI
		–		UI
		–		UI
		–		UI
		–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance			–	UI
			–	UI
			–	UI
			–	UI
			–	UI
			–	UI
		Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 128.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoCs.

Table 130: **Maximum Performance for Interlaken Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		195.32		195.32		161.14		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		195.32		195.32		161.14		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	300.00(1)		300.00(1)		300.00	322.27	300.00(1)	429.69	300.00	322.27	MHz
		460.00(2)		460.00(2)				412.50(2)				MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	349.52	300.00	349.52	300.00	322.27			300.00	322.27	MHz

Notes:

1. The minimum value for CORE_CLK is 300 MHz for the 12 x 12.5G Interlaken configuration.
2. The minimum value for CORE_CLK is 412.5 MHz for the 6 x 25.78125G Interlaken configuration. This 6 x 25.78125G configuration is not supported in the lane logic-only mode.

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoCs.

Table 131: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2(1)	-1	-2	-1	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include this block.

Table 132: **Maximum Performance for PCI Express Designs(1)(2)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -2I and -3E speed grades.

Video Codec Performance

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoC EV devices that include the Video Codec unit (VCU).

Table 133: **VCU Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
Video Codec decoder block maximum frequency (H.264/5 10-bit 4:2:2)	667	667	667	667	667	MHz

PL System Monitor Specifications

Table 134: **PL SYSMON Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy(1)						
Resolution			10	–	–	Bits
Integral nonlinearity(2)	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity	INL	T_j = –55°C to 125°C	–	–	±1	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = –55°C to 125°C	–	–	±1	
Analog Inputs(2)						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
On-Chip Sensor Accuracy						
Temperature sensor error(1)		T_j = –40°C to 100°C (with external REF)	–	–	±4	°C
		T_j = –55°C to 125°C (with external REF)	–	–	±4.5	°C
		T_j = –40°C to 100°C (with internal REF)	–	–	±5	°C
		T_j = –55°C to 125°C (with internal REF)	–	–	±6.5	°C

Table 134: **PL SYSMON Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Supply sensor error(3)		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate(4)						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference(5)						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
4. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

PL SYSMON I2C/PMBus Interfaces

Table 135: **PL SYSMON I2C Fast Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	µs
T_{SMFCKH}	SCL High time	0.6	–	µs
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:
1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

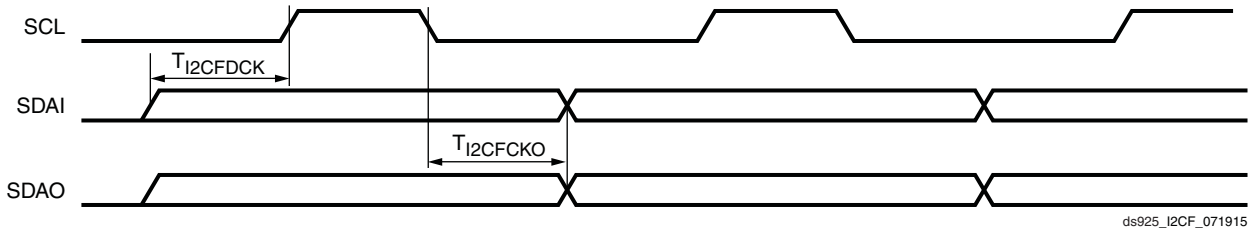

Figure 25: **PL SYSMON I2C Fast Mode Interface Timing**

Table 136: **PL SYSMON I2C Standard Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	µs
T_{SMSCKH}	SCL High time	4.0	–	µs
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:
1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

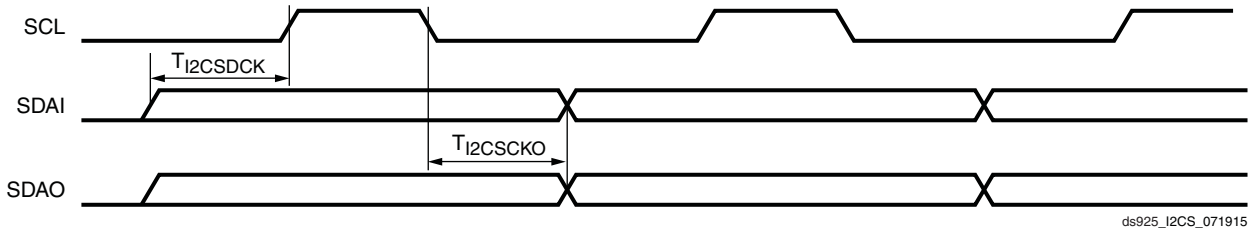

Figure 26: **PL SYSMON I2C Standard Mode Interface Timing**

Configuration Switching Characteristics

Table 137: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3)	200	200	200	175	175	MHz, Max
DNA Port Switching							
F_{DNACK}	DNA port frequency (DNA_PORT)	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency	50.00	50.00	50.00	50.00	50.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance	±15	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max

eFUSE Programming Conditions

Table 138: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{PLFS}	PL V_{CCAUX} supply current.	–	–	115	mA
I_{PSFS}	PS V_{CC_PSAUX} supply current.	–	–	115	mA
t_j	Temperature range.	–40	–	125	°C

Notes:

1. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/20/2016	1.1	Updated the Summary description. In Table 1, revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU}, I_{RPD}, and Note 4 to Table 2 and updated $V_{PS\_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5. Updated Note 5 in Table 5. Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added MIPI_DPHY_DCI to Table 13, Table 14, and Table 16. Updated Table 22, including removing the V_{CCO} specification and adding Note 1. Added Note 1 to Table 23. Updated Table 24 speed specifications for Vivado Design Suite 2016.1. Added values to Table 27. Updated the -2 value in Table 28. Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 32. Added VCO frequencies to Table 35. Added the T_{PSPOR} minimum to Table 36 and updated Note 1. Added Table 37. Added value delineation over V_{CCINT} operating voltages in Table 38. Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 39 and added value delineation over V_{CCINT} operating voltages. Updated Note 1 in Table 40, Table 41, and Table 42. Revised some units and Note 1 in Table 43 and Table 44. Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 45. Added $F_{TSU\_REF\_CLK}$ to Table 46 and updated Note 1. In Table 47, revised $T_{DCSDHSCLK1}$, $T_{DCSDHSCLK2}$, and $T_{DCSDHSCLK3}$ and Note 1. In Table 48, revised Note 1. In Table 49, revised Note 1. Revised Table 50, including Note 1, and added Note 2 and Note 3. In Table 51, Table 52, Table 53, and Table 55, revised Note 1. Updated Table 72. Replaced Table 74. Updated Table 75 and Table 76. Updated the tables in the I/O Standard Adjustment Measurement Methodology section. In Table 80, added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 59 and Table 95. Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97. Added Table 100 and Table 118. Added Note 2 to Table 112. Revised data in Table 115. Revised Table 120. Revised data and added notes to Table 130 and Table 131. Moved Table 133. Revised INL in Table 134. Added notes to Table 135 and Table 136. In Table 138, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.

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