TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

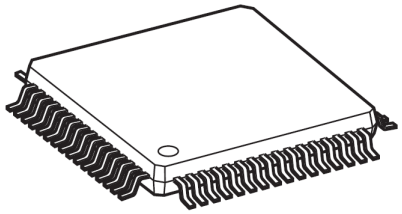
TC90106FG

Multi System Video Decoder for Component input

TC90106FG is the Video decoder which incorporated a video selector. The CVBS supports 3 input, and the Component or Y/C supports 2 input.

The Component supports 480i & 480p & 576i & 576p.

The output supports ITU-R BT.656 or 4:2:2 signal of 8bits serial output (SAV & EAV implantation)



LQFP64-P-1010-0.50E

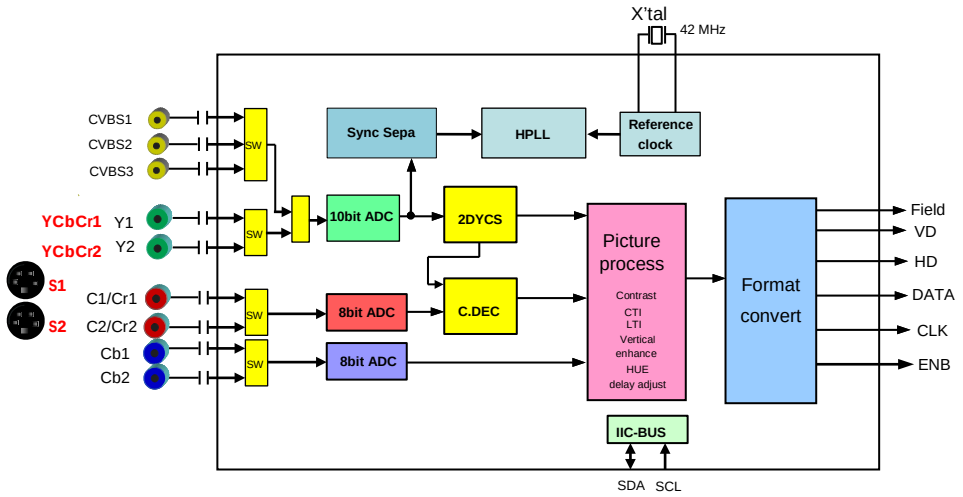
Weight: 0.4 g (typ.)

1. Feature

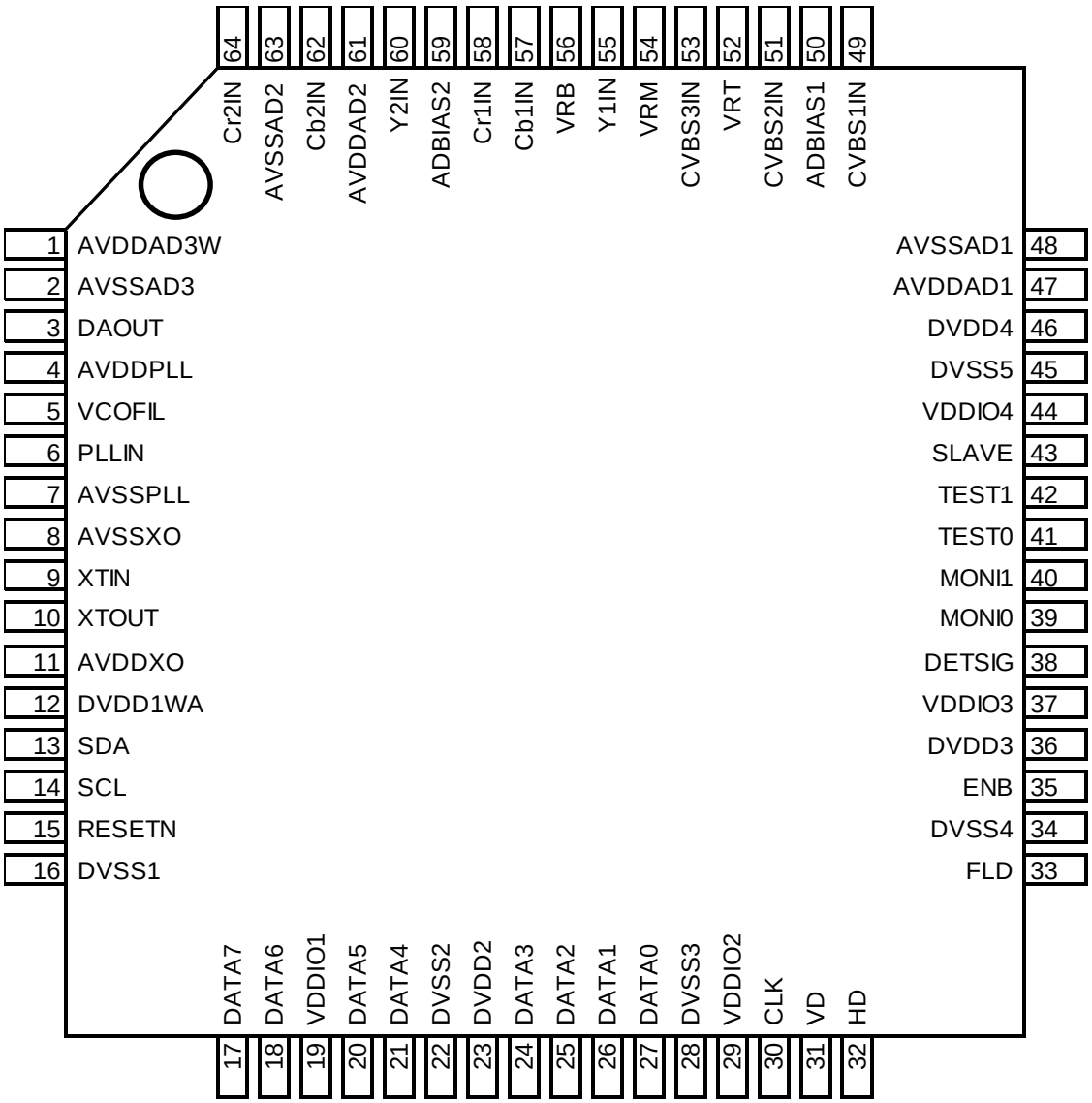
- Input signal: CVBS is 3ch, S-video is 2ch, Component is 2ch.
- Internal 10bit ADC 1ch and 8bit ADC 2ch.
- Y/C separation: 3-line YCS (NTSC/PAL)
  Band Pass Filter (SECAM)
- Full multi-color decoder
- Picture process Y: brightness, contrast, sharpness, noise cancel, V-Enhance, LTI
  C: TOF, ACC, color gain, CTI, noise cancel, Hue
- Judgment of D1/D2
- Function to output High/Low on a terminal when not a signal.
- Automatically mute function when not a signal.
- Function to improve gradation.
- 8bit ITU-R BT.656 / 8bit 4:2:2 Serial + SAV/EAV implantation + Sync output
- I^2C-bus control
- Operating temperature: -40°C to + 85°C
- Package: LQFP64-P-1010-0.50E (0.50 mm pitch)
- Power supply: 3.3 V, 2.5 V, 1.5 V

2. Block Diagram

The function block / circuit / fixed value in the block diagram omit this, or it easily writes it.



3. Pin Layout



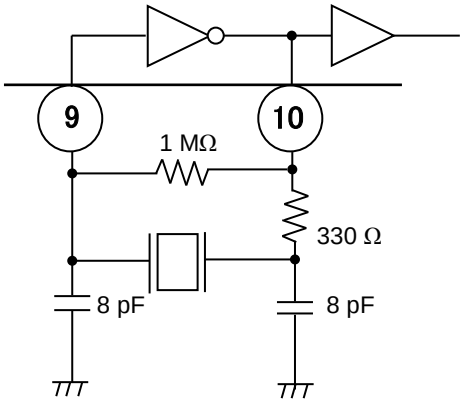
4. Pin Descriptions

Pin No.	Pin Name	Pin Function	Pin Type	Withstand voltage [V]	Processing at unused time
1	AVDDAD3W	2.5 V power supply for ADC	VDD	2.5	−
2	AVSSAD3	GND for ADC	GND	0	−
3	DAOUT	Output of DAC circuit	OUT	2.5	−
4	AVDDPLL	2.5 V power supply for DAC/PLL	VDD	2.5	−
5	VCOFIL	VCO Filter terminal	OUT	2.5	−
6	PLLIN	Input of PLL circuit	IN	2.5	−
7	AVSSPLL	DAC/PLL GND	GND	0	−
8	AVSSXO	GND for X'tal circuit	GND	0	−
9	XTIN	Input for X'tal circuit	IN	2.5	−
10	XTOUT	Output for X'tal circuit	OUT	2.5	−
11	AVDDXO	Power supply for X'tal	VDD	2.5	−
12	DVDD1WA	1.5 V power supply for Logic circuit	VDD	1.5	−
13	SDA	I^2C-BUS SDA terminal	IN/OUT	5.0	−
14	SCL	I^2C-BUS SCL terminal	IN	5.0	−
15	RESETN	System reset	IN	3.3	−
16	DVSS1	Digital GND	GND	0	−
17	DATA7	DATA7 output	OUT	3.3	Open
18	DATA6	DATA6 output	OUT	3.3	Open
19	VDDIO1	3.3 V power supply for I/O	VDD	3.3	−
20	DATA5	DATA5 output	OUT	3.3	Open
21	DATA4	DATA4 output	OUT	3.3	Open
22	DVSS2	Digital GND	GND	0	−
23	DVDD2	1.5 V power supply for Logic circuit	VDD	1.5	−
24	DATA3	DATA3 output	OUT	3.3	Open
25	DATA2	DATA2 output	OUT	3.3	Open
26	DATA1	DATA1 output	OUT	3.3	Open
27	DATA0	DATA0 output	OUT	3.3	Open
28	DVSS3	Digital GND	GND	0	−
29	VDDIO2	3.3 V power supply for I/O	VDD	3.3	−
30	CLK	Clock signal output	OUT	3.3	−
31	VD	VD signal output	OUT	3.3	Open
32	HD	HD signal output	OUT	3.3	Open

Pin No.	Pin Name	Pin Function	Pin Type	Withstand voltage [V]	Processing at unused time
33	FLD	Field signal output	OUT	3.3	Open
34	DVSS4	Digital GND	GND	0	—
35	ENB	Enable signal output. It is same the HD timing.	OUT	3.3	Open
36	DVDD3	1.5 V power supply for Logic circuit	VDD	1.5	—
37	VDDIO3	3.3 V power supply for I/O	VDD	3.3	—
38	DETSIG	Output of No signal Low： No signal High： In signal	OUT	3.3	Open
39	MONI0	Monitor output terminal 0	OUT	3.3	Open
40	MONI1	Monitor output terminal 1	OUT	3.3	Open
41	TEST0	For TEST signal, Connect to GND	IN	3.3	—
42	TEST1	For TEST signal, Connect to GND	IN	3.3	—
43	SLAVE	Slave address select	IN	3.3	—
44	VDDIO4	3.3 V power supply for I/O	VDD	3.3	—
45	DVSS5	Digital GND	GND	0	—
46	DVDD4	1.5V power supply for Logic circuit	VDD	1.5	—
47	AVDDAD1	2.5V power supply for ADC	VDD	2.5	—
48	AVSSAD1	Analog GND for ADC	GND	0	—
49	CVBS1IN	CVBS Input 1	IN	2.5	To GND via 0.1μF
50	ADBIAS1	Bias terminal for 10bit ADC	BIAS	2.5	-
51	CVBS2IN	CVBS Input 2	IN	2.5	To GND via 0.1μF
52	VRT	Upper limit reference voltage for ADC	BIAS	2.5	—
53	CVBS3IN	CVBS Input 3	IN	2.5	To GND via 0.1μF
54	VRM	Middle of reference voltage for ADC	BIAS	2.5	-
55	Y1IN	Y Input 1	IN	2.5	To GND via 0.1μF
56	VRB	Lower limit reference voltage for ADC	BIAS	2.5	-
57	Cb1IN	Cb Input 1	IN	2.5	To GND via 0.1μF
58	Cr1IN	Cr Input 1	IN	2.5	To GND via 0.1μF
59	ADBIAS2	Bias terminal for 8bit ADC	BIAS	2.5	-
60	Y2IN	Y Input 2	IN	2.5	To GND via 0.1μF
61	AVDDAD2	2.5V power supply for ADC	VDD	2.5	-
62	Cb2IN	Cb Input 2	IN	2.5	To GND via 0.1μF
63	AVSSAD2	Analog GND for ADC	GND	0	-
64	Cr2IN	Cr Input 2	IN	2.5	To GND via 0.1μF

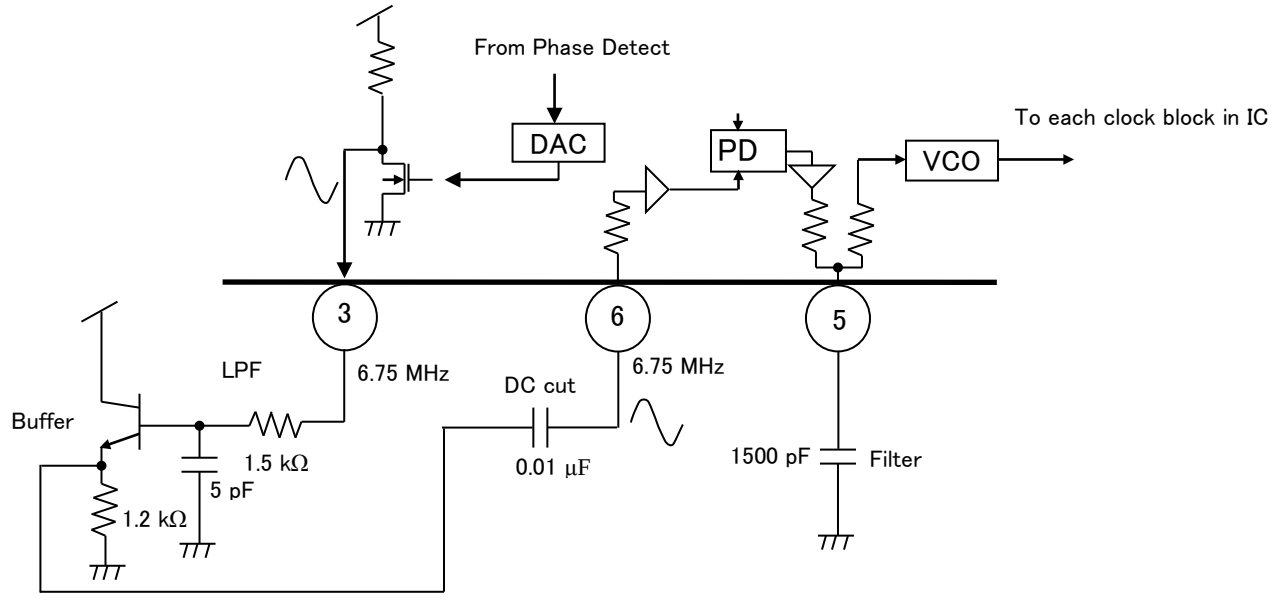
4.1 X'tal input and output terminal

Terminal 9 and Terminal 10 is connection terminal of Crystal.
The Inverter is contained between 9pin and 10pin of the IC. Let it oscillate in the basic wave of the crystal oscillator. The following figures are recommended basic wave oscillation circuits.
Recommended X'tal is fundamental frequency of 42MHz. The frequency deviation of the crystal oscillator chooses to be small.
The frequency deviation influences the subcarrier lock range of fsc.
When the deviation of 50 ppm, NTSC is 179 Hz (50 ppm of 3.579545 MHz), PAL is 222 Hz, It is shifted the Center of subcarrier lock range.
Standard for subcarrier lock range is -500 Hz to + 500 Hz
In this case, NTSC is -321 Hz (-500+179) to + 679 Hz (500+179).
The subcarrier lock range of fsc is possible to change by 16h_D6,
Normal Mode(16h_D6 = 0)**:** fsc ± 500 Hz
Wide Mode(16h_D6 = 1) **:** fsc ± 800 Hz



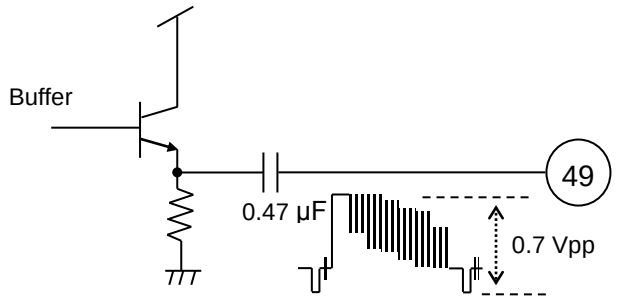
4.2 DAC output to PLLIN

HPLL is composed of 3pin**:** DAC-out to 5pin**:** VCO-Filter to 6pin**:** PLL-IN
It composes as VCO-out becomes the H-lock.
The following figures are recommended circuits.



4.3 CVBS and Y input terminal

49pin: CVBS in 1, 51pin: CVBS in 2, 53pin: CVBS in 3, 55pin: Y in 1, 60pin: Y in 2 are input terminal.
The following figure is recommended circuit.
The signal of 0.7 Vpp is inputted in each terminal via the C (0.47 µF).



5. Function

5.1 Overview

TC90106FG supports CVBS signal and Y/C signal(S signal) and Component signal (D1 or D2).
The CVBS signal can choose one among three input. The chosen CVBS is processed by the 3line YCseparation and multi-color decoder.
And output is ITU-R BT.656 and HD, VD, Field. Component signal supports 480i, 480p, 576i and 576p.
The Component signal can choose one from two inputs. And output is 54 MHz 8bit (SAV&EAV implantation) and HD, VD.
It chooses one among this input and can output it.
And incorporate various picture improvement functions.

5.2 Input signal

5.2.1 Recommended input level

TC90106FG supports CVBS signal and Y/C signal (S signal) and Component signal (D1 or D2).
The dynamic range of Y-ADC is designed AVDD × 0.4. (AVDD = 2.5 V (Typ.))
Please set the recommended standard input level on 0.7 Vp-p in 140IRE in NTSC/PAL and Y signal of 480i/p, 576i/p.

5.2.2 Input table

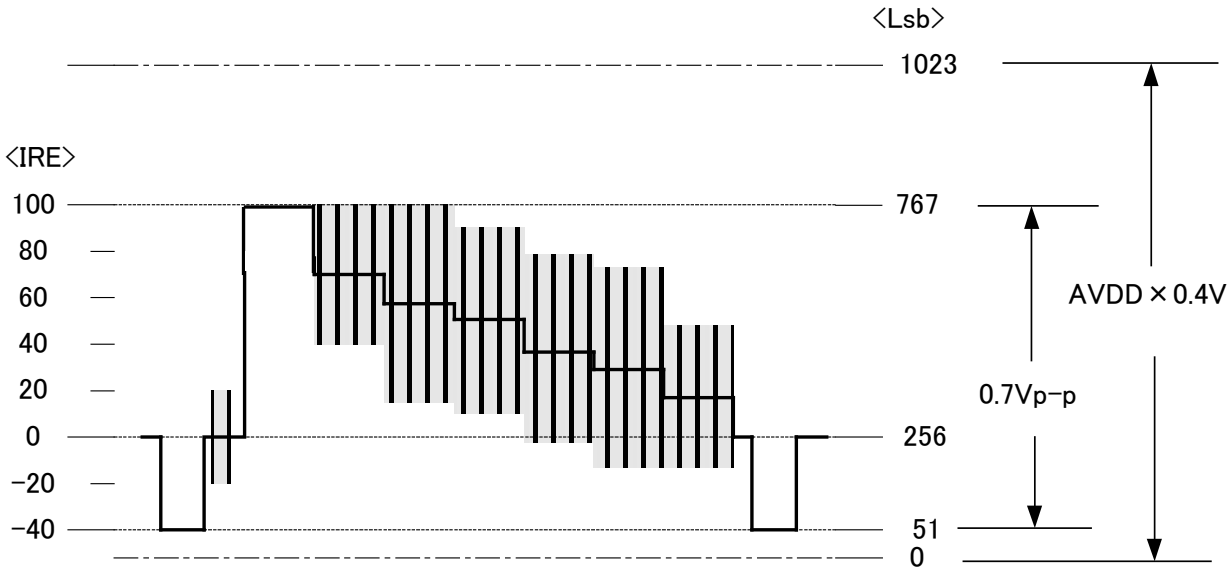
Input signal format			Frequency	
			fH[kHz]	fV[Hz]
CVBS	NTSC		15.75/15.734	60/59.94
	PAL		15.625	50
Y/C	NTSC		15.75/15.734	60/59.94
	PAL		15.625	50
YCbCr	D1	480i	15.75/15.734	60
		576i	15.625	50
	D2	480p	31.5/31.469	60
		576p	31.25	50

5.2.3 Input-Output table

Input signal				Processing		Output signal				
Input format			fH [kHz]	Sampling Clock [MHz]	Internal Processing Format	Output Clock [MHz]	656 8bit	HD	VD	Field
CVBS	NTSC		15.75/15.734	27	4:2:2	27	○	○	○	○
	PAL		15.625	27	4:2:2	27	○	○	○	○
Y/C	NTSC		15.75/15.734	27	4:2:2	27	○	○	○	○
	PAL		15.625	27	4:2:2	27	○	○	○	○
YCbCr	D1	480i	15.75/15.734	27	4:2:2	27	○	○	○	○
		576i	15.625	27	4:2:2	27	○	○	○	○
	D2	480p	31.5/31.469	27	4:2:2	54	○	○	○	−
		576p	31.25	27	4:2:2	54	○	○	○	−

5.2.4 Typical level of Analog input signal

1) CVBS signal / Y signal



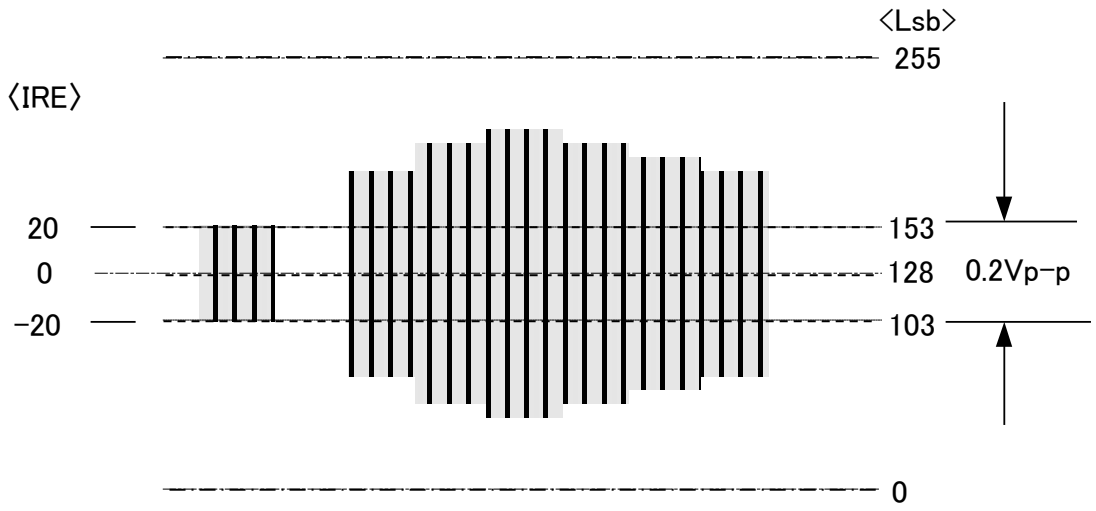
CVBS(Y) signal (to 10bit ADC) has to input 0.7 Vp-p (equal 140IRE) at the time of NTSC use.
And, The C input at the time of the S-input, 2) as shown, input level for ADC of C is 0.2 Vp-p (equal 40IRE).
(When VDD was 2.5 V, and 140IRE of the NTSC signal assumed it 0.7 Vp-p.)
When you use it in YCbCr, please be careful about input levels to C-AD (8bit ADC).
As for the input level of CbCr (8 bit ADC), please make 100% input 0.7 Vp-p, like 3) figures.
(The figure above is 75% color bar signal)

An input and output level list when it was based on 100% input.

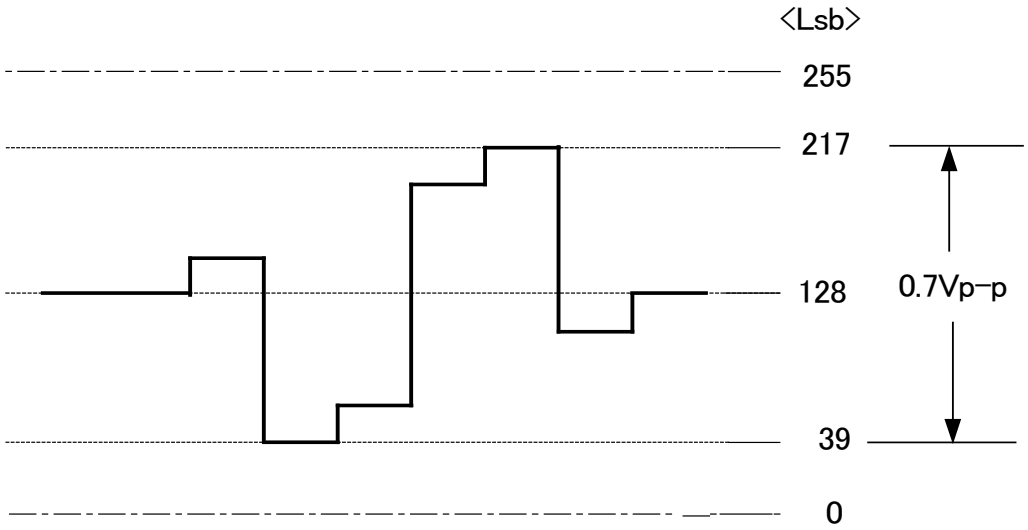
Input	Input level: Vp-p(*1)	Output: LSB (*2)	Notes
CVBS	0.7 Vp-p (500 mVp-p)	16-235 (8bit)	Output is 656 format
Y	0.7 Vp-p (500 mVp-p)	16-235 (8bit)	Output is 656 format
C	0.2 Vp-p (Burst)	31-225 (8bit)	Output is 656 format
Cb	0.7 Vp-p	31-225 (8bit)	Output is 656 format
Cr	0.7 Vp-p	31-225 (8bit)	Output is 656 format

*1 Input level : Input level of CVBS and Y is 140IRE at white 100%.
In (), It is the level from a pedestal to white 100%.
Input level of C (chroma) is Burst level of NTSC-CVBS signal.
Input level of CbCr is a level at the time of color-100% signal.
*2 Output level : Output level of CVBS and Y is 140IRE at white 100% of NTSC.
(Output is the level from a pedestal to white 100%.)
Output level of C is CbCr output level at time of color-100% signal.
Output of CbCr is a input at the time of color-100% signal.
(notes) Mentioned output level changes by picture level adjustment of contrast, gain, ACC, etc.
These are not maximum level.

2) C signal



3) Cb/Cr signal



5.3 Signal Output

5.3.1 H/V sync process

This IC processes horizontal sync separation and vertical sync separation, and outputs a signal of HD and VD. There are two output mode for pulse phase and pulse width. One is based on 656 format, other one is sync through mode which can output same timing and width as sync of input signal.

In 656 format mode, it is selectable from 656-3 and 656-4 mode.

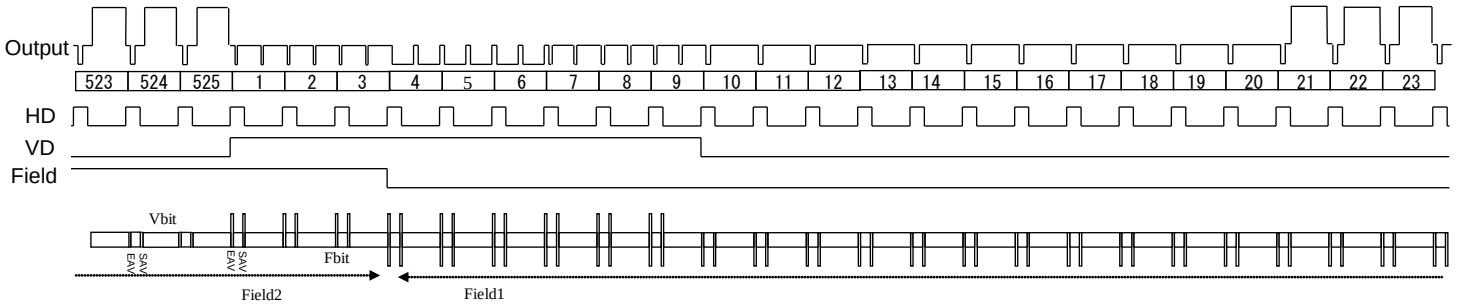
Setting the 656 mode

NTSC (CVBS)	Vbit: 1	Vbit: 0	Fbit: 1	Fbit: 0
656-3	9 line SAV			
		9 line EAV 263 line SAV	3 line SAV	
	263 line EAV 272 line SAV			3 line EAV 265 line SAV
		272 line EAV 525 line SAV	265 line EAV 528(3) line SAV	
	525 line EAV			528(3) line EAV
656-4	19 line SAV			
		19 line EAV 263 line SAV	3 line SAV	
	263 line EAV 282 line SAV			3 line EAV 265 line SAV
		282 line EAV 525 line SAV	265 line EAV 528(3) line SAV	
	525 line EAV			528 line EAV

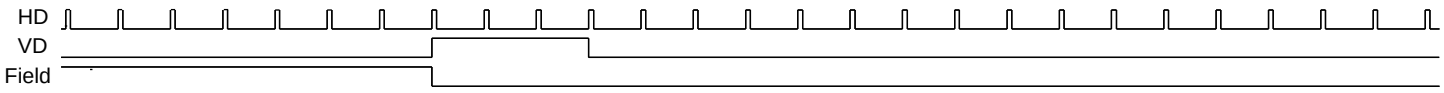
5.3.2 656 output timing of 480i / 60Hz

NTSC (525 line/60 Hz) first Field (odd)

at (25h_D6:0, 29h_D4:0)

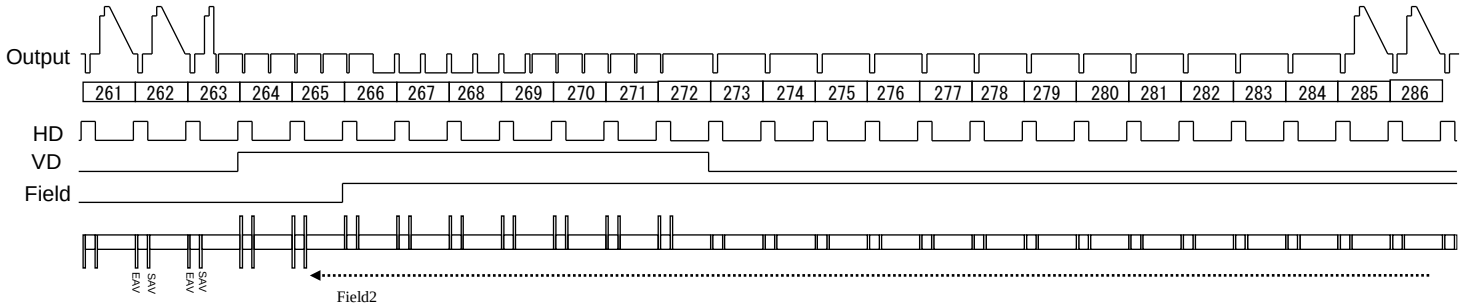


at (25h_D6:1, 29h_D4:1)

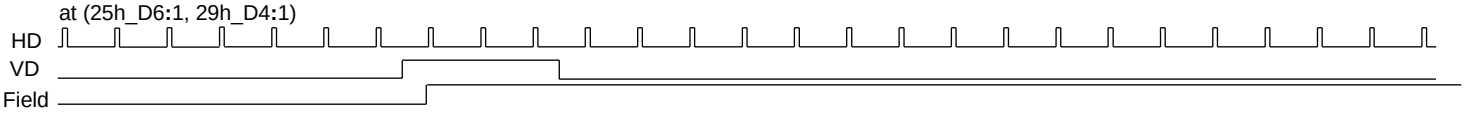


NTSC(525line/60Hz) second Field(even)

at (25h_D6:0, 29h_D4:0)



at (25h_D6:1, 29h_D4:1)



5.3.3 Output format

Output is 656 (27MHz_8bit_EAV&SAV) when input signal is CVBS, S, YCbCr(D1).
Output is 54MHz_8bit_serial_EAV&SAV when input signal is YCbCr (525p/625p).

Y: pedestal level = 16 LSB
C: center electric potential = 128 LSB

Signal process of Y output signal below pedestal is set by register CLP (Bank 0, Sub address 29h).
CLP = 1 : The signal under pedestal level is fixed on 16LSB
CLP = 0 : The signal under pedestal level is outputted through

Output	Bit	Data Rate	Notes
YCbCr [0-7]	8	27MHz・54MHz	ITU-R BT.656
Field	1	-	-
CLK	1	27MHz・54MHz	-
HD	1	fH	Separated Horizontal sync
VD	1	fV	Separated Vertical sync

6. Absolute maximum rating

The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the maximum rating may result in destruction, degradation or other damage to the IC and other components. When designing applications for this IC, be sure that none of the maximum rating values will ever be exceeded.

Characteristics	Symbol	Rating	Unit
Power voltage1 (1.5V system)	VDD1	-0.3 to VSS+2.0	V
Power voltage2 (2.5V system)	VDD2	-0.3 to VSS+3.5	V
Power voltage3 (3.3V system)	VDD3	-0.3 to VSS+3.9	V
Input voltage (2.5V system)	VIN2	-0.3 to VDD+0.3	V
Input voltage (3.3V system)	VIN3	-0.3 to VDD+0.3	V
Input voltage (3.3V system, 5V withstand voltage)	VIN4 (Note1)	-0.3 to VSS+5.5	V
Potential difference between power pins (between 1.5 V system power pins)	ΔVDG1 (Note2)	0.3	V
Potential difference between power pins (between 2.5 V system power pins)	ΔVDG2 (Note3)	0.3	V
Potential difference between power pins (between 3.3 V system power pins)	ΔVDG3 (Note4)	0.3	V
Power dissipation	PD (Note5)	1667	mW
Storage temperature	Tstg	-40 to 125	°C

Note1: The withstand voltage for pins (SDA, SCL) is 5 V.

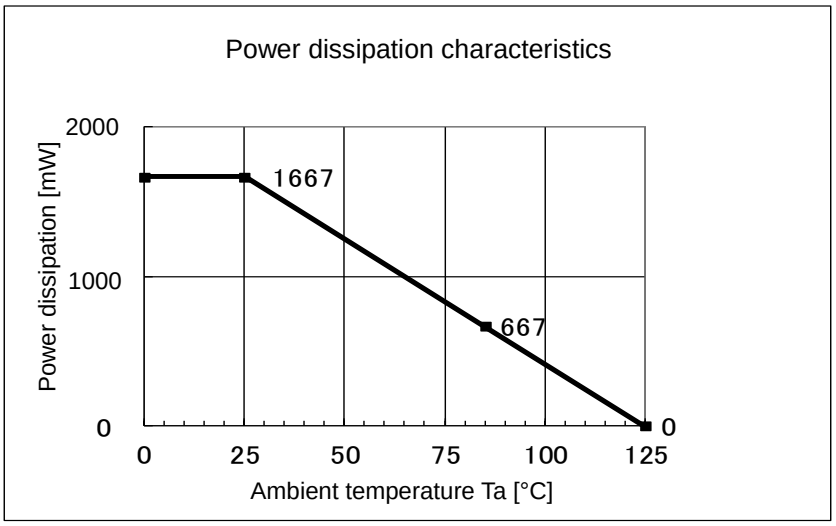
Note2: When you supply a voltage to the VDD pin of 1.5 V of voltage, the potential difference between these VDD pin, Please do not exceed the rated value of the described.

Note3: When you supply a voltage to the VDD pin of 2.5 V of voltage, the potential difference between these VDD pin Please do not exceed the rated value of the described.

Note4: When you supply a voltage to the VDD pin of 3.3 V of voltage, the potential difference between these VDD pin Please do not exceed the rated value of the described.

And, keep the maximum potential difference between all VSS pins within 0.01 V.

Note5: If you intended to use a temperature higher than Ta = 25°C, reduce by 16.67 mW per one degree (°C) increase.



7. Operating condition

The TC90106FG is not guaranteed to function correctly if it is used outside its specified power voltage rage (1.5 V system power**:** 1.40 V to 1.60 V, 2.5 V system power**:** 2.3 V to 2.7 V, 3.3 V system power**:** 3.0 V to 3.6 V). Please use within the specified operating conditions.
If you temporarily leave and then return to the specified operating conditions, this IC's conditions will change, and so it is necessary to reset the IC's power to continue using it correctly within the specified operating conditions.

Characteristics	Corresponding terminal	Symbol	Min	Typ.	Max	Unit
Power voltage of digital block	12, 23, 36, 46	VDD-D	1.4	1.5	1.6	V
Power voltage of I/O block	19, 29, 37, 44	VDD-IO	3.0	3.3	3.6	V
Power voltage of XO block	11	VDDXO	2.3	2.5	2.7	V
Power voltage of PLL block	4	VDDPLL	2.3	2.5	2.7	V
Power voltage of analog block	1, 47, 61	VDDDA, VDDAD	2.3	2.5	2.7	V
Operating templature	-	Topr	-40	―	85	°C

8. Electrical characteristic

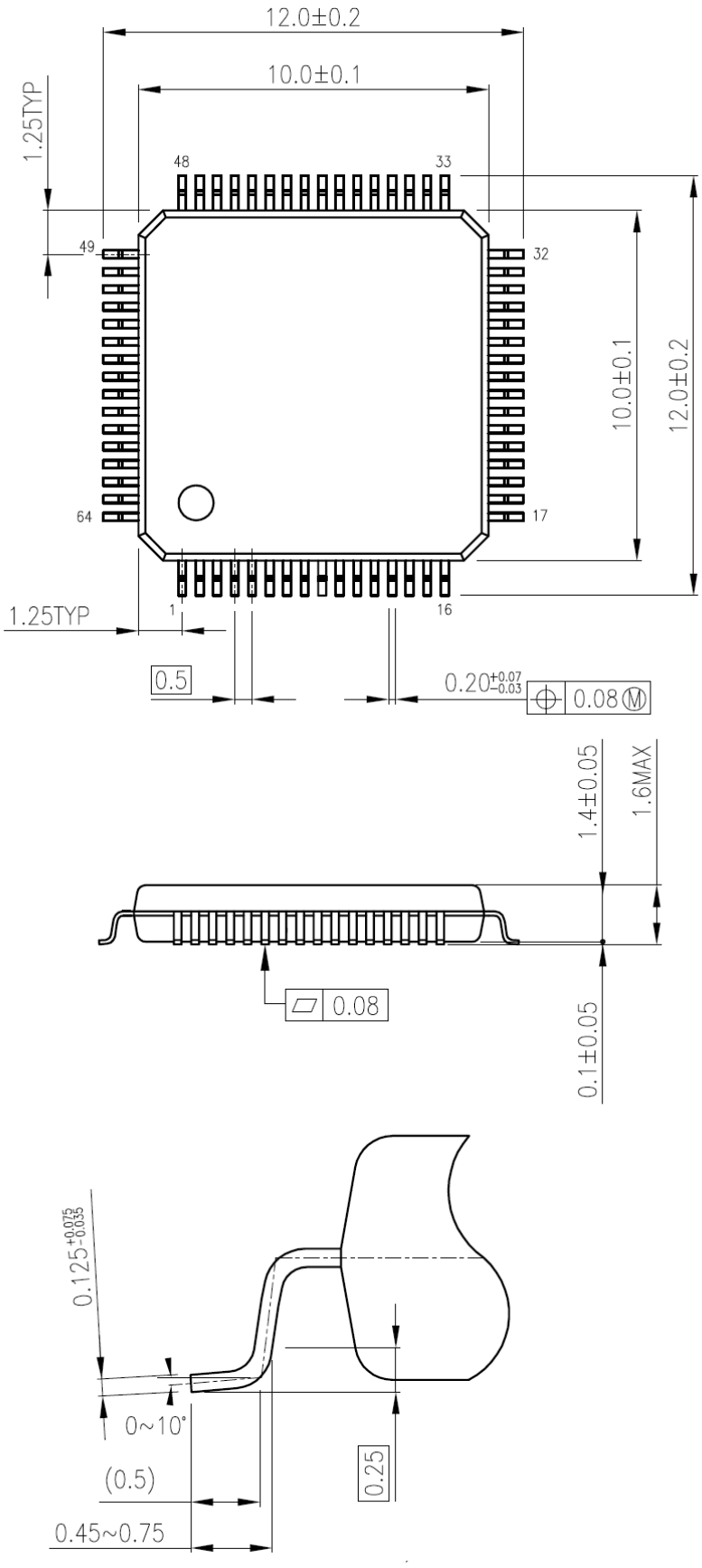
8.1 DC characteristic

(Ta = 25°C, VDD1 = 1.50 ± 0.1 V, VDD2 = 2.50 ± 0.2 V, VDD3 = 3.30 ± 0.3 V)

Characteristic	Terminal No.	Symbol	Min	Typ.	Max	unit	Notes
Powers upply current	12, 23, 36, 46	IDD1 (1.5 V system)	—	30	45	mA	3.3 V system current will change by I/O.
	1, 4, 11, 47, 61	IDD2 (2.5 V system)	—	100	120	mA	
	19, 29, 37, 44,	IDD3 (3.3 V system)	—	25	65	mA	
Input Voltage	15, 41, 42, 43	VIH	VDD3 x 0.8	—	VDD3	V	3.3 V I/O terminal
	13, 14						5.0 V withstand voltage I/O terminal
	15, 41, 42, 43	VIL	VSS	—	VDD3 x 0.2	V	3.3 V I/O terminal
	13, 14						5.0 V withstand voltage I/O terminal
Input current	15, 41, 42, 43	IIH	-10	—	10	μA	3.3 V I/O terminal
	13, 14						5.0 V withstand voltage I/O terminal
	15, 41, 42, 43	IIL	-10	—	10	μA	3.3 V I/O terminal
	13, 14						5.0 V withstand voltage I/O terminal
Output voltage	17, 18, 20, 21, 24, 25, 26, 27, 30, 31, 32, 33, 35, 38, 39, 40	V_{OH}	VDD3 - 0.6	—	VDD3	V	3.3 V I/O terminal when 4 mA out load
		V_{OL}	VSS	—	0.4	V	3.3 V I/O terminal when 4 mA out load

9. Package

LQFP64-P-1010-0.50E **Unit: mm**



Weight: 0.4 g (typ.)

10. Revision History

Date	Revision	Contents
15/09/30	1.00	First edition

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