# TGA2731-SM

***2.7 – 4.0 GHz Driver Amplifier***

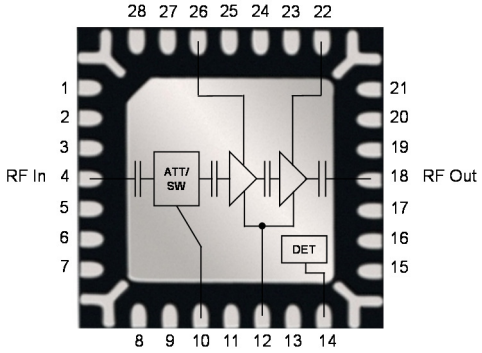
## Applications

- Commercial and Military Radar
- Communications
- Test Instrumentation


## Product Features

- Frequency Range: 2.7 - 4.0 GHz
- Small Signal Gain: > 24 dB
- Power: > 30.7 dBm
- PAE: > 22 %
- IM3: < -32 dBc (@ 3.5 GHz)
- Input Return Loss > 7 dB
- Output Return Loss > 11 dB
- Self-Bias: $V_D$ = 6 V, $V_G$ = 0 V, $I_{DQ}$ = 900 mA
- Single Supply Operation
- Package Dimensions: 5.0 x 5.0 x 0.85 mm

## Functional Block Diagram




## General Description

TriQuint's TGA2731-SM is a driver amplifier fabricated on TriQuint's TQPHT25 0.25um GaAs production process. The TGA2731-SM operates from 2.7 to 4.0 GHz and provides > 30.7 dBm of output power with > 22.7 dB of large signal gain. The TGA2731-SM also includes a 13dB attenuator at the input, and a simple resistively coupled power detector at the output. The amplifier can be operated from a single supply in the self-biased mode.

The TGA2731-SM is offered in a 5x5 mm plastic QFN. It is well-matched to 50 ohms, and includes integrated DC blocking caps on both RF ports allowing for simple system integration.

Lead-Free & RoHS compliant.

Evaluation Boards are available on request.

## Pad Configuration

| Pad Number | Symbol |
|---|---|
| 1-3, 5-9, 11 13, 15-17, 19-21, 23-25, 27-28 | No Connect |
| 4 | RF Input |
| 10 | $V_{SW}$ |
| 12 | $V_G$ |
| 14 | Power Sample |
| 18 | RF Output |
| 22 | $V_{D2}$ |
| 26 | $V_{D1}$ |
| 29 | GND |

## Ordering Information

| Part | ECCN | Description |
|---|---|---|
| TGA2731-SM | EAR99 | 2.7 – 4.0 GHz Driver Amplifier |

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Drain Voltage ($V_D$) | 9 |
| Gate Voltage Limits ($V_G$) | -1 V / 0V |
| Drain Current ($I_D$) | 1000 mA |
| Gate Current (+$I_G$ @$T_{CH}$ = 150 °C) | -5.28 / 24.8 mA |
| Power Dissipation, $T_{BASE}$ = 85 °C, $T_{CH}$ = 200 °C, CW operation (Pdiss) | 4.50 W |
| Input Power, CW, 50 Ω [1] | 13 dBm |
| Input Power, CW, VSWR 10:1 [1] | 13 dBm |
| Channel Temperature ($T_{CH}$) | 200 °C |

Notes:

1. $V_D$ = 6 V, $V_G$ = 0 V, $T_{BASE}$ = 85 °C

## Recommended Operating Conditions

| Parameter | Value |
|---|---|
| Drain Voltage ($V_D$) | 6 V |
| Gate Voltage ($V_G$) (self-biased mode) | 0 V |
| Quiescent Drain Current ($I_{DQ}$) | 900 mA |
| Operating Drain Current ($I_{D\_DRIVE}$) | 800-975 mA |

## Electrical Specifications

Test conditions, unless otherwise noted: T = 25 °C, $V_D$ = 6 V, $V_G$ = 0 V / $I_{DQ}$ ~ 900 mA, $V_{SW}$ = 0 V, part mounted to EVB
Output Power and PAE pulse conditions: PW = 100 us, DC = 20%

| Parameter | Min | Typical | Max | Units |
|---|---|---|---|---|
| Operating Frequency Range | 2.7 | | 4.0 | GHz |
| Output Power (Pulsed, Pin = 8 dBm) | | > 30.7 | | dBm |
| Power Added Efficiency (Pulsed, Pin = 8 dBm) | | > 22 | | % |
| Small Signal Gain | | > 24 | | dB |
| Input Return Loss | | > 7 | | dB |
| Output Return Loss | | > 11 | | dB |
| IM3 ($P_{OUT}$/tone ≤ 23 dBm, 3.5 GHz) | | < -32 | | dBc |
| 2nd Harm. Suppression ( $P_{OUT}$ ≤ 30 dBm, 3.5 GHz) | | < -39 | | dBc |
| 3rd Harm. Suppression ( $P_{OUT}$ ≤ 30 dBm, 3.5 GHz) | | < -44 | | dBc |
| Output Power Temperature Coefficient | | -0.004 | | dB/°C |

## Specifications

### Thermal and Reliability Information

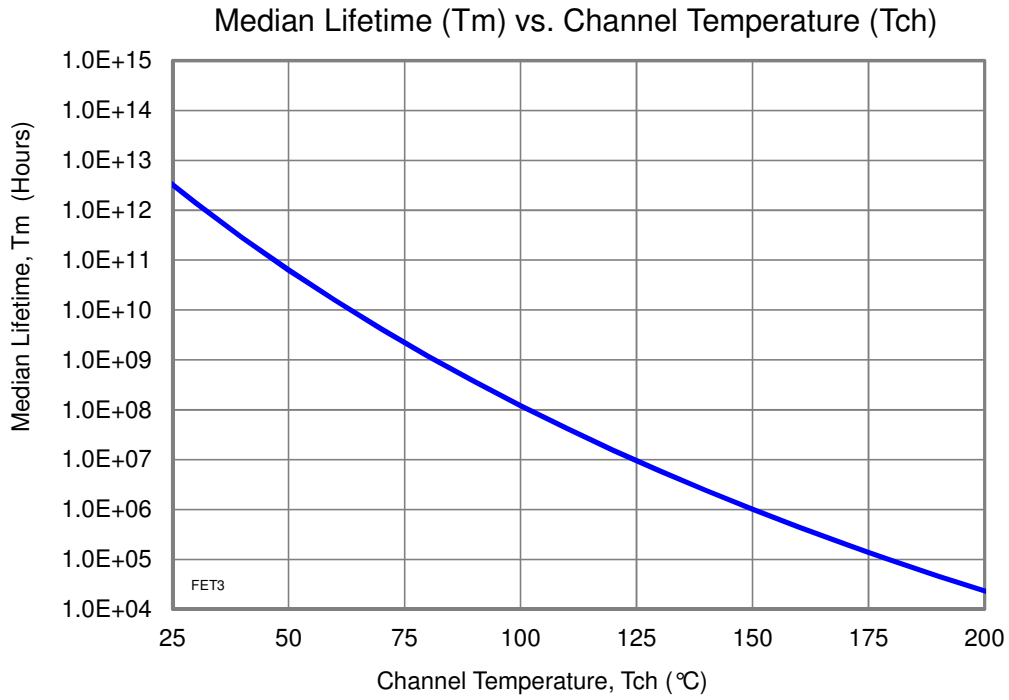
| Parameter | Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance ($\theta_{JC}$) (1) | $T_{BASE}$ = 85°C, $V_D$ = 6 V, $V_G$ = 0 V, $I_{D\_DRIVE}$ = 800 mA, Pulse Power Conditions: Pulse Width = 100 us, Duty Cycle = 10%, $P_{IN}$ = 0 dBm, $P_{OUT}$ = 27 dBm, $P_{DISS(PULSE)}$ = 4.75 W | 11.6 | ºC/W |
| Channel Temperature ($T_{CH}$) (1) | | 140 | °C |
| Median Lifetime ($T_M$) | | 2.4E06 | Hrs |

Note:

1. Package backside temperature fixed at 85 °C.

## Median Lifetime

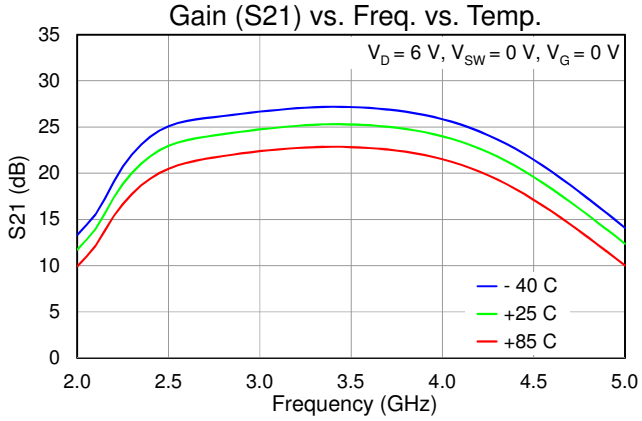
Test Conditions: 10 V; Failure Criterion = 10% reduction in $I_{D\ MAX}$



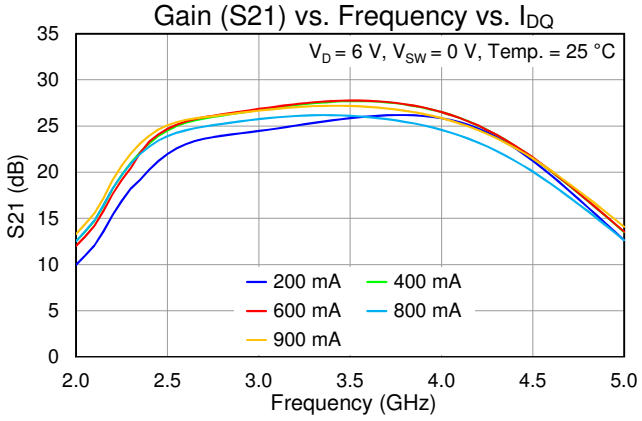
## Typical Performance – Small Signal

Test conditions, unless otherwise noted: T = 25 °C, part mounted to EVB

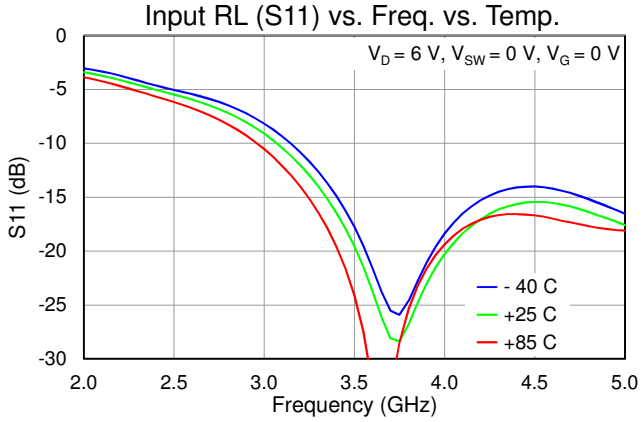
Gain (S21) vs. Freq. vs. Temp.



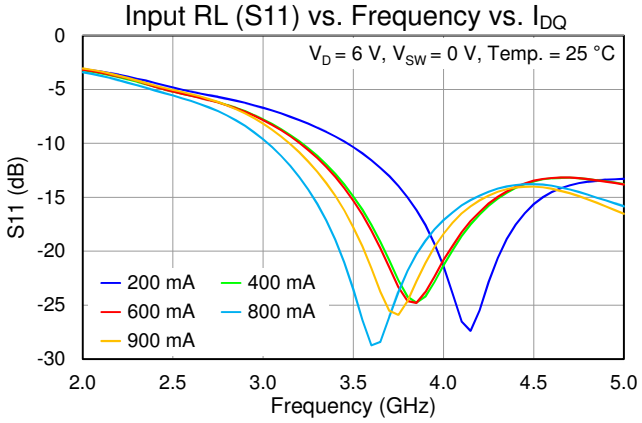

Gain (S21) vs. Frequency vs. $I_{DQ}$



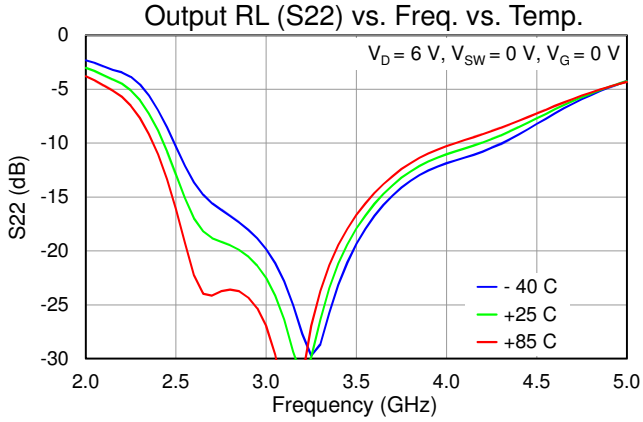

Input RL (S11) vs. Freq. vs. Temp.



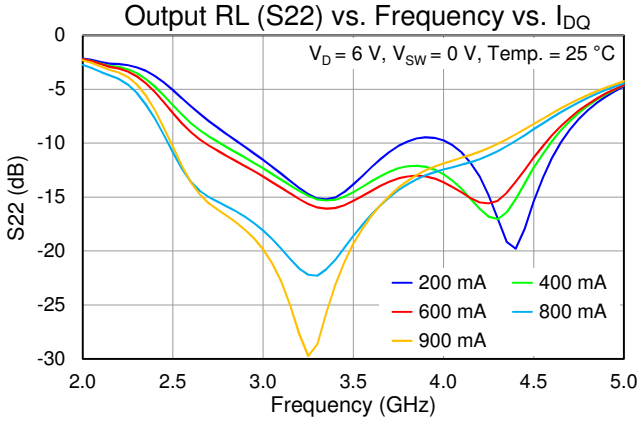

Input RL (S11) vs. Frequency vs. $I_{DQ}$




Output RL (S22) vs. Freq. vs. Temp.



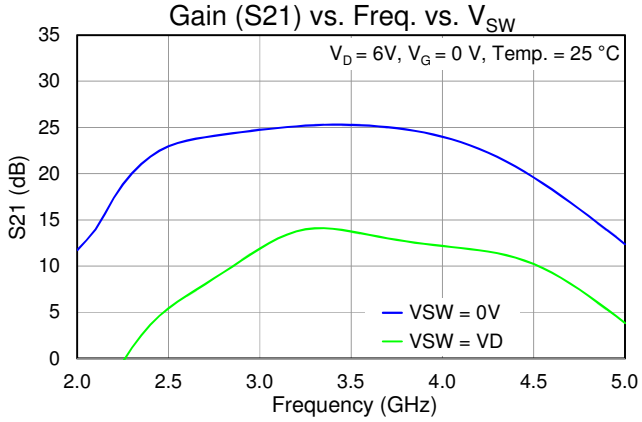

Output RL (S22) vs. Frequency vs. $I_{DQ}$



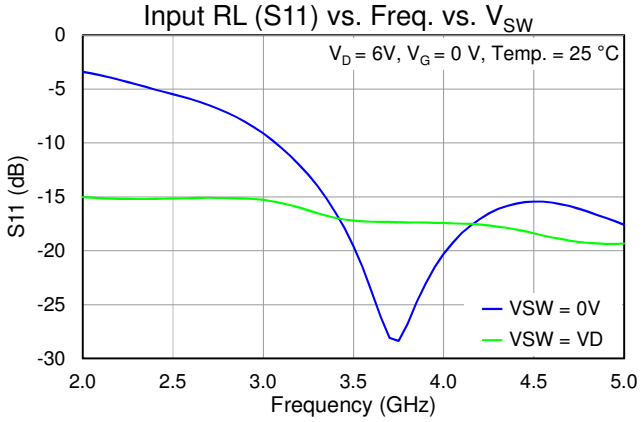
## Typical Performance – Small Signal

Test conditions, unless otherwise noted: T = 25 °C, part mounted to EVB

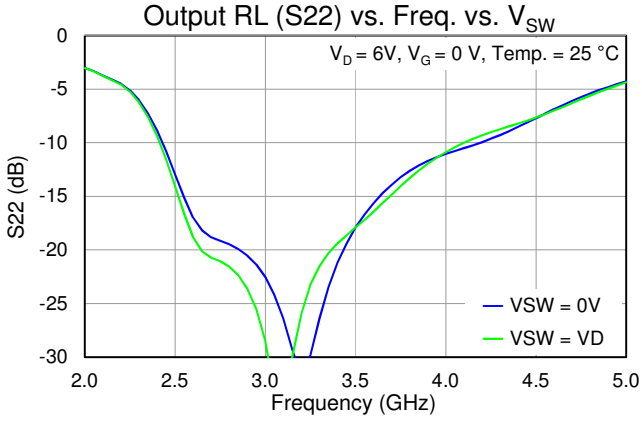
Gain (S21) vs. Freq. vs. $V_{SW}$




Input RL (S11) vs. Freq. vs. $V_{SW}$



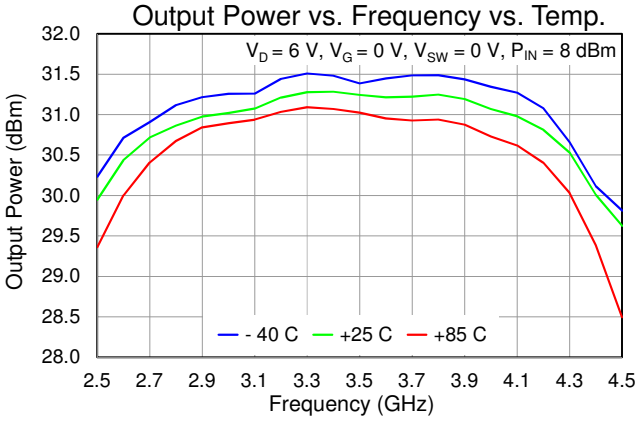

Output RL (S22) vs. Freq. vs. $V_{SW}$



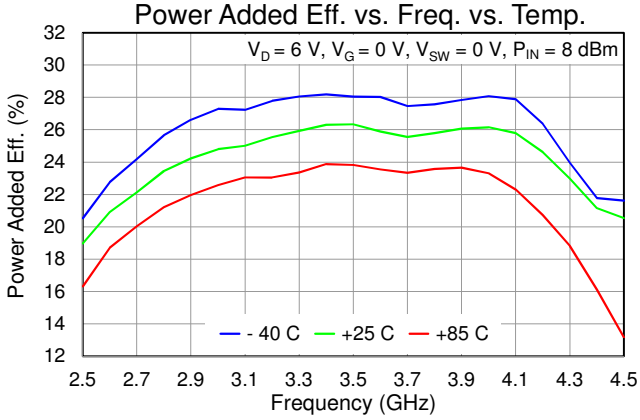
## Typical Performance – Large Signal (Pulsed)

Test conditions, unless otherwise noted: T = 25 °C, part mounted to EVB, Pulse Power: PW = 100 us, DC = 20%

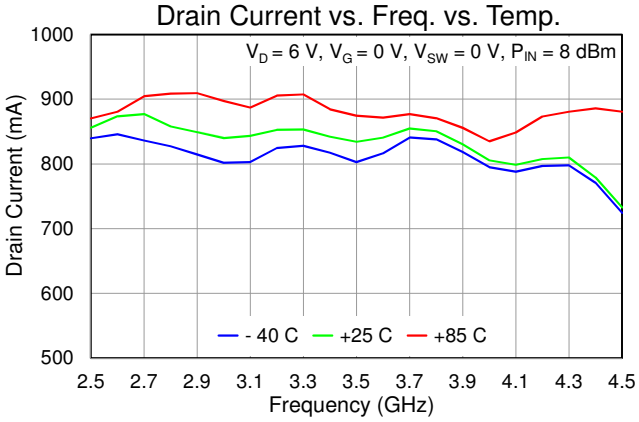
Output Power vs. Frequency vs. Temp.



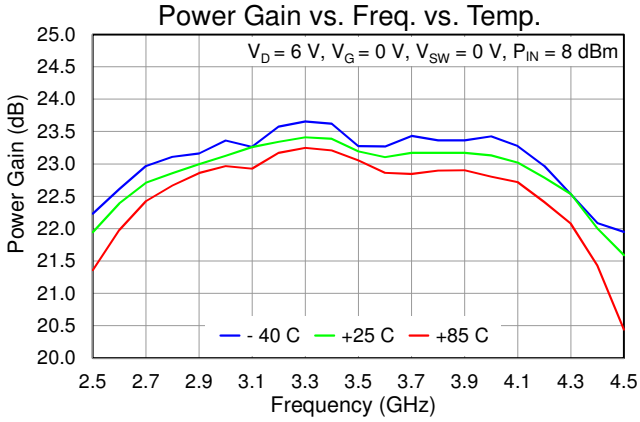

Power Added Eff. vs. Freq. vs. Temp.



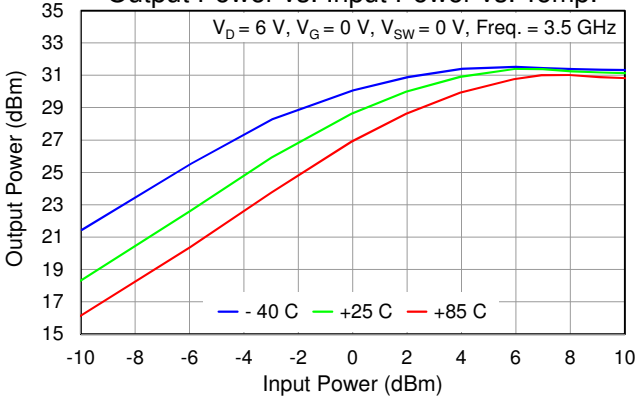

Drain Current vs. Freq. vs. Temp.



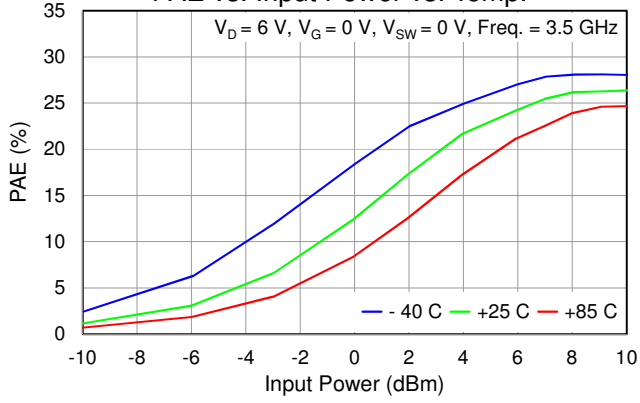

Power Gain vs. Freq. vs. Temp.




Output Power vs. Input Power vs. Temp.



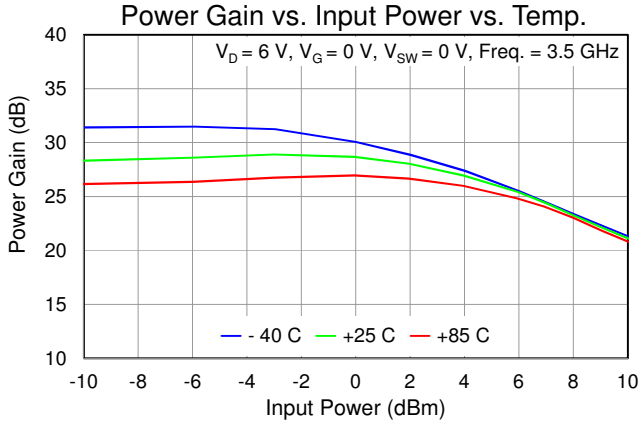

PAE vs. Input Power vs. Temp.



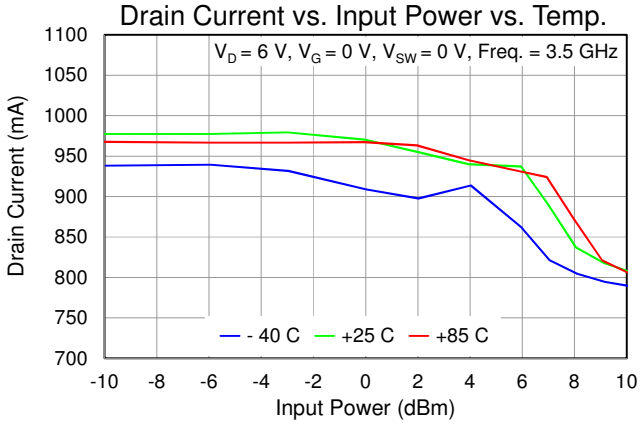
## Typical Performance – Large Signal (Pulsed)

Test conditions, unless otherwise noted: T = 25 °C, part mounted to EVB, Pulse Power: PW = 100 us, DC = 20%

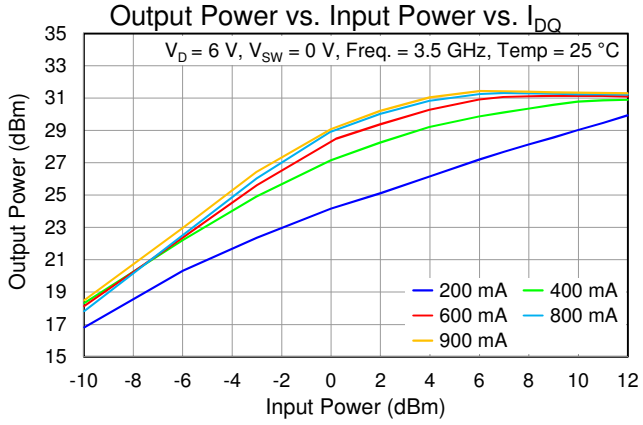
Power Gain vs. Input Power vs. Temp.



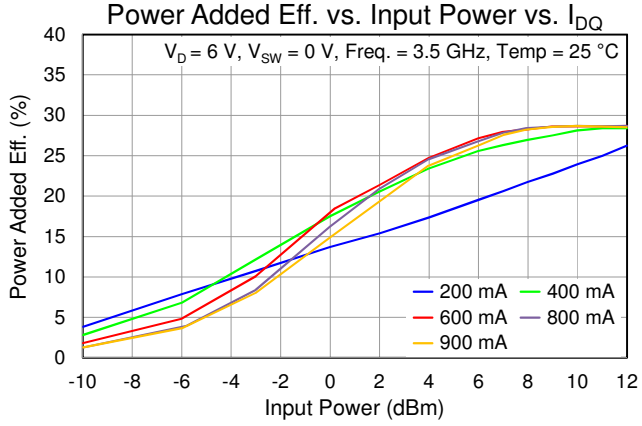

Drain Current vs. Input Power vs. Temp.



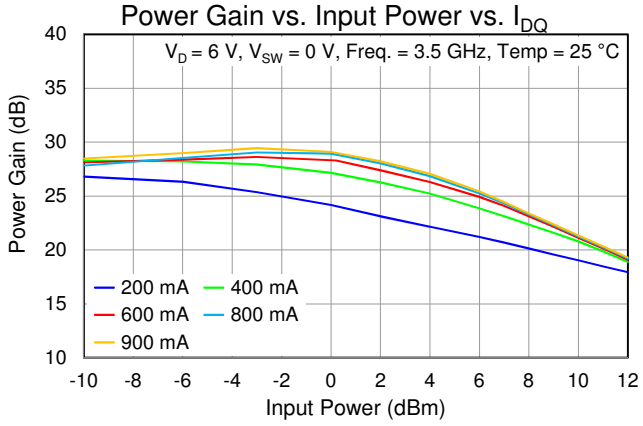

Output Power vs. Input Power vs. $I_{DQ}$



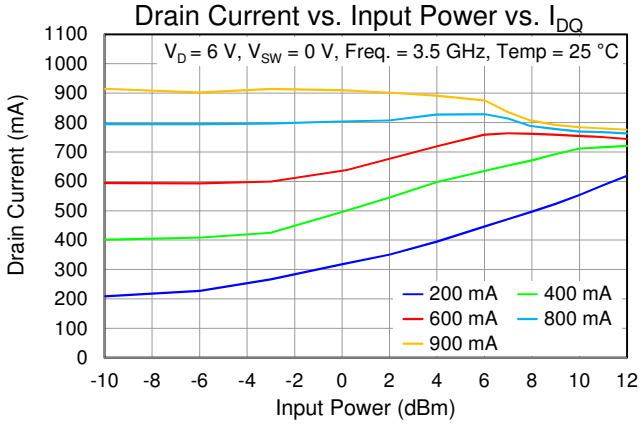

Power Added Eff. vs. Input Power vs. $I_{DQ}$




Power Gain vs. Input Power vs. $I_{DQ}$



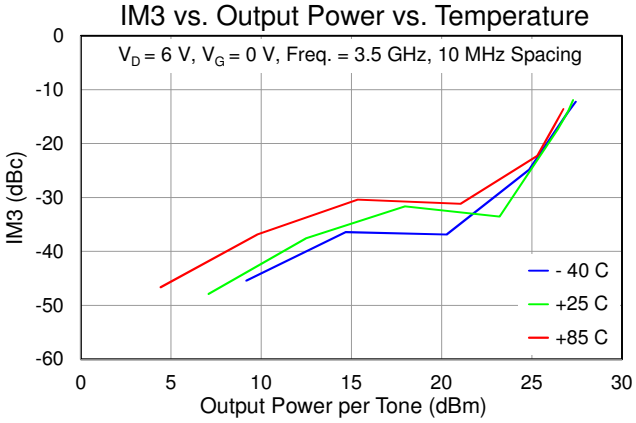

Drain Current vs. Input Power vs. $I_{DQ}$



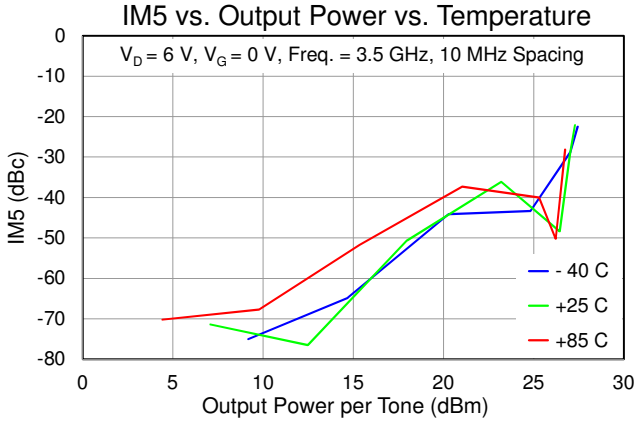
## Typical Performance - Linearity

Test conditions, unless otherwise noted: T = 25 °C, $V_{SW}$ = 0 V, part mounted to EVB

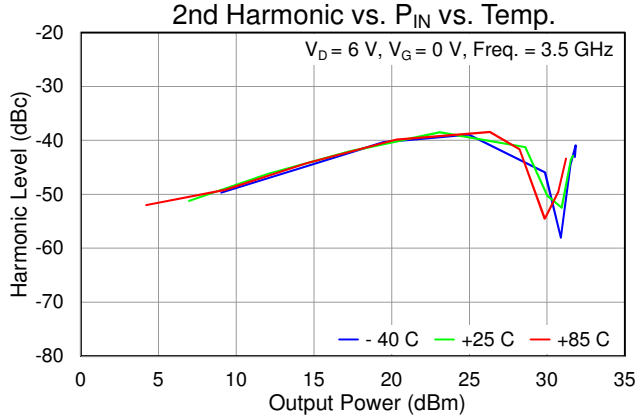
IM3 vs. Output Power vs. Temperature



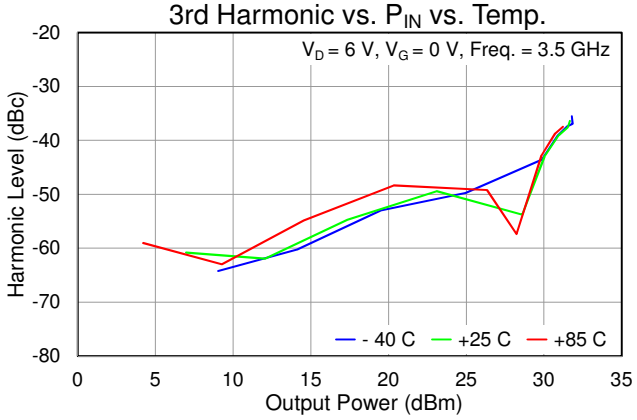

IM5 vs. Output Power vs. Temperature



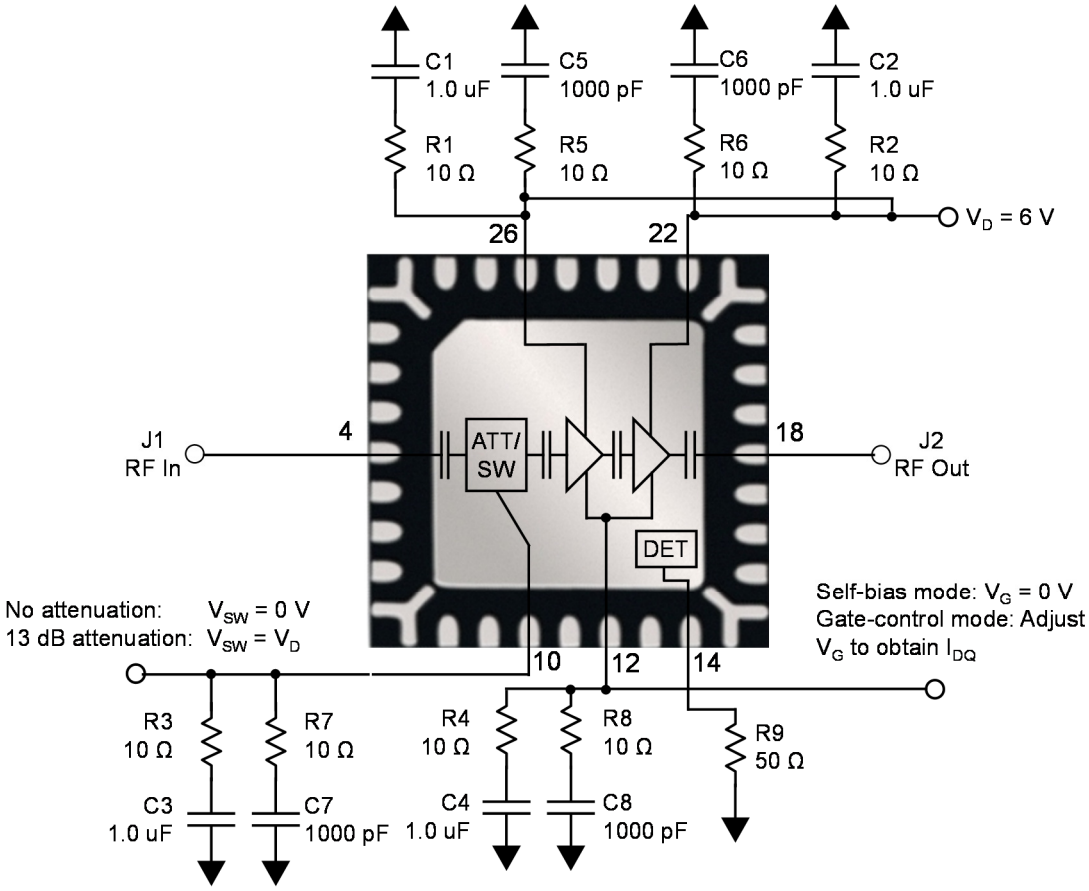

2nd Harmonic vs. $P_{IN}$ vs. Temp.




3rd Harmonic vs. $P_{IN}$ vs. Temp.



## Application Circuit




## Bias-up Procedure

1. Set $I_D$ limit to 1000 mA, $I_G$ limit to 12 mA
2. Self-biased mode: Set $V_G$ to 0 V
   Gate-control mode: Adjust $V_G$ to obtain desired $I_{DQ}$
3. Increase $V_D$ to +6 V
4. Apply RF signal

## Bias-down Procedure

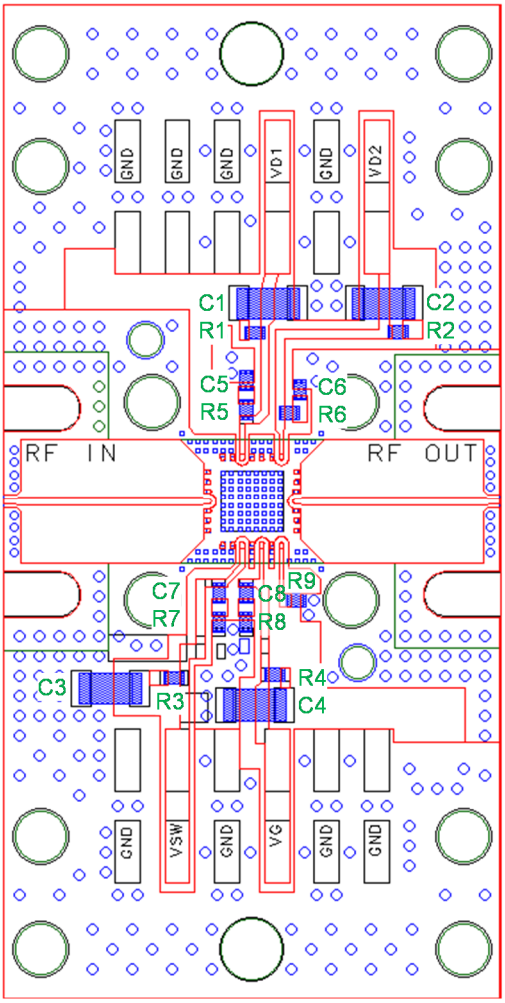
1. Turn off RF signal
2. Set $V_D$ to 0 V. Ensure $I_{DQ}$ ~ 0 mA
3. Turn off $V_D$ supply
4. Turn off $V_G$, $V_{SW}$ supply

## Applications Information

### Evaluation Board Layout

RF Layer is 0.008" thick Rogers Corp. RO4003C, εr = 3.38. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

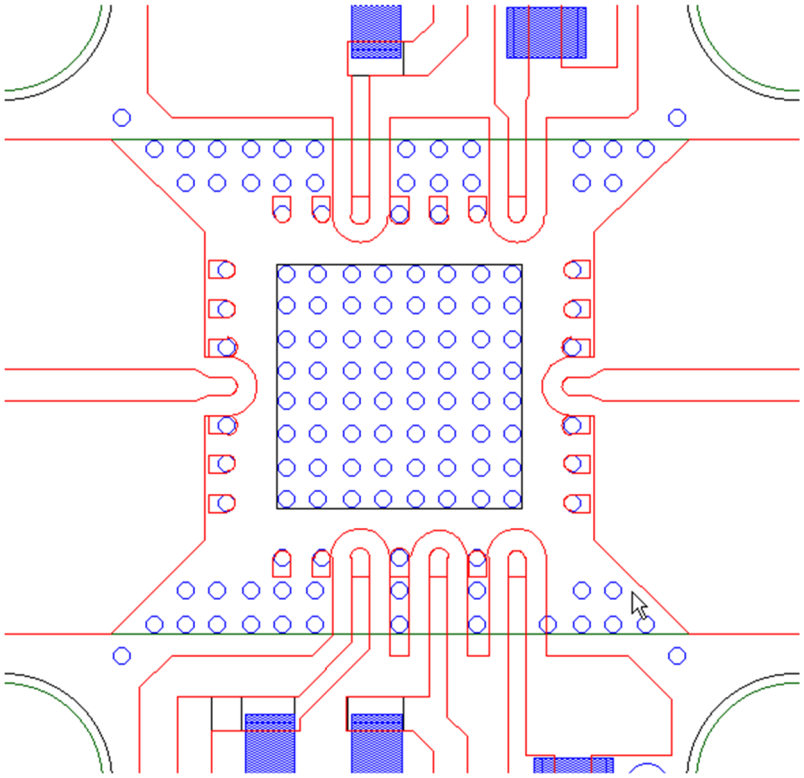
The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.




## Bill of Materials

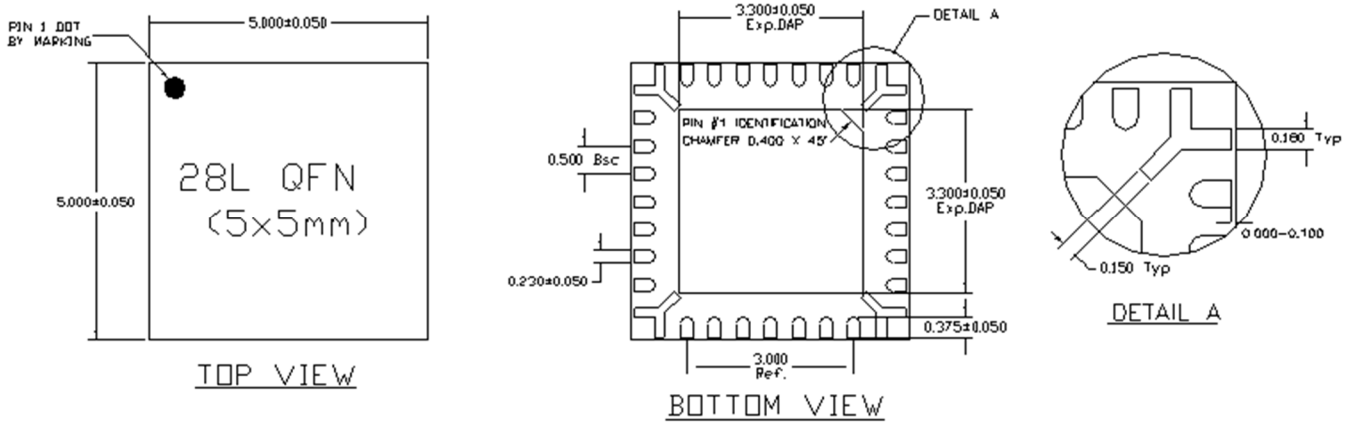
| Ref. Designation | Value | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| C1 – C4 | 1.0 uF | Cap., 50V, 10% X5R, 1206 case | Various | |
| C5 – C8 | 1000 pF | Cap., 50V, 10% X7R, 0402 case | Various | |
| R1 – R8 | 10 Ohms | Resistor, 0402 case | Various | |
| R9 | 50 Ohms | Resistor, 0402 case | Various | |

## Mounting Detail

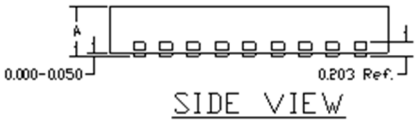


Note:
Multiple copper filled vias are preferred for optimum thermal performance and to minimize inductance to ground.

## Mechanical Information




| | | QFN |
|---|---|---|
| A | MAX. | 0.900 |
| | NOM. | 0.850 |
| | MIN. | 0.800 |

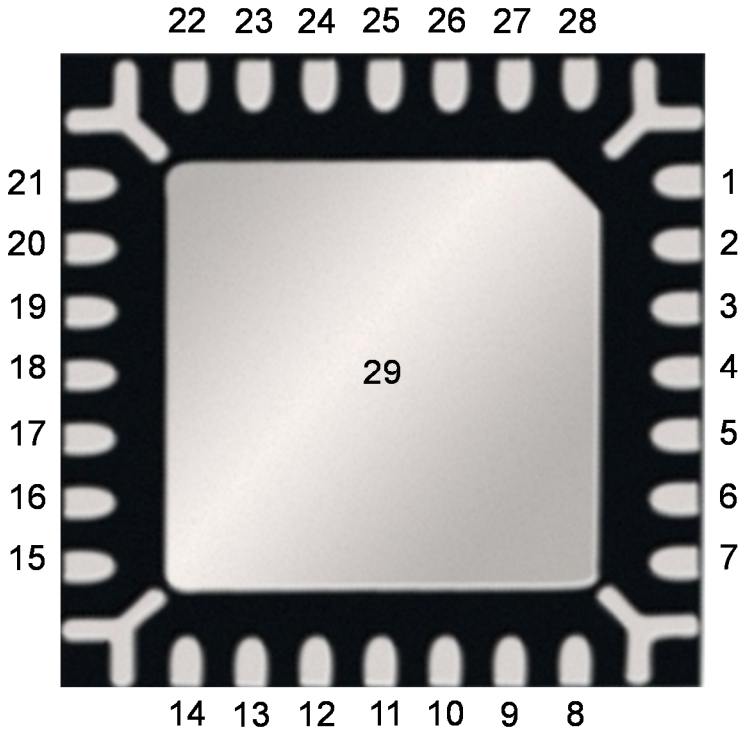



The TGA2731-SM will be marked with the “ZZZZ” and “YYWW” designators and a lot code marked below the part designator. Here, the “ZZZZ” will be “2731”. The “YY” represents the last two digits of the year the part was manufactured, the “WW” is the work week, and the “XXXX” is an auto-generated number.

This package is lead-free/RoHS-compliant. This package is compatible with both lead free and tin-lead soldering processes.

Dimensions are in millimeters.

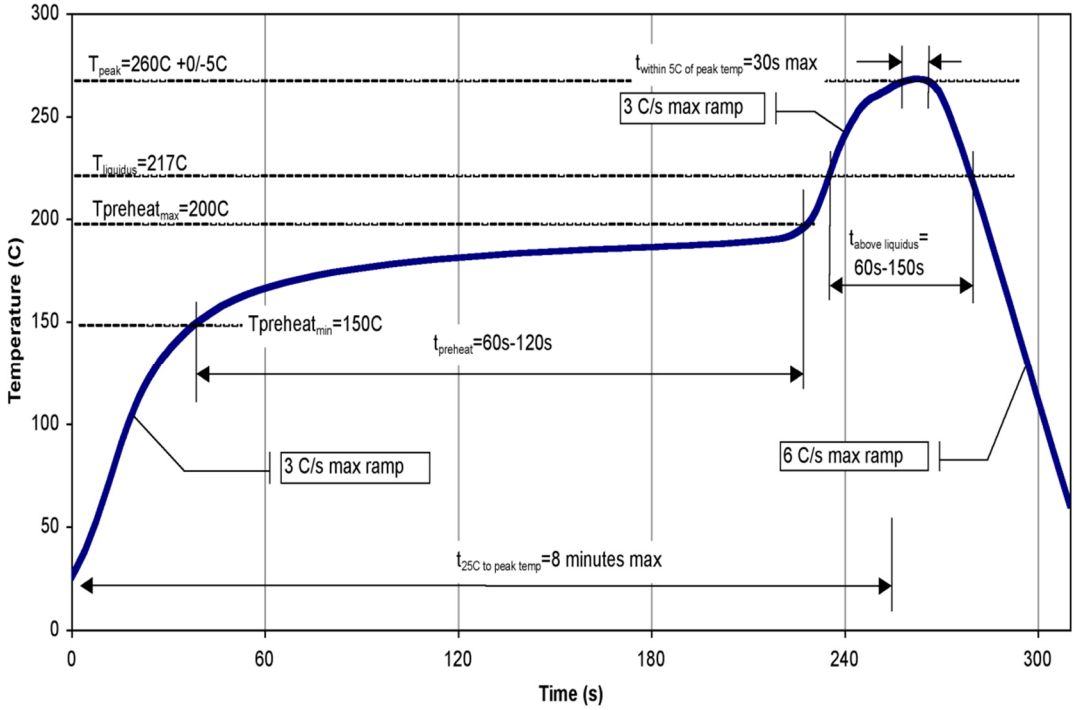
## Pad Description




**Bottom view of package base**

| Pin Number | Label | Description |
|---|---|---|
| 1-3, 5-9, 11 13, 15-17, 19-21, 23-25, 27-28 | No Connect | No internal connection. Pads on PCB should be grounded to improve RF isolation |
| 4 | RF Input | RF input, matched to 50 Ω, DC blocked |
| 10 | $V_{SW}$ | Input attenuator switch control voltage for gain control |
| 12 | $V_G$ | Gate voltage |
| 14 | Power Sample | Coupled output power |
| 18 | RF Output | RF output, matched to 50 Ω, DC blocked |
| 22 | $V_{D2}$ | Second stage drain voltage. Bias network required |
| 26 | $V_{D1}$ | First stage drain voltage. Bias network required |
| 29 | GND | Ground paddle; must be grounded using plated through/copper filled via holes on PCB to improve isolation and for heat sinking |

## Recommended Soldering Temperature Profile



## Product Compliance Information

### ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

### ECCN

US Department of Commerce: EAR99

### Solderability

Compatible with the latest version of J-STD-020 Lead free solder, 260 °C.

### MSL Rating

TBD at 260 °C convection reflow
The part is rated Moisture Sensitivity Level TBD
JEDEC standard IPC/JEDEC J-STD-020.

### RoHS-Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

**Web:** www.triquint.com **Tel:** +1.972.994.8465
**Email:** info-sales@tqs.com **Fax:** +1.972.994.8504

For technical questions and application information: **Email:** info-products@tqs.com

## Important Notice

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