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AC11657: Objective Specification
ACT11657: Preliminary Specification
Octal transceiver with 8-bit parity checker/generator

FEATURES

- 3-State outputs
- Combines '245 and '280 functions in one package
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11657 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11657 device is an octal transceiver featuring non-inverting buffers and an 8-bit parity generator/checker, and is intended for bus-oriented applications.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n	C_L = 50pF			5.3	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled		95	pF
			Disabled		21	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	V_{IO} = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

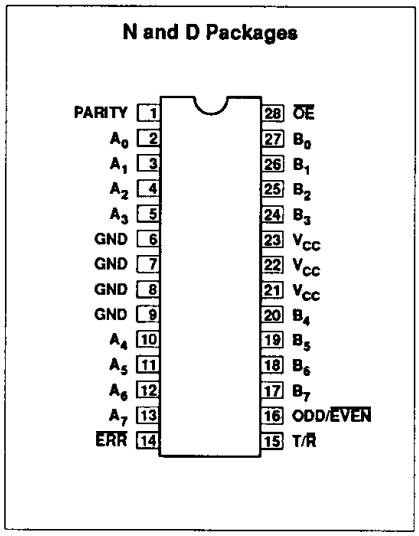
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

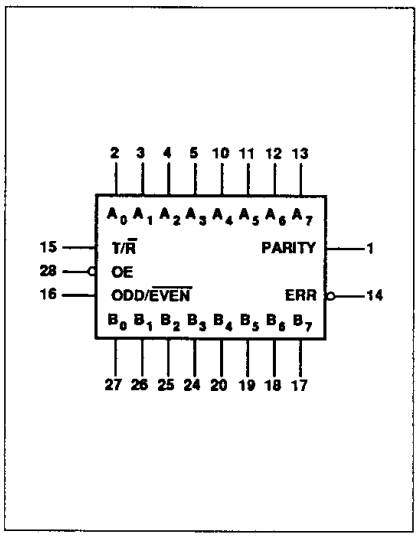
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11657N 74ACT11657N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11657D 74ACT11657D

PIN CONFIGURATION

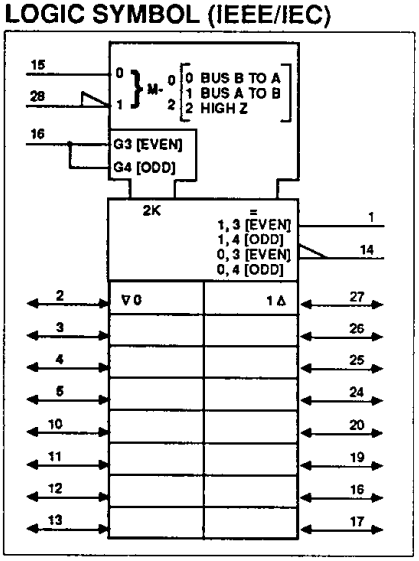
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from port A to B (T/$\overline{R}$ = High) and an input when receiving from port B to A (T/$\overline{R}$ = Low). When transmitting (T/$\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$ = Low) the B port is polled to determine the number of High bits.

If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERR}$ will be asserted Low, indicating an error.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	T/$\overline{R}$	Transmit/receive input
16	ODD/$\overline{EVEN}$	Parity select input
28	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A ports 3-State inputs/output
27, 26, 25, 24, 20, 19, 18, 17	B_0 - B_7	B ports 3-State inputs/output
1	PARITY	Parity input/output
14	$\overline{ERR}$	Error output
6, 7, 8, 9	GND	Ground (0V)
21, 22, 23	V_{CC}	Positive supply voltage

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1,3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

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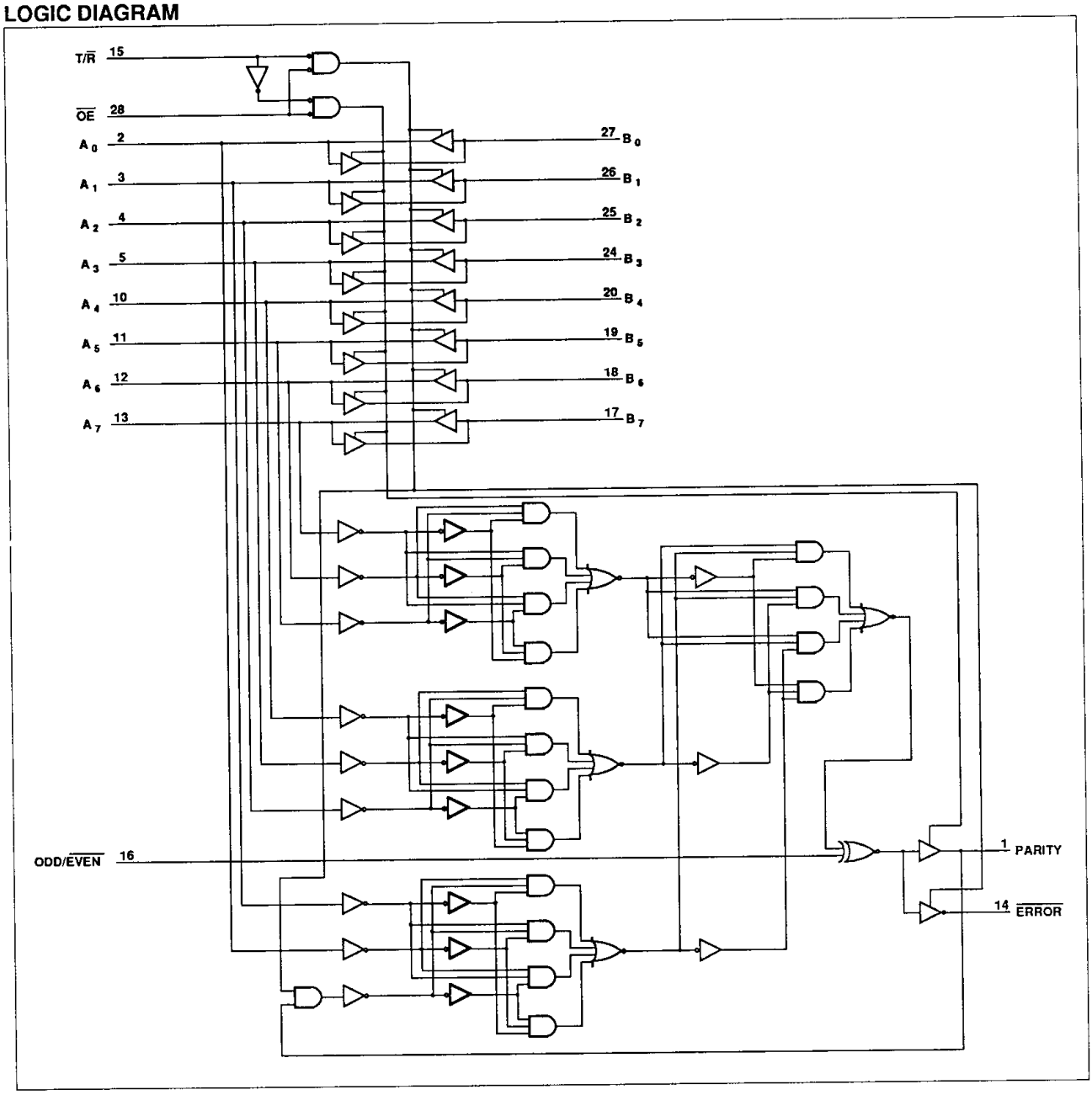
LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11657			74ACT11657			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{OE}$ only	0		10	0		10	ns/V
		All other inputs	0		5	0		5	
T_{amb}	Operating free-air temperature range		-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11657				74ACT11657				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4:94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11657					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A_n to B_n or B_n to A_n	1						ns
t_{PLH} t_{PHL}	Propagation delay, A_n to PARITY	1						ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{ODD/EVEN}$ to $\overline{PARITY}$, $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, B_n to $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{PARITY}$ to $\overline{ERROR}$	1						ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2						ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2						ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11657					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A_n to B_n or B_n to A_n	1						ns
t_{PLH} t_{PHL}	Propagation delay, A_n to PARITY	1						ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{ODD/EVEN}$ to $\overline{PARITY}$, $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, B_n to $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{PARITY}$ to $\overline{ERROR}$	1						ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2						ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2						ns

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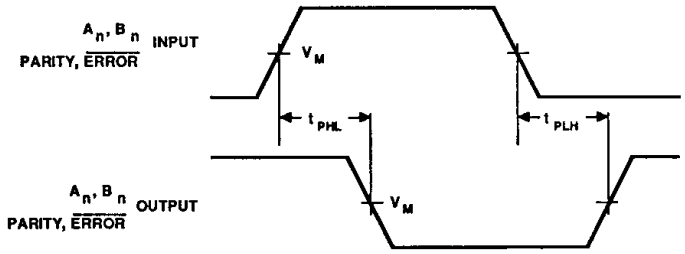
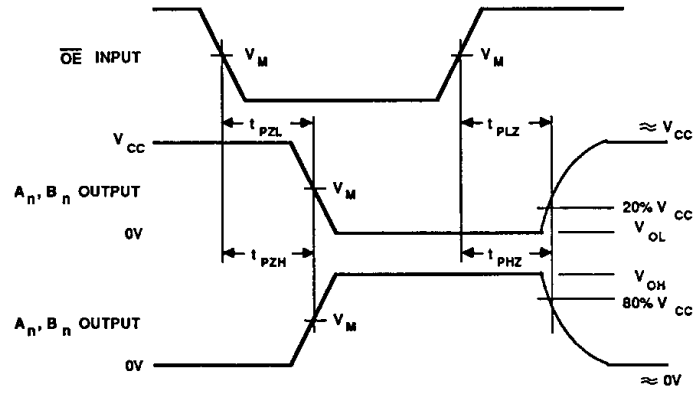
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11657					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A_n to B_n or B_n to A_n	1	3.2 2.2	5.5 5.1	6.9 7.2	3.2 2.2	7.6 7.8	ns
t_{PLH} t_{PHL}	Propagation delay, A_n to PARITY	1	3.6 4.0	7.5 8.1	10.3 10.7	3.6 4.0	11.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay, ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	1	2.8 3.1	6.0 6.4	7.8 8.3	2.8 3.1	8.7 9.1	ns
t_{PLH} t_{PHL}	Propagation delay, B_n to $\overline{ERROR}$	1	4.6 4.9	12.4 12.8	16.9 17.7	4.6 4.9	19.4 20.2	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{PARITY}$ to $\overline{ERROR}$	1	4.1 3.9	7.7 7.7	10.0 10.4	4.1 3.9	11.1 11.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	3.2 3.9	6.2 7.5	9.8 10.5	3.2 3.9	10.5 11.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	4.5 4.8	7.5 7.4	10.1 9.3	4.5 4.8	10.9 10.0	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n, B_n) to Output (B_n, A_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

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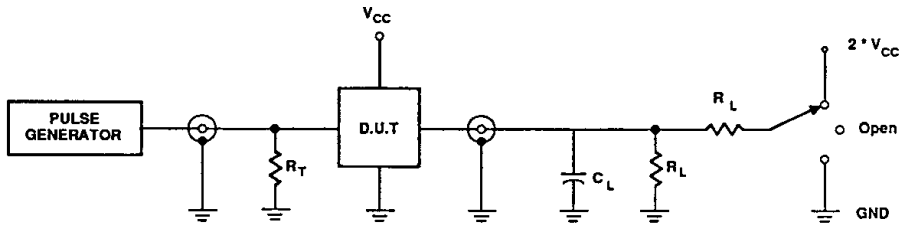
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns