iW1692

Low-Power Off-line Digital PWM Controller

1.0 Features

- Primary-side feedback eliminates opto-isolators and simplifies design
- Multi-mode operation for highest overall efficiency
- Built-in cable drop compensation
- Very tight output voltage regulation
- No external loop compensation components required
- Complies with CEC/EPA/IEC no load power consumption and average efficiency regulations
- Built-in output constant-current control with primary-side feedback
- Low start-up current (10 µA typical)
- Built-in soft start
- Built-in short circuit protection
- AC line under/overvoltage and output overvoltage protection
- 40 kHz PWM switching frequency
- PFM operation at light load
- Built-in I_{SENSE} pin short protection
- Space-saving SOT-23 package

2.0 Description

The iW1692 is a high performance AC/DC power supply controller which uses digital control technology to build peak current mode PWM flyback power supplies. The device provides high efficiency along with a number of key built-in protection features while minimizing the external component count and bill of material cost. The iW1692 removes the need for secondary feedback circuitry while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range.

The low start-up power and PFM operation at light load ensure that the iW1692 is ideal for applications targeting the newest regulatory standards for standby power.

3.0 Applications

- Low power AC/DC adapter/chargers for cell phones, PDAs, digital still cameras
- Standby supplies for televisions, DVDs, set-top boxes and other consumer electronics

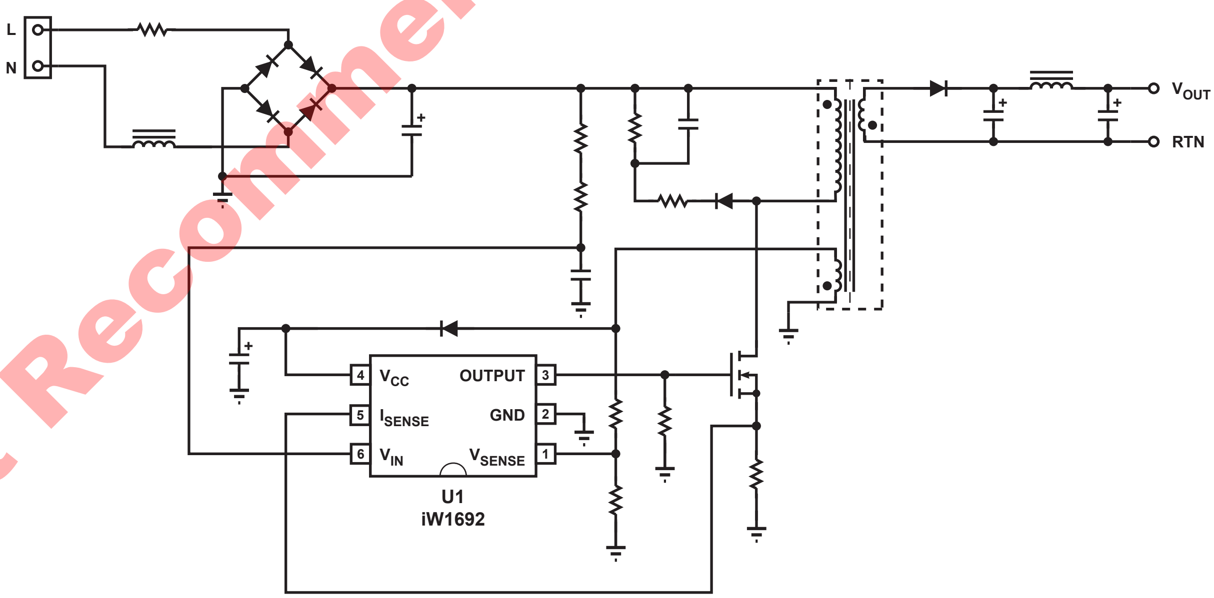
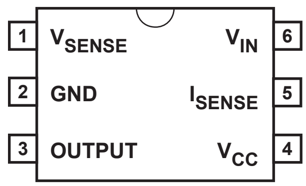


Figure 2.0.1 iW1692 Typical Application Circuit

4.0 Pinout Description

iW1692



Pin #	Name	Type	Pin Description
1	V_{SENSE}	Input	Voltage sense input from the auxiliary winding.
2	GND	Ground	Ground connection.
3	OUTPUT	Output	Gate drive output for the external power MOSFET switch.
4	V_{CC}	Input	Supply voltage.
5	I_{SENSE}	Input	Primary current sense. Used for cycle-by-cycle peak current control and limit.
6	V_{IN}	Input	Senses average rectified input voltage.

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parametric values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 4, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18	V
DC supply current at V_{CC} pin	I_{CC}	20	mA
Output (pin 3)		-0.3 to 18	V
V_{SENSE} input (pin 1, I_{Vsense} ≤ 10 mA)		-0.7 to 4.0	V
I_{SENSE} input (pin 5)		-0.3 to 4.0	V
V_{IN} input (pin 6)		-0.3 to 18	V
Power dissipation at T_A ≤ 25°C	P_D	400	mW
Maximum junction temperature	$T_{J\,(MAX)}$	125	°C
Storage temperature	T_{STG}	–65 to 150	°C
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	°C
Thermal resistance junction-to-ambient	θ_{JA}	240	°C/W
ESD rating per JEDEC JESD22-A114 (HBM)		2,000	V
Latch-Up test per JEDEC 78		±100	mA

6.0 Electrical Characteristics

V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} SECTION (Pin 6)						
Start-up voltage threshold	V_{INST}	T_A= 25°C, positive edge	366	407	448	mV
Start-up current	I_{INST}	V_{IN} = 10 V, C_{VCC} = 10 µF R_{OUTPUT} = 10 kΩ to GND		10	15	µA
Shutdown low voltage threshold	V_{UVDC}	T_A= 25°C	216	240	264	mV
Shutdown high voltage threshold	V_{OVDC}	T_A= 25°C	1.834	1.988	2.123	V
Input impedance	Z_{IN}	After start-up		20		kΩ
V_{SENSE} SECTION (Pin 1)						
Input leakage current	I_{BVS}	V_{SENSE} = 2 V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A=25°C, negative edge	1.523	1.538	1.553	V
Output OVP threshold (1692-00)	$V_{SENSE(MAX)}$	T_A=25°C, negative edge	1.649	1.700	1.751	V
OUTPUT SECTION (Pin 3)						
Output low level ON-resistance	$R_{DS(ON)LO}$	I_{SINK} = 5 mA		45	100	Ω
Output high level ON-resistance	$R_{DS(ON)HI}$	I_{SOURCE} = 5 mA		65	100	Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330 pF 10% to 90%		40	75	ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330 pF 90% to 10%		40	75	ns
Output switching frequency	f_S	I_{LOAD} > 15% of maximum	36	40	44	kHz
V_{CC} SECTION (Pin 4)						
Maximum operating voltage	$V_{CC(MAX)}$				16	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	11.0	12.0	13.2	V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	5.5	6.0	6.6	V
Operating current	I_{CCQ}	C_L = 330 pF, V_{SENSE} = 1.5 V		2.5	3.5	mA
I_{SENSE} SECTION (Pin 5)						
Peak limit threshold	V_{PEAK}			1000		mV
CC limit threshold	$V_{CC\text{-}TH}$			900		mV

Notes:

Note 1. Adjust V_{CC} above the start-up threshold before setting at 12 V.

Note 2. These parameters are not 100% tested, guaranteed by design and characterization.

7.0 Typical Performance Characteristics

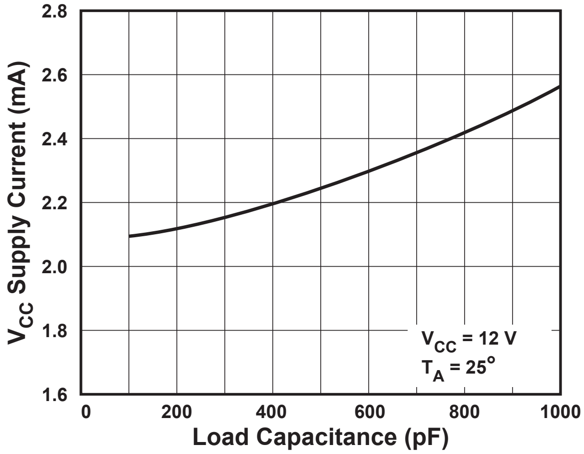


Figure 7.0.1 Supply Current vs. Load Capacitance

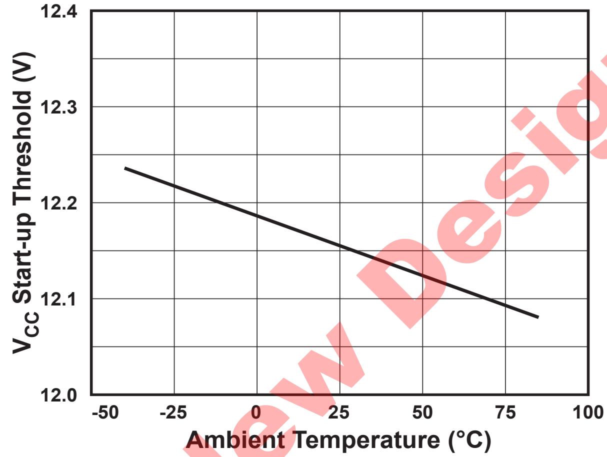


Figure 7.0.3 Start-Up Threshold vs. Temperature

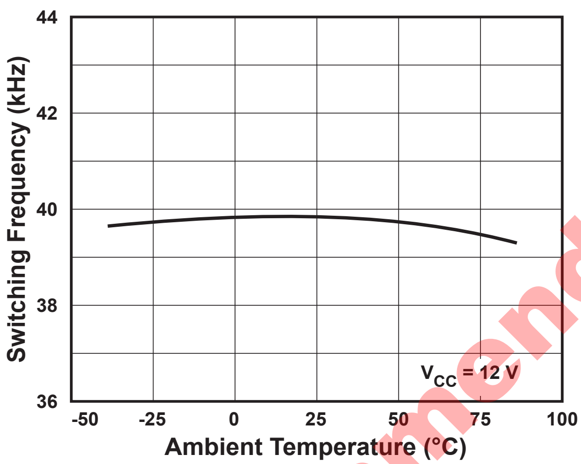


Figure 7.0.2 Switching Frequency vs. Temperature

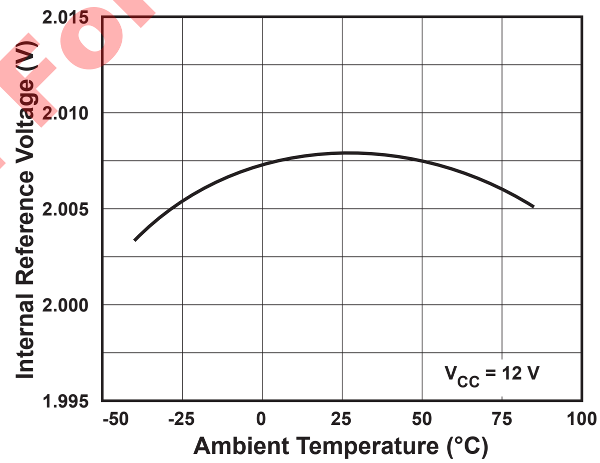


Figure 7.0.4 Internal Reference vs. Temperature

8.0 Functional Block Diagram

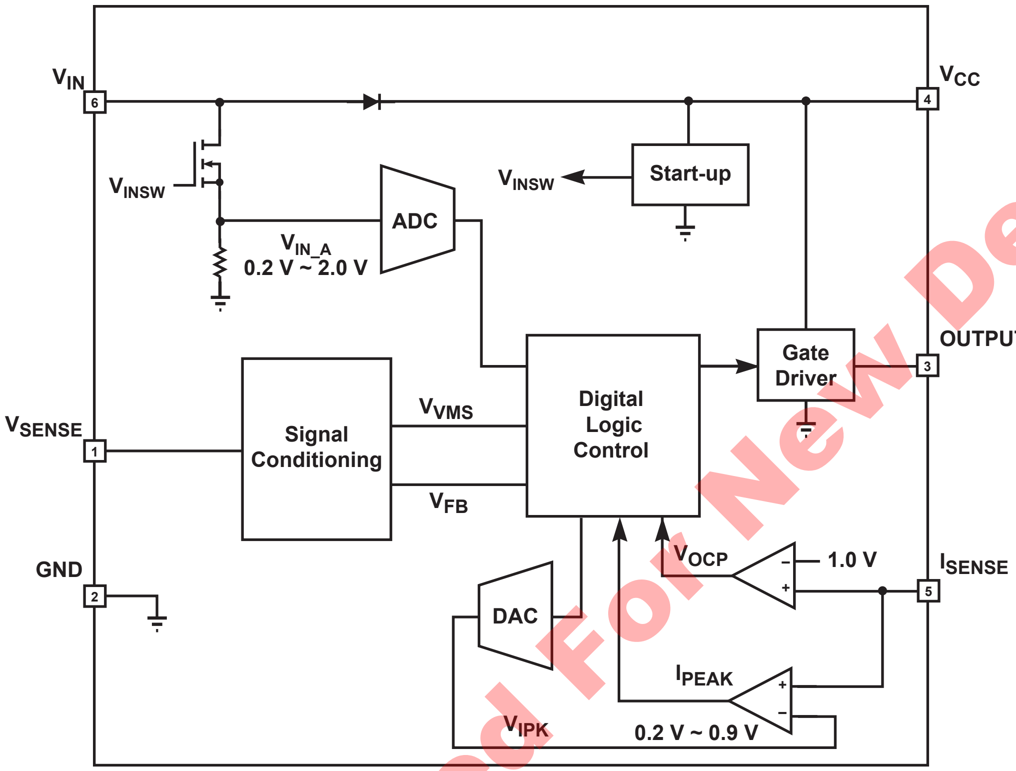


Figure 8.0.1 iW1692 Functional Block Diagram

9.0 Theory of Operation

The iW1692 is a digital controller which uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at heavy load and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, iWatt's digital control technology enables fast dynamic response, tight output regulation, and full featured circuit protection with primary-side control.

Referring to the block diagram in Figure 8.0.1, the digital logic control generates the switching on-time and off-time information based on the line voltage and the output voltage feedback signal. The system loop is internally compensated inside the digital logic control, and no external analog components are required for loop compensation. The iW1692 uses an advanced digital control algorithm to reduce system design time and improve reliability.

Furthermore, accurate secondary constant-current operation is achieved without the need for any secondary-side sense and control circuits.

The iW1692 uses PWM mode control at higher output power levels and switches to PFM mode at light load to minimize power dissipation. Additional built-in protection features include overvoltage protection (OVP), output short circuit protection (SCP), AC low line brown out, over current protection, single pin fault protection and I_{SENSE} fault detection.

iWatt's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control.

9.1 Pin Detail

Pin 1 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 2 – GND

Analog, digital and power ground.

Pin 3 – OUTPUT

Gate drive signal for the external power MOSFET switch.

Pin 4 – V_{CC}

Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 12 V (typical) and shuts-down when the V_{CC} voltage is below 6 V (typical). A 100 nF decoupling capacitor should be connected between the V_{CC} pin and GND.

Pin 5 – I_{SENSE}

Primary current sense.

Pin 6 – V_{IN}

Sense signal input representing the instantaneous rectified line voltage. V_{IN} is used for line regulation. The internal impedanace is 20 kΩ and the scale factor is 0.0043. It also provides input undervoltage and overvoltage protection. This pin also provides the supply current to the IC during start-up.

9.2 Start-up

Prior to start-up the V_{IN} pin charges up the V_{CC} capacitor, through the diode between V_{IN} and V_{CC}. When V_{CC} is fully charged to a voltage higher than $V_{CC(ST)}$ threshold, then the V_{IN_SW} turns on and the analog-to-digital converter begins to sense the input voltage. The iW1692 commences soft-start function as soon as the voltage on V_{IN} pin is above V_{INST}.

The iW1692 incorporates an internal soft-start function. The soft-start time is set at 3.0 ms. Once the V_{IN} pin voltage has reached its turn-on threshold, the iW1692 starts switching, but limits the on-time to a percentage of the maximum on-time. During the first 1 ms, the on-time is limited to 25%. During the next 1 ms, the on-time is limited to 50% and during the last 1 ms, the on-time is limited to 75%.

If at any time the V_{CC} voltage drops below $V_{CC(UVL)}$ threshold then all the digital logic is fully reset. At this time the V_{IN_SW} switches off so that the V_{CC} capacitor can be charged up again.

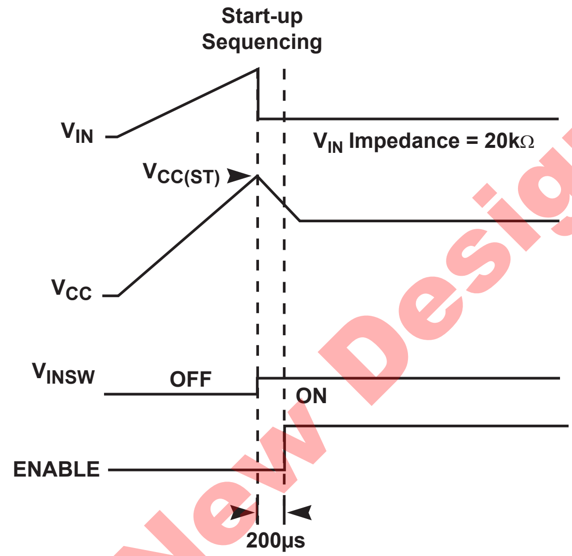


Figure 9.2.1 Start-up Sequencing Diagram

9.3 Understanding Primary Feedback

Figure 9.3.1 illustrates a simplified flyback converter. When the switch Q1 conducts during t_{ON}, the current i_g is directly drawn from rectified sinusoid v_g. The energy E_g is stored in the primary winding. The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

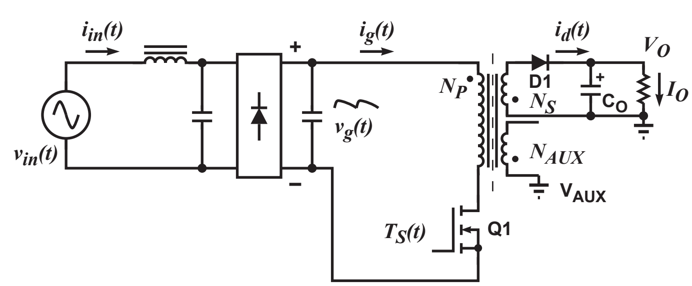


Figure 9.3.1 Simplified Flyback Converter

In order to regulate the output voltage within a tight specification, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q_1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across the primary winding is $v_g(t)$, assuming the voltage dropped across Q_1 is zero. The current in Q_1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \tag{9.1}$$

At the end of on-time, the current has ramped up to:

$$i_g(t) = \frac{v_g(t) \times t_{ON}(t)}{L_M} \tag{9.2}$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_g(t)^2 \tag{9.3}$$

When Q_1 turns off, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off, the primary current transfers to the secondary at an amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_g(t) \tag{9.4}$$

Assuming the secondary winding is master, the auxiliary winding is slave.

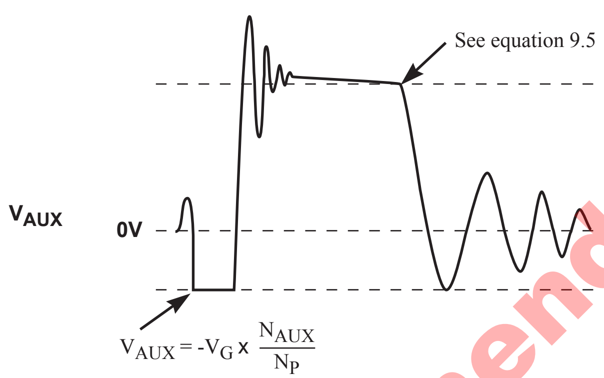


Figure 9.3.2 Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \tag{9.5}$$

and reflects the output voltage as shown in Figure 9.3.2.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is small.

The real-time waveform analyzer in the iW1692 reads this information cycle by cycle and then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage and is used to regulate the output voltage.

9.4 Understanding CC and CV mode

The constant current mode (CC mode) is useful in battery charging applications. During this mode of operation the iW1692 will regulate the output current at a constant maximum level regardless of the output voltage drop, while avoiding continuous conduction mode.

To achieve this regulation the iW1692 senses the load current indirectly through the primary current. The primary current is detected by the I_{SENSE} pin through a resistor from the MOSFET source to ground (R_{SS}). This resistor value is given by:

$$R_{SS} = \frac{N \times K_C}{2 \times I_{OUTMAX}} \tag{9.6}$$

N is the ratio of primary turns to secondary turns of the transformer and K_C is given as 0.264 V.

9.5 Constant Voltage Operation

After soft-start is completed, the digital control block measures the output conditions. If the I_{SENSE} signal is not consistently over 0.9 V, then the device will operate in constant voltage mode.

If no voltage is detected on V_{SENSE} after 20 pulses, it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1692 shuts down.

As long as calculated T_{ON} for CV is less than the T_{ON} in CC the IC operates in constant voltage mode.

9.6 Constant Current Operation

The iW1692 has been designed to work in constant-current mode for battery charging applications. If the output voltage drops, but does not go below 20% of the nominal designed value, the device operates in this mode.

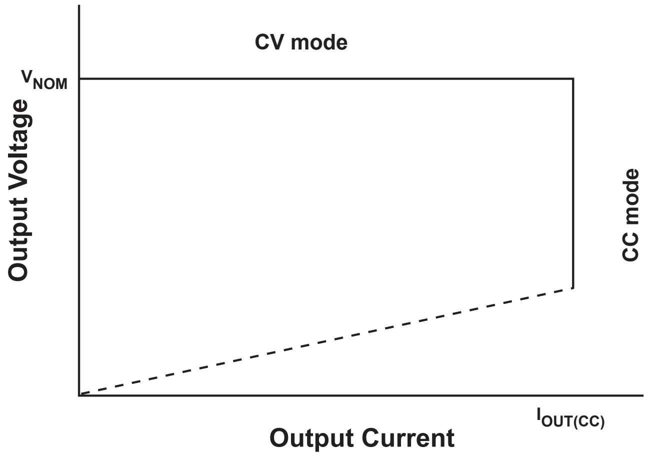


Figure 9.6.1 Modes of operation

9.7 Variable Frequency Mode

The iW1692 is designed to operate in discontinuous conduction (DCM) mode at a fixed frequency of 40 kHz in both CC and CV modes. To avoid operation in continuous conduction (CCM) mode, the iW1692 checks for the falling edge of the V_{SENSE} input on every cycle. If a falling edge of V_{SENSE} is not detected during the normal 25μs period, the switching period is extended until the falling edge V_{SENSE} does occur. If the switching period reaches 75μs without V_{SENSE} being detected, the iW1692 immediately shuts off.

9.8 PFM Mode at Light Load

The iW1692 operates in a fixed frequency PWM mode when I_{OUT} is greater than approximately 5% of the specified maximum load current. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased. At the moment that t_{ON} drops below t_{ON_MIN}, the controller transitions to Pulse Frequency Modulation (PFM) mode. Thereafter, the on-time is modulated by the line voltage and the off-time is modulated by the load current. The device automatically returns to PWM mode when the load current increases.

9.9 Internal Loop Compensation

The iW1692 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. The loop stability is guaranteed by design to provide at least 45 degrees of phase margin and –20dB of gain margin.

9.10 Voltage Protection Functions

The iW1692 includes functions that protect against input and output overvoltage.

The input voltage is monitored by the V_{IN} pin and the output voltage is monitored by the V_{SENSE} pin. If the voltage at these pins exceed their undervoltage or overvoltage thresholds for more than 6 cycles, the iW1692 shuts-down immediately. However, the IC remains biased which discharges the V_{CC} supply. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up, but does not fully start-up until the fault condition is removed.

The output voltage can be high enough to damage the output capacitor when the feedback loop is broken. The iW1692 uses the primary feedback only with no secondary feedback loop. When the V_{SENSE} pin is shorted to GND (by shorting/open sense resistor). The controller will shut off with 6 consecutive pulses after start-up.

9.11 Cable Drop Compensation

The iW1692-30 incorporates an innovative method to compensate for any IR drop in the secondary circuitry including cable and cable connector. A 5 W AC adapter with 5 VDC output has 6% deviation at 1 A load current due to the drop across the DC cable without cable compensation. The iW1692-30 cancels this error by providing a voltage offset to the feedback signal based on the amount of load current detected. The iW1692-30 has 300mV of cable drop compensation at maximum current. The iW1692-00 does not include any cable drop compensation.

10.0 Design Example

10.1 Design Procedure

This design example gives the procedure for a flyback converter using iW1692. Refer to figure 12.0.1 for the application circuit. The design objectives for this adapter are given in table 10.1. It meets UL, IEC, and CEC requirements.

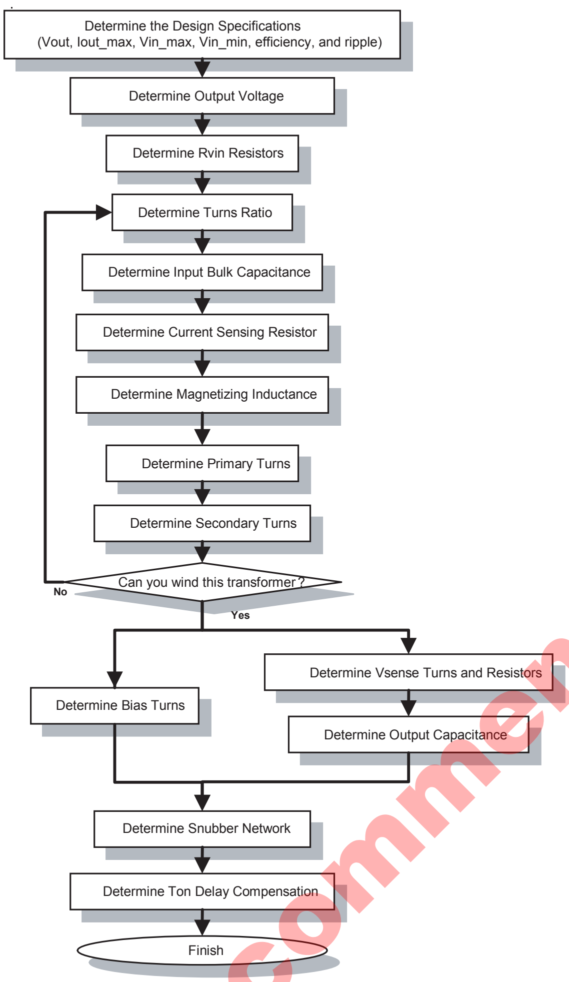


Figure 10.0.1 iW1692 Design Flow Chart

Parameter	Symbol	Range
Input Voltage	V_{IN}	85 - 264 V_{RMS}
Frequency	f_{IN}	47 - 64 Hz
No Load Input	P_{IN}	200 mW
Output Voltage	V_{OUT_PCB}	4.95 - 5.05 V
Output Current	I_{OUT}	1 A
Output Ripple	V_{RIPPLE}	<100 mV
Power Out	P_{OUT}	5 W
CEC Efficiency	η	65%

Table 10.1 iW1692 Design Specification Table

10.2 Output Voltage

Use equation 10.1 for V_{OUT} in the following equations, where V_{FD} is the forward voltage of the output diode:

$$V_{OUT} = V_{OUT(PCB)} + V_{FD} \tag{10.1}$$

Since no cable is used and the forward drop on the output diode (V_{FD}) is 500 mV, V_{OUT} is 5.0 V.

10.3 Input Selection

V_{IN} resistors are chosen primarily to scale down the input voltage for the IC. The scale factor for the input voltage in the IC is 0.0043 and the internal impedance of this pin is 20 kΩ. Therefore, the V_{IN} resistors should equate to:

$$R_{Vin} = \frac{20k\Omega}{0.0043} - 20k\Omega = 4.63M\Omega \tag{10.2}$$

From equation 10.2, ideally R_{VIN} should be 4.63 MΩ because R10 and R11 add up to approximately 4.6 MΩ. By selecting the value of R_{VIN}, the $(V_{IN} \cdot T_{ON})_{MAX\_LIMIT}$ and $(V_{IN} \cdot T_{ON})_{PFM}$ are determined:

$$(V_{IN} \cdot T_{ON})_{MAX\_LIMIT} = 0.0043 \times \frac{900V \cdot \mu s}{\left(\frac{20k\Omega}{R_{Vin} + 20k\Omega}\right)} \tag{10.3}$$

$$(V_{IN} \cdot T_{ON})_{PFM} = 0.0043 \times \frac{185V \cdot \mu s}{\left(\frac{20k\Omega}{R_{Vin} + 20k\Omega}\right)} \tag{10.4}$$

Keep in mind by changing R_{VIN} to be something other than 4.63 MΩ the minimum and maximum input voltage for start-up will also change.

Since the iW1692 uses the exact scaled value of V_{IN} for its calculations, C6 should be included to filter out any noise that may appear on the V_{IN} signal. This is especially important for line-in surge conditions.

10.4 Turns Ratio

The maximum allowable turns ratio between the primary and secondary winding is determined by the minimum detectable reset time of the transformer, during PFM mode

$$N_{tr\_MAX} = \frac{(V_{IN} \times T_{ON})_{PFM}}{T_{RESET\_MIN} \times V_{OUT}} \quad (10.5)$$

To avoid continuous conduction the turns ratio must be high enough so that T_{RESET} does not exceed $T_{PERIOD} - T_{ON} - T_{DEAD}$. T_{PERIOD} is given by the PWM switching frequency of 40 kHz. T_{RESET_MAX} is given by:

$$T_{RESET\_MAX} = T_{PERIOD} - T_{ON\_MAX} - T_{DEAD} \quad (10.6)$$

Thus, the minimum turns ratio is given by:

$$N_{tr\_MIN} = \frac{(V_{IN} \times T_{ON})_{MAX}}{T_{RESET\_MAX} \times V_{OUT}} \quad (10.7)$$

$(V_{IN} \times T_{ON})_{PFM}$ is limited by the iW1692 to be 185 V·µs, and T_{RESET_MIN} is required by the IC to be 2.3 µs.

$$N_{tr\_MAX} = \frac{185V \cdot \mu s}{2.3\mu s \times 5.5V} = 15$$

The product of V_{IN} and T_{ON} is typically chosen by equation 10.8 for CC limit performance. For this example we choose 750 V·µs.

$$700V \cdot \mu s < (V_{IN} \times T_{ON})_{MAX} < 850V \cdot \mu s \quad (10.8)$$

Assuming V_{INDC_MIN} is 77.0 V, then

$$T_{ON(\max)} = \frac{(V_{IN} \cdot T_{ON})_{\max}}{V_{INDC(\min)}} \quad (10.9)$$

$$T_{ON(\max)} = \frac{750V \cdot \mu s}{77V} = 9.7\mu s$$

T_{DEAD} is estimated to be about 4.8 µs, solving for the minimum turns ratio yields.

$$T_{RESET\_MAX} = 25\mu s - 9.7\mu s - 4.8\mu s$$

$$T_{RESET\_MAX} = 10.5\mu s$$

$$N_{tr\_MIN} = \frac{750V \cdot \mu \sec}{(10.5\mu \sec) \times 5.5V} = 13$$

Pick a number between the maximum and minimum turns ratio; in the example the turn ratio is 13. A turns ratio in the range of 11 to 15 is suggested for optimal performance.

10.5 Input Bulk Capacitor

The input bulk capacitance (C1 // C2) is chosen to maintain enough input power to sustain constant output power even as the input voltage is dropping. In order for this to be true the minimum total input bulk capacitance must be:

$$C_{BULK} = \frac{2 \times P_{IN} \times \left[0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{INDC(\min)}}{\sqrt{2} \times V_{INAC(\min)}}\right)\right]}{\left[2 \times V_{INAC(\min)}^2 - V_{INDC(\min)}^2\right] \times f_{line}} \quad (10.10)$$

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta_{\text{power supply}}}$$

Assume $\eta_{\text{power supply}} = 72\%$

$$P_{IN} = \frac{5.5V \times 1A}{72\%} = 7.333W$$

From this result we can now get V_{INDC_MIN} with 77.0 V into equation 10.10.

$$\frac{2 \times 7.333W \times \left[0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{77V}{\sqrt{2} \times 85Vac}\right)\right]}{\left(2 \times 85^2 - 77^2\right) \times 47Hz} = 13.26\mu F$$

Increase the value of C1 // C2 to account for efficiency losses. For this example, 13.6 µF is chosen.

10.6 Current Sense Resistor

The I_{SENSE} resistor determines the maximum current output of the power supply. The output current of the power supply is determined by:

$$I_{OUT} = \frac{1}{2} \times N_{TR} \times I_{PRI\_PK} \times \frac{T_{RESET}}{T_{PERIOD}} \times \eta_X \quad (10.11)$$

η_X is the transformer conversion efficiency.

When the maximum current output is achieved the voltage seen on the I_{SENSE} pin (V_{ISENSE}) should reach its maximum. Thus, at constant current limit:

$$I_{PRI\_PK} = \frac{V_{Isense\_CC}}{R_{Isense}} \tag{10.12}$$

Substituting this into equation 10.11 gives:

$$V_{Isense(CC)} = \frac{2 \times I_{OUT} \times R_{Isense}}{N_{TR} \times \eta_X} \times \frac{T_{PERIOD}}{T_{RESET}} \tag{10.13}$$

During constant current mode, where output current is at its maximum, the first term in Equation 10.13 is constant. Therefore, we can call this K_C. Substituting this back into equation 10.13 we get:

$$V_{Isense\_CC} = \frac{T_{PERIOD}}{T_{RESET}} \times K_C \tag{10.14}$$

For iW1692 K_C is 0.264 V, therefore R_{Isense} depends on the maximum output current by:

$$R_{Isense} = \frac{N_{tr} \times K_C}{2 \times I_{OUT}} \times \eta_x \tag{10.15}$$

Using this equation and N_{tr} from section 10.4 assume η_X is 87%:

$$R_{Isense} = \frac{13 \times 0.264V}{2 \times 1A} \times 87\% = 1.5\Omega$$

We recommend using ±1% tolerance resistors for R_{Isense}.

10.7 Magenitizing Inductance

A feature of the iW1692 is the lack of dependence on the magnetizing inductance for the CC curve.

Although the constant current limit does not depend on the magnetizing inductance, there are still restrictions on the magnetizing inductance. The maximum L_M is limited by the amount of power that needs to come out of the transformer in order for the power supply to regulate. This is given by:

$$L'_{M\_MAX} = \frac{(V_{IN} \cdot T_{ON})^2_{\max} \times 40kHz}{2 \times P_{XFMR\_MAX}}$$
$$P_{XFMR\_MAX} = \frac{V_{OUT} \times I_{OUT}}{\eta_X} \tag{10.16}$$

The minimum L_M is limited by the maximum allowable primary peak current (I_{PRI_PK}). 0.9 V on the I_{SENSE} pin should correspond to the maximum allowable primary peak current. Therefore, the maximum primary peak current is:

$$I_{PRI\_PK} < \frac{0.9V}{R_{Isense}} \tag{10.17}$$

Thus, L_M is limited by:

$$L_{M\_MIN} = \frac{(V_{IN} \cdot T_{ON})_{MAX}}{0.9V/R_{Isense}} \tag{10.18}$$

There is also a lower limit on I_{SENSE} signal of 0.2 V. This gives a second maximum value on L_M; compare this with the value obtained from equation 10.16 and pick the smaller of the two values.

$$L_{M\_MAX} = \frac{2 \times P_{XFMR\_MAX} \times R^2_{Isense}}{(0.2V)^2 \times 40kHz} \tag{10.19}$$

We can obtain the amount of power that needs to come out of the transformer as:

$$P_{XFMR\_MAX} = \frac{5.5V \times 1A}{87\%} = 6.332W$$

Substituting this into equation 10.16 we get:

$$L'_{M\_MAX} = \frac{(750V \cdot \mu s)^2 \times 40kHz}{2 \times 6.322W} = 1.78mH$$

To get the minimum value of the primary inductance, use the value for R_{ISENSE} from section 10.6.

$$I_{PRI\_PK} < \frac{0.9V}{1.5\Omega} = .6A$$

Substituting this primary peak current into equation 10.18:

$$L_{M\_MIN} = \frac{750V \cdot \mu\sec}{0.9V/1.5\Omega} = 1.25mH$$

Choose a primary inductance somewhere between 1.78 mH and 1.42 mH; we chose 1.5 mH.

10.8 Primary Winding

In order to keep the transformer from saturation, the maximum flux density must not be exceeded. Therefore the minimum primary winding on the transformer must meet:

$$N_{PRI} \geq \frac{(V_{IN} \cdot T_{ON})_{MAX}}{B_{MAX} \times A_e} \tag{10.19}$$

Where: B_{MAX} is maximum flux density and A_e is the cross-sectional area of the core.

Picking $(V_{IN} \times T_{ON})_{MAX}$ to be 750 V·µsec and getting the maximum flux density and core area from the transformer datasheet, we can calculate the minimum number of turns for the primary winding. Substitute B_{MAX} as 320mT and the area of the core to be 19.2 mm² we solve equation 10.19 to get:

$$N_{PRI} \geq \frac{750V \cdot \mu s}{320mT \times 19.2mm^2} = 122.1 turns$$

To avoid hitting the maximum flux density, pick a value for N_{PRI} to be higher than this. In this example 144 turns is picked.

10.9 Secondary Winding

From the primary winding turns, we obtain the secondary winding.

$$N_{SEC.} = \frac{N_{PRI}}{N_{tr}} \tag{10.20}$$

Thus, in our example:

$$N_{SEC} = \frac{144}{13} = 11 \ turns$$

At this point it is advantageous to make sure the primary winding and secondary winding chosen is actually feasible to wind.

10.10 Bias Winding

V_{CC} is the supply to the iW1692 and should be between 12 V and 16 V. The number of auxiliary windings needs to ensure that V_{CC} does not exceed 16 V.

$$N_{BIAS} = \frac{N_{SEC} \times (V_{CC} + V_{fd})}{V_{OUT}} \tag{10.21}$$

The number of auxiliary windings can be calculated using equation 10.21. Let V_{CC} = 12 V

$$N_{BIAS} = \frac{11 turns \times 12.5V}{5.5V} = 25 turns$$

Here we've actually chosen a lower number for the bias winding, 22 turns.

10.11 VSENSE Resistors and Winding

The output voltage regulation is mainly determined by the feedback signal V_{SENSE}.

$$V_{SENSE} = V_{OUT\_PCB} \times K_{SENSE} \tag{10.22}$$

Where:

$$K_{SENSE} = \frac{R_4}{R_4 + R_3} \times \frac{N_{Vsense}}{N_{SEC}} \tag{10.23}$$

Internally, V_{SENSE} is compared to a reference voltage 1.538 V. From equation 10.22 we get:

$$K_{SENSE} = \frac{1.538V}{5.0V} = 0.3076 \tag{10.24}$$

(5.0 V without the addition of V_{FD} is used here see 9.3 for details)

Solving for R4 in equation 10.23 assuming R3 is 20 kΩ, and N_{VSENSE} is 24 turns we get R4 should be around 3 kΩ.

In figure 12.0.1, C8 is used to help filter the V_{SENSE} signal.

10.12 Output Capacitors

Assuming an ideal capacitor where ESR (equivalent series resistance) and ESL (equivalent series inductance) are negligible then:

$$C_{OUT} = \frac{Q_{OUT}}{V_{OUT\_RIPPLE\_PK}} \tag{10.25}$$

The output capacitor supplies the load current when the secondary current is below the output current.

$$Q_{OUT} = \frac{L_M \times (I_{SEC\_PK} - I_{OUT})^2}{2 \times N_{TR}^2 \times \eta_X \times V_{OUT}} \tag{10.26}$$

The secondary peak current is:

$$I_{SEC} = \frac{(V_{IN} \cdot T_{ON})_{MAX}}{L_M} \times N_{TR} \times \eta_X \tag{10.27}$$

Assuming we want to get under 50 mV of ripple on the output:

$$I_{SEC} = \frac{720V \cdot \mu s}{1.5mH} \times 13 \times 87\% = 5.655A$$

$$Q_{OUT} = \frac{1.5mH \times (5.655A - 1A)^2}{2 \times 13^2 \times 87\% \times 5.5V} = 20\mu C$$

$$C_{OUT} = \frac{20\mu C}{50mV} = 402\mu F$$

In this calculations ESR and ESL are ignored; the reason this calculation is still valid is because of the second stage LC filter, L3 and C11. These two components reduce the ESR and ESL ripple. However, the actual output capacitance needs to be higher than this calculated value.

10.13 Snubber Network

The snubber network is implemented to reduce the voltage stress on the MOSFET immediately following the turn off of the gate drive. The goal is to dissipate the energy from the leakage inductance of the transformer. For simplicity and a more conservative design first assume the energy of the leakage inductance is only dissipated through the snubber. Thus:

$$\frac{1}{2} \times L_{lk} \times I_{pri\_pk}^2 = \frac{1}{2} \times C_3 \times \left[V_{pk}^2 - V_{val}^2 \right] \tag{10.28}$$

L_{LK} can be measured from the transformer, I_{PRI_PK} is 0.9 V divided by R_{ISENSE}, and V_{PK} is the peak V_{DS} of the MOSFET. Choose C3, keeping in mind that the larger the value of C3 you choose, the lower the voltage stress is that is applied to the MOSFET. However, capacitors are more expensive the larger their capacitance. Choose C3 based on these two criteria and select V_{PK} and V_{VAL}. Now a resistor needs to be selected to dissipate V_{PK} to V_{VAL} during the on-time of the gate driver. The dissipation of this resistor is given by:

$$\frac{V_{val}}{V_{pk}} = e^{-Tperiod / R_5 \cdot C_3} \tag{10.29}$$

Using equation 10.29 solve for R5. This will give a conservative estimate of what C3 and R5 should be.

Included in the snubber network is also a resistor (R6) in series with the diode (D6). D6 directs the current to C3 when the MOSFET is turned off; however there is some reverse current that goes through the diode immediately after the MOSFET is turned back on. This reverse current occurs because there is a short period of time when the diode still conducts after switching from forward biased to reverse biased. This conduction will distort the falling edge of the V_{SENSE} curve and affect the operation of the IC. So, the resistor, R6, is there to diminish the reverse current that goes through D6 immediately after the MOSFET is turned on.

10.14 ON-Time Delay Filter

iW1692 also contains a feature that allows for adjustment to match high line and low line constant current curves. The mismatch in high line and low line curves is due to the IC propagation delay, and the MOSFET turn off delay. iW1692 slightly over compensates for them to provide flexibility in design by providing extra delay. R15 and C5 can be used to adjust the compensation. To determine values R15 and C5 follow these steps:

1. Measure the difference between high line and low line constant current limit without R15 and C5.
2. Find the curve that best matches this difference from Figure 11.0.7.
3. Find the L_M that matches the power supply. Match the τ_{RC}.
4. Find R15 and C5 from equation 10.30:

$$\tau_{RC} = R_{15} \times C_5 \tag{10.30}$$

We observe that the difference between high line and low line constant current limit is 20 mA. Matching the primary inductance 2 mH and the curve, we find τ_{RC} to be 4.4×10^{-8} s. We then pick R15 to be 1 kΩ and substitute into equation 10.30.

$$4.4 \cdot 10^{-8}\,\text{sec} = 1k\Omega \times C_5$$

Solving for C5, we get 44 pF. The result should be a match between high line and low line constant current curves. See figure 11.0.7 for details.

10.15 PCB Layout

In the iW1692, there are two signals that are important to control output performance; these are the I_{SENSE} signal and the V_{SENSE} signal. The I_{SS} resistor should be close to the source of the MOSFET to avoid any trace resistance from contaminating the I_{SENSE} signal. Also the I_{SENSE} signal should be placed close to the I_{SENSE} pin. The V_{SENSE} signal should be placed close to the transformer to improve the quality of the sensing signal.

11.0 Design Example Performance Characteristics

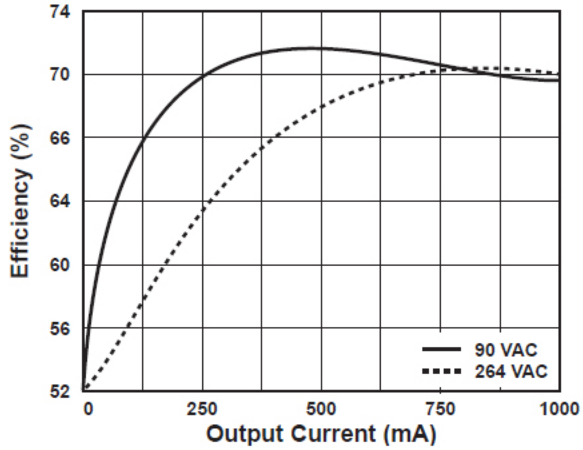


Figure 11.0.1 V_{SENSE} Efficiency at 90 V_{AC} and 264 V_{AC}

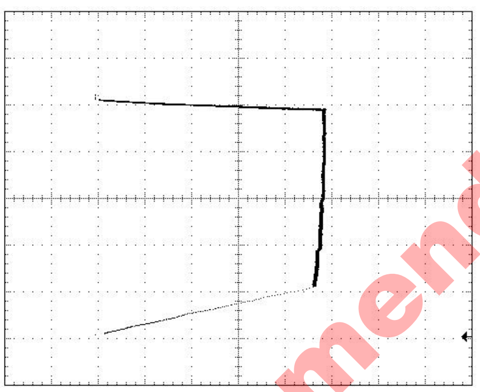


Figure 11.0.2 Regulation

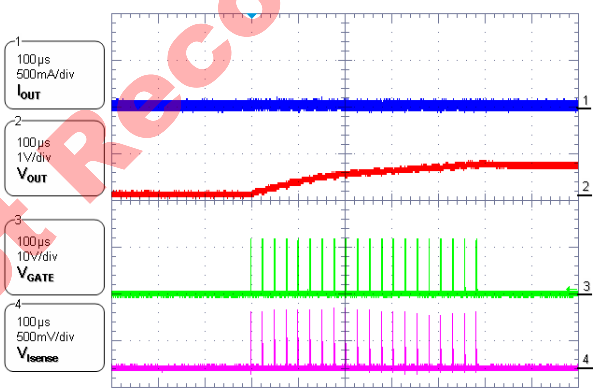


Figure 11.0.4 V_{SENSE} Short Before Start-up (no load)

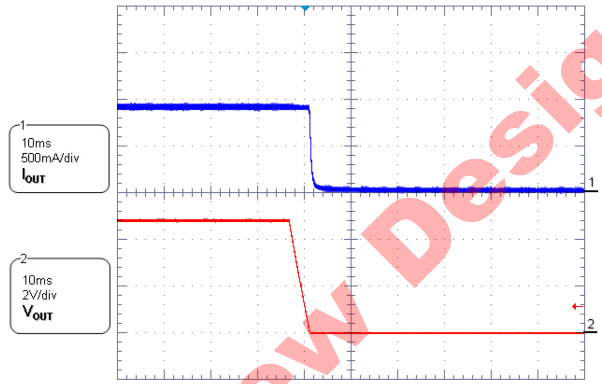


Figure 11.0.5 I_{SENSE} Short at 90 V_{AC}

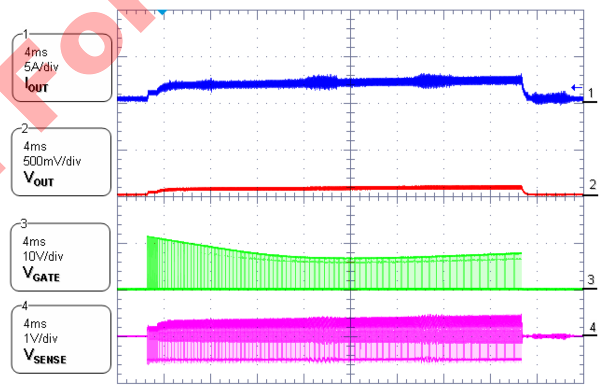


Figure 11.0.6 output Short Fault (50% load)

11.0 Design Example Performance Characteristics

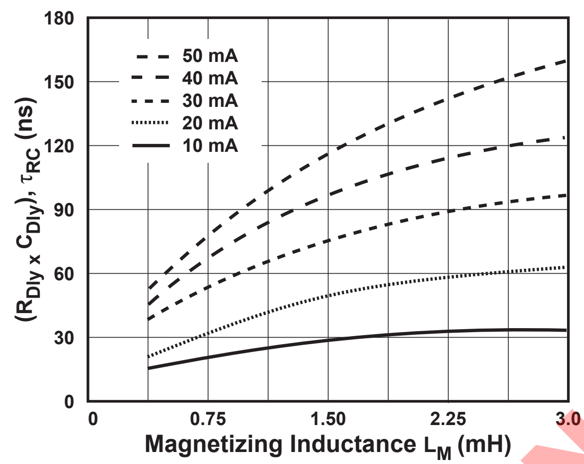


Figure 11.0.7. T_{ON} Compensation Chart

12.0 Application Circuit

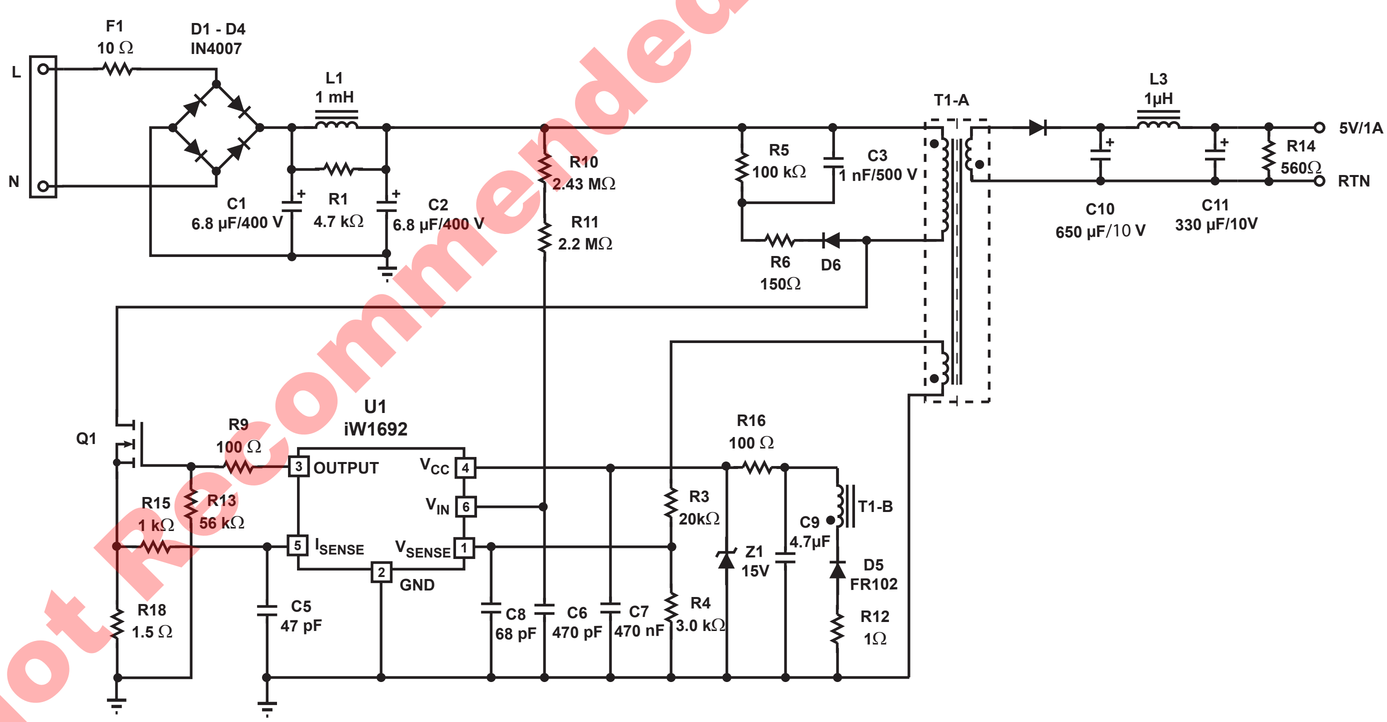
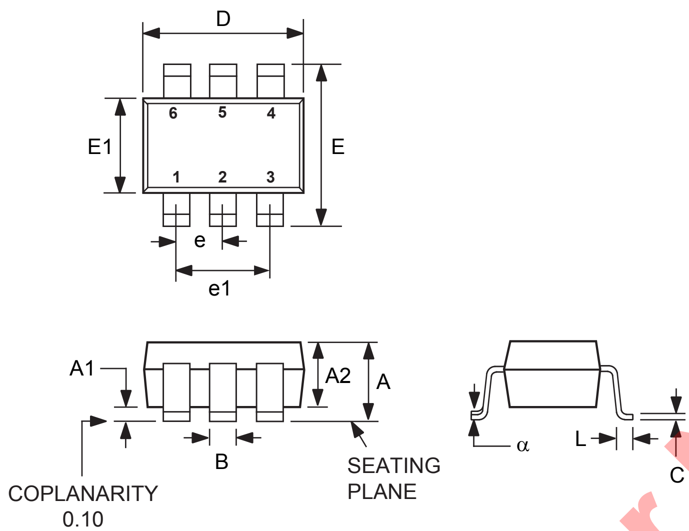


Figure 12.0.1. Typical Application Circuit

13.0 Physical Dimensions

6-Lead Small Outline Transistor Package



Symbol	Millimeters	
	MIN	MAX
A	-	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
C	0.08	0.22
D	2.90 BSC	
E	2.80 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
α	0°	8°

Figure 13.0.1. Physical dimensions, 6-lead SOT-23 package

Compliant to JEDEC Standard MO-178AB

Controlling dimensions are in millimeters

This package is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; packages can withstand 10 s immersion < 270ºC

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E1 are are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs and interlead flash, but including any mismatch between top and bottom of the plastic body.

14.0 Ordering Information

Part Number	Mark	Package	Description
iW1692-00	Gxxx	SOT23-6L	Tape & Reel[1]

Note 1: Tape & Reel quantity for SOT23 is 3,000/Reel.

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