# NBM™ Bus Converter

## NBM6123x46C15A6yzz

## Non-Isolated, Fixed Ratio DC-DC Converter

### Features

- Up to 160A continuous secondary current
- Up to 3600W/in$^3$ power density
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 6123 through-hole ChiP package
  - 2.402" x 0.990" x 0.286" (61.00mm x 25.14mm x 7.26mm)

### Typical Applications

- DC Power Distribution
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

| Product Ratings | |
|---|---|
| $V_{PRI}$ = 42V (36 – 46V) | $I_{SEC}$= up to 160A |
| $V_{SEC}$ = 14V (12.0 – 15.3V) (NO LOAD) | K = 1/3 |

### Product Description

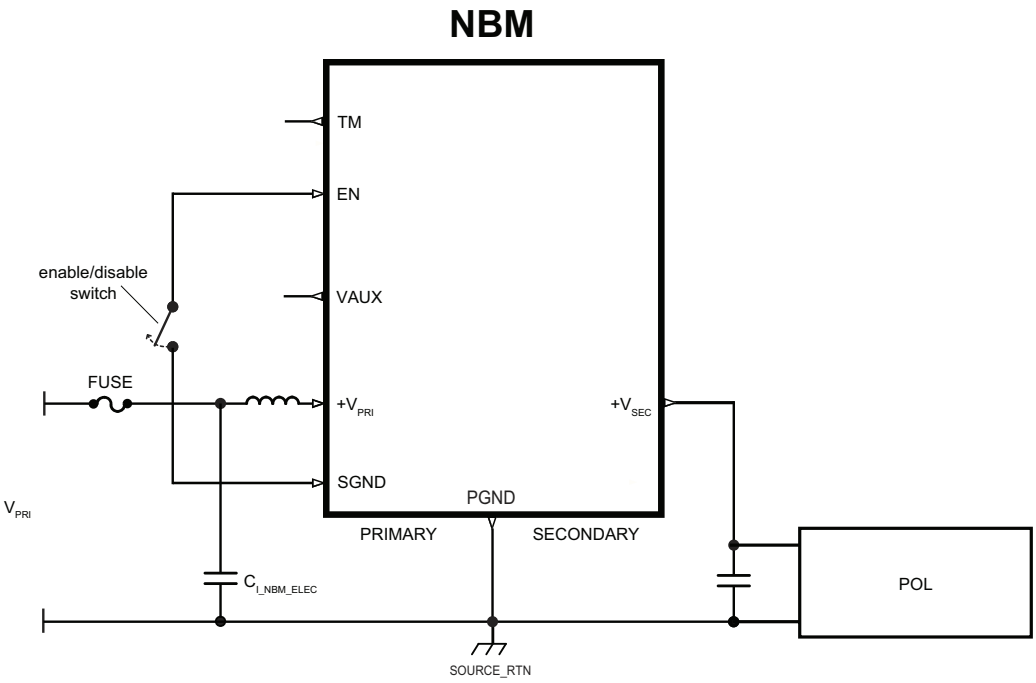
The VI Chip® Non-Isolated Bus Converter (NBM™) is a high efficiency Sine Amplitude Converter™ (SAC™), operating from a 36 to 46$V_{DC}$ primary bus to deliver a non-isolated, ratiometric secondary voltage from 12.0 to 15.3$V_{DC}$.

The NBM6123x46C15A6yzz offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a POL regulator to be located at the primary side of the NBM module. With a primary to secondary K factor of 1/3, that capacitance value can be reduced by a factor of 9x, resulting in savings of board area, material and total system cost.

Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the NBM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components, enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

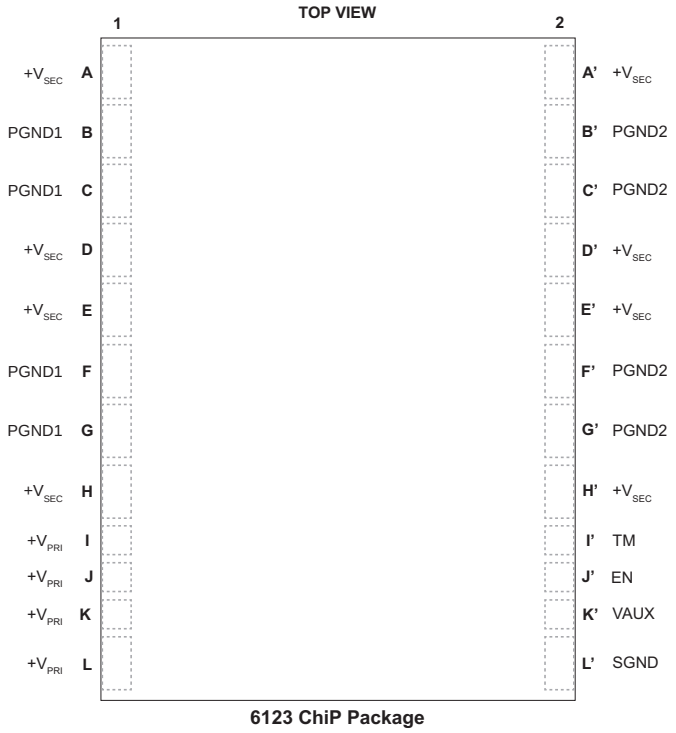
The NBM non-isolated topology allows operation in forward and reverse directions and provides bidirectional protections. However if power train is disabled by any protection, and $V_{SEC}$ is present, then voltage equal to $V_{SEC}$ minus two diode drops will appear on primary side.

## Typical Application




NBM6123x46C15A6yzz+ Point of Load

## Pin Configuration




**6123 ChiP Package**

## Pin Descriptions

| Pin Number | Signal Name | Type | Function |
|---|---|---|---|
| I1, J1, K1, L1 | $+V_{PRI}$ | PRIMARY POWER | Positive primary auto-transformer power terminal |
| I'2 | TM | OUTPUT | Temperature Monitor; Primary side referenced signals |
| J'2 | EN | INPUT | Enables and disables power supply; Primary side referenced signals |
| K'2 | VAUX | OUTPUT | Auxilary Voltage Source; Primary side referenced signals |
| L'2 | SGND | SIGNAL RETURN | Signal return terminal only. Do not connect to PGND |
| A1, D1, E1, H1, A'2, D'2, E'2, H'2 | $+V_{SEC}$ | SECONDARY POWER | Positive secondary auto-transformer power terminal |
| B1, C1, F1, G1 B'2, C'2, F'2, G'2 | PGND* | POWER RETURN | Common negative primary and secondary auto-transformer power return terminal |

*For proper operation an external low impedance connection must be made between listed -PGND1 and PGND2 terminals.

## Part Ordering Information

| Product Function | Package Size | Package Mounting | Max Primary Input Voltage | Range Identifier | Max Secondary Voltage | Secondary Output Current | Temperature Grade | Option |
|---|---|---|---|---|---|---|---|---|
| NBM | 6123 | x | 46 | C | 15 | A6 | y | zz |
| Non-isolated Bus Converter Module | 61 = L<br>23 = W | **T** = TH<br>**S** = SMT | 46V | 36 – 46V | 15V<br>No Load | 160A | **T** = -40°C – 125°C<br>**M** = -55°C – 125°C | **00** = Analog Ctrl<br>**01** = PMBus Ctrl<br>**0R** = Reversible Analog Ctrl<br>**0P** = Reversible PMBus Ctrl |

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

## Standard Models

| Product Function | Package Size | Package Mounting | Max Primary Input Voltage | Range Identifier | Max Secondary Voltage | Secondary Output Current | Temperature Grade | Option |
|---|---|---|---|---|---|---|---|---|
| NBM | 6123 | T | 46 | C | 15 | A6 | T | 0R |

## Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

| Parameter | Comments | Min | Max | Unit |
|---|---|---|---|---|
| $+V_{PRI_DC}$ to $-V_{PRI_DC}$ | | -1 | 60 | V |
| $V_{PRI_DC}$ or $V_{SEC_DC}$ slew rate (operational) | | | 1 | V/µs |
| $+V_{SEC_DC}$ to $-V_{SEC_DC}$ | | -1 | 20 | V |
| TM to $-V_{PRI_DC}$ | | -0.3 | 4.6 | V |
| EN to $-V_{PRI_DC}$ | | | 5.5 | V |
| VAUX to $-V_{PRI_DC}$ | | | 4.6 | V |

## Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **General Powetrain PRIMARY to SECONDARY Specification (Forward Direction)** | | | | | | |
| Primary Input Voltage range, continuous | $V_{PRI_DC}$ | | **36** | | **46** | V |
| $V_{PRI}$ µController | $V_{\mu C_ACTIVE}$ | $V_{PRI_DC}$ voltage where µC is initialized, (ie VAUX = Low, powertrain inactive) | | | 15 | V |
| PRI to SEC Input Quiescent Current | $I_{PRI_Q}$ | Disabled, EN Low, $V_{PRI_DC}$ = 42V | | 8 | | mA |
| | | $T_{INTERNAL}$ ≤ 100°C | | | 12 | |
| PRI to SEC No Load Power Dissipation | $P_{PRI_NL}$ | $V_{PRI_DC}$ = 42V, $T_{INTERNAL}$ = 25°C | | 12.5 | 19.5 | W |
| | | $V_{PRI_DC}$ = 42V | **5** | | **28** | |
| | | $V_{PRI_DC}$ = 36V to 46V, $T_{INTERNAL}$ = 25 °C | | | 22 | |
| | | $V_{PRI_DC}$ = 36V to 46V | | | **31** | |
| PRI to SEC Inrush Current Peak | $I_{PRI_INR_PK}$ | $V_{PRI_DC}$ = 46V, $C_{SEC_EXT}$ = 3000µF, $R_{LOAD_SEC}$ = 20% of full load current | | 30 | | A |
| | | $T_{INTERNAL}$ ≤ 100°C | | | 75 | |
| DC Primary Input Current | $I_{PRI_IN_DC}$ | At $I_{SEC_OUT_DC}$ = 160A, $T_{INTERNAL}$ ≤ 100°C | | | 53.9 | A |
| Transformation Ratio | K | Primary to secondary, K = $V_{SEC_DC}$ / $V_{PRI_DC}$, at no load | | 1/3 | | V/V |
| Secondary Output Current (continuous) | $I_{SEC_OUT_DC}$ | | | | 160 | A |
| Secondary Output Current (pulsed) | $I_{SEC_OUT_PULSE}$ | 10ms pulse, 25% Duty cycle, $I_{SEC_OUT_AVG}$ ≤ 50% rated $I_{SEC_OUT_DC}$ | | | 176 | A |
| PRI to SEC Efficiency (ambient) | $\eta_{AMB}$ | $V_{PRI_DC}$ = 42V, $I_{SEC_OUT_DC}$ = 160A | 97.4 | 98 | | % |
| | | $V_{PRI_DC}$ = 36V to 46V, $I_{SEC_OUT_DC}$ = 160A | 97.1 | | | |
| | | $V_{PRI_DC}$ = 42V, $I_{SEC_OUT_DC}$ = 80A | 97.5 | 98.2 | | |
| PRI to SEC Efficiency (hot) | $\eta_{HOT}$ | $V_{PRI_DC}$ = 42V, $I_{SEC_OUT_DC}$ = 160A | 96.9 | 97.4 | | % |
| PRI to SEC Efficiency (over load range) | $\eta_{20\%}$ | 32A < $I_{SEC_OUT_DC}$ < 160A | 90 | | | % |
| PRI to SEC Output Resistance | $R_{SEC_COLD}$ | $V_{PRI_DC}$ = 42V, $I_{SEC_OUT_DC}$ = 160A, $T_{INTERNAL}$ = -40°C | 0.8 | 0.95 | 1.1 | mΩ |
| | $R_{SEC_AMB}$ | $V_{PRI_DC}$ = 42V, $I_{SEC_OUT_DC}$ = 160A | 0.9 | 1.3 | 1.7 | |
| | $R_{SEC_HOT}$ | $V_{PRI_DC}$ = 42V, $I_{SEC_OUT_DC}$ = 160A, $T_{INTERNAL}$ = 100°C | 1.5 | 1.75 | 2.0 | |
| Switching Frequency | $F_{SW}$ | Frequency of the Output Voltage Ripple = 2x $F_{SW}$ | **1.14** | 1.20 | **1.26** | MHz |
| Secondary Output Voltage Ripple | $V_{SEC_OUT_PP}$ | $C_{SEC_EXT}$ = 0µF, $I_{SEC_OUT_DC}$ = 160A, $V_{PRI_DC}$ = 42V, 20MHz BW | | 110 | | mV |
| | | $T_{INTERNAL}$ ≤ 100°C | | | 205 | |
| Primary Input Leads Inductance (Parasitic) | $L_{PRI_IN_LEADS}$ | Frequency 2.5MHz (double switching frequency), Simulated lead model | | 3 | | nH |
| Secondary Output Leads Inductance (Parasitic) | $L_{SEC_OUT_LEADS}$ | Frequency 2.5MHz (double switching frequency), Simulated lead model | | 0.64 | | nH |

## Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **General Powetrain PRIMARY to SECONDARY Specification (Forward Direction) Cont.** | | | | | | |
| Effective Primary Capacitance (Internal) | $C_{PRI_INT}$ | Effective Value at $42V_{PRI_DC}$ | | 16.8 | | µF |
| Effective Secondary Capacitance (Internal) | $C_{SEC_INT}$ | Effective Value at $14V_{SEC_DC}$ | | 140 | | µF |
| Effective Secondary Output Capacitance (External) | $C_{SEC_OUT_EXT}$ | Excessive capacitance may drive module into SC protection | | | **3000** | µF |
| Effective Secondary Output Capacitance (External) | $C_{SEC_OUT_AEXT}$ | $C_{SEC_OUT_AEXT}$ Max = N * 0.5 * $C_{SEC_OUT_EXT\ MAX}$, where N = the number of units in parallel | | | | |
| **Protection PRIMARY to SECONDARY (Forward Direction)** | | | | | | |
| Auto Restart Time | $t_{AUTO_RESTART}$ | Startup into a persistent fault condition. Non-Latching fault detection given $V_{PRI_DC}$ > $V_{PRI_UVLO+}$ | **940** | | **1010** | ms |
| Primary Overvoltage Lockout Threshold | $V_{PRI_OVLO+}$ | | **48** | 50 | **52** | V |
| Primary Overvoltage Recovery Threshold | $V_{PRI_OVLO-}$ | | **46** | 48 | **50** | V |
| Primary Overvoltage Lockout Hysteresis | $V_{PRI_OVLO_HYST}$ | | | 2 | | V |
| Primary Overvoltage Lockout Response Time | $t_{PRI_OVLO}$ | | | 30 | | µs |
| Primary Undervoltage Lockout Threshold | $V_{PRI_UVLO-}$ | | **28** | 30 | **32** | V |
| Primary Undervoltage Recovery Threshold | $V_{PRI_UVLO+}$ | | **30** | 32 | **34** | V |
| Primary Undervoltage Lockout Hysteresis | $V_{PRI_UVLO_HYST}$ | | | 2 | | V |
| Primary Undervoltage Lockout Response Time | $t_{PRI_UVLO}$ | | | 100 | | µs |
| Primary Undervoltage Startup Delay | $t_{PRI_UVLO+_DELAY}$ | From $V_{PRI_DC}$ = $V_{PRI_UVLO+}$ to powertrain active, EN floating, (i.e One time Startup delay from application of $V_{PRI_DC}$ to $V_{SEC_DC}$) | | 30 | | ms |
| Primary Soft-Start Time | $t_{PRI_SOFT-START}$ | From powertrain active. Fast Current limit protection disabled during Soft-Start | | 1 | | ms |
| Secondary Output Overcurrent Trip Threshold | $I_{SEC_OUT_OCP}$ | | **177** | 200 | **240** | A |
| Secondary Output Overcurrent Response Time Constant | $t_{SEC_OUT_OCP}$ | Effective internal RC filter | | 4 | | ms |
| Secondary Output Short Circuit Protection Trip Threshold | $I_{SEC_OUT_SCP}$ | | **240** | | | A |
| Secondary Output Short Circuit Protection Response Time | $t_{SEC_OUT_SCP}$ | | | 1 | | µs |
| Overtemperature Shutdown Threshold | $t_{OTP+}$ | Temperature sensor located inside controller IC | **125** | | | °C |
| Overtemperature Recovery Threshold | $t_{OTP–}$ | | 105 | 110 | 115 | °C |
| Undertemperature Shutdown Threshold | $t_{UTP}$ | Temperature sensor located inside controller IC; Protection not available for M-Grade units. | | | -45 | °C |
| Undertemperature Restart Time | $t_{UTP_RESTART}$ | Startup into a persistent fault condition. Non-Latching fault detection given $V_{PRI_DC}$ > $V_{PRI_UVLO+}$ | | 3 | | s |

## Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **General Powetrain SECONDARY to PRIMARY Specification (Reverse Direction)** | | | | | | |
| Secondary Input Voltage range, continuous | $V_{SEC_DC}$ | | **12** | | **15.3** | V |
| SEC to PRI No Load Power Dissipation | $P_{SEC_NL}$ | $V_{SEC_DC}$ = 14V, $T_{INTERNAL}$ = 25°C | | 12.5 | 20 | W |
| | | $V_{SEC_DC}$ = 14V | **5** | | **29** | |
| | | $V_{SEC_DC}$ = 12V to 15.3V, $T_{INTERNAL}$ = 25°C | | | 22 | |
| | | $V_{SEC_DC}$ = 12V to 15.3V | | | **31** | |
| DC Secondary Input Current | $I_{SEC_IN_DC}$ | At $I_{PRI_DC}$ = 53.3A, $T_{INTERNAL}$ ≤ 100°C | | | **162** | A |
| Primary Output Current (continuous) | $I_{PRI_OUT_DC}$ | | | | **53.3** | A |
| Primary Output Current (pulsed) | $I_{PRI_OUT_PULSE}$ | 10ms pulse, 25% Duty cycle, $I_{PRI_OUT_AVG}$ ≤ 50% rated $I_{PRI_OUT_DC}$ | | | **58.7** | A |
| SEC to PRI Efficiency (ambient) | $\eta_{AMB}$ | $V_{SEC_DC}$ = 14V, $I_{PRI_OUT_DC}$ = 53.3A | 97 | 98 | | % |
| | | $V_{SEC_DC}$ = 12V to 15.3V, $I_{PRI_OUT_DC}$= 53.3A | 96.7 | | | |
| | | $V_{SEC_DC}$ = 14V, $I_{PRI_OUT_DC}$ = 26.7A | 97.6 | 98.3 | | |
| SEC to PRI Efficiency (hot) | $\eta_{HOT}$ | $V_{SEC_DC}$ = 14V, $I_{PRI_OUT_DC}$ = 53.3A | 96.6 | 97 | | % |
| SEC to PRI Efficiency (over load range) | $\eta_{20\%}$ | 10.66A < $I_{PRI_OUT_DC}$ < 53.3A | **90** | | | % |
| SEC to PRI Output Resistance | $R_{PRI_COLD}$ | $V_{SEC_DC}$ = 14V, $I_{PRI_OUT_DC}$ = 53.3A, $T_{INTERNAL}$ = -40°C | 10 | 12 | 14 | mΩ |
| | $R_{PRI_AMB}$ | $V_{SEC_DC}$ = 14V, $I_{PRI_OUT_DC}$ = 53.3A | 12 | 16 | 20 | |
| | $R_{PRI_HOT}$ | $V_{SEC_DC}$ = 14V, $I_{PRI_OUT_DC}$ = 53.3A, $T_{INTERNAL}$ = 100°C | 16 | 19 | 22 | |
| Primary Output Voltage Ripple | $V_{PRI_OUT_PP}$ | $C_{PRI_OUT_EXT}$ = 0µF, $I_{PRI_OUT_DC}$ = 53.3A, $V_{SEC_DC}$ = 14V, 20MHz BW | | 330 | | mV |
| | | $T_{INTERNAL}$ ≤ 100°C | | | **615** | |

## Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Protection SECONDARY to PRIMARY (Reverse Direction)** | | | | | | |
| Effective Primary Output Capacitance (External) | $C_{PRI_OUT_EXT}$ | Excessive capacitance may drive module into SC protection when starting from Secondary to Primary | | | **300** | µF |
| Secondary Overvoltage Lockout Threshold | $V_{SEC_OVLO+}$ | | **16** | 16.7 | **17.4** | V |
| Secondary Overvoltage Recovery Threshold | $V_{PRI_OVLO-}$ | | **15.3** | 16 | **16.7** | V |
| Secondary Overvoltage Lockout Response Time | $t_{PRI_OVLO}$ | | | 30 | | µs |
| Secondary Undervoltage Lockout Threshold | $V_{SEC_UVLO-}$ | | **9.3** | 10 | **10.7** | V |
| Secondary Undervoltage Recovery Threshold | $V_{PRI_UVLO+}$ | | **10** | 10.7 | **11.4** | V |
| Secondary Undervoltage Lockout Response Time | $t_{SEC_UVLO}$ | | | 100 | | µs |
| Primary Output Overcurrent Trip Threshold | $I_{PRI_OUT_OCP}$ | Powertrain is stopped but current can flow from Secondary to Primary through MOSFET body Diodes | **59** | 66.7 | **80** | A |
| Primary Output Overcurrent Response Time Constant | $t_{PRI_OUT_OCP}$ | Effective internal RC filter | | 4 | | ms |
| Primary Short Circuit Protection Trip Threshold | $I_{PRI_SCP}$ | Powertrain is stopped but current can flow from Secondary to Primary through MOSFET body Diodes | **80** | | | A |
| Primary Short Circuit Protection Response Time | $t_{PRI_SCP}$ | | | 1 | | µs |

## Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Temperature Monitor | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| • The TM pin is a standard analog I/O configured as an output from an internal µC.<br>• The TM pin monitors the internal temperature of the controller IC within an accuracy of ±5°C.<br>• µC 250kHz PWM output internally pulled high to 3.3V. | | | | | | | | |
| **SIGNAL TYPE** | **STATE** | **ATTRIBUTE** | **SYMBOL** | **CONDITIONS / NOTES** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **DIGITAL OUTPUT** | Startup | Powertrain active to TM time | $t_{TM}$ | | | **100** | | µs |
| | Regular Operation | TM Duty Cycle | $TM_{PWM}$ | | **18.18** | | **68.18** | % |
| | | TM Current | $I_{TM}$ | | | | **4** | mA |
| | | **Recommended External filtering** | | | | | | |
| | | TM Capacitance (External) | $C_{TM_EXT}$ | Recommended External filtering | | 0.01 | | µF |
| | | TM Resistance (External) | $R_{TM_EXT}$ | Recommended External filtering | | 1 | | kΩ |
| | | **Specifications using recommended filter** | | | | | | |
| | | TM Gain | $A_{TM}$ | | | 10 | | mV / °C |
| | | TM Voltage Reference | $V_{TM_AMB}$ | | | 1.27 | | V |
| | | TM Voltage Ripple | $V_{TM_PP}$ | $R_{TM_EXT}$ = 1K Ohm, $C_{TM_EXT}$ = 0.01µF, $V_{PRI_DC}$ = 42V, $I_{SEC_DC}$ = 160A | | 28 | | mV |
| | | | | $T_{INTERNAL}$ ≤ 100°C | | | 40 | |

| Enable / Disable Control | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| • The EN pin is a standard analog I/O configured as an input to an internal µC.<br>• It is internally pulled high to 3.3V.<br>• When held low the NBM™ internal bias will be disabled and the powertrain will be inactive.<br>• In an array of NBMs, EN pins should be interconnected to synchronize startup.<br>• Unit must not be disabled if a load is present on $+V_{PRI}$ while in reverse operation. | | | | | | | | |
| **SIGNAL TYPE** | **STATE** | **ATTRIBUTE** | **SYMBOL** | **CONDITIONS / NOTES** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **ANALOG INPUT** | Startup | EN to Powertrain active time | $t_{EN_START}$ | $V_{PRI_DC}$ > $V_{PRI_UVLO+}$, EN held low both conditions satisfied for T > $t_{PRI_UVLO+_DELAY}$ | | **10** | | ms |
| | Regular Operation | EN Voltage Threshold | $V_{EN_TH}$ | | **2.3** | | | V |
| | | EN Resistance (Internal) | $R_{EN_INT}$ | Internal pull up resistor | | 1.5 | | kΩ |
| | | EN Disable Threshold | $V_{EN_DISABLE_TH}$ | | | | **1** | V |

## Signal Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

**Auxiliary Voltage Source**

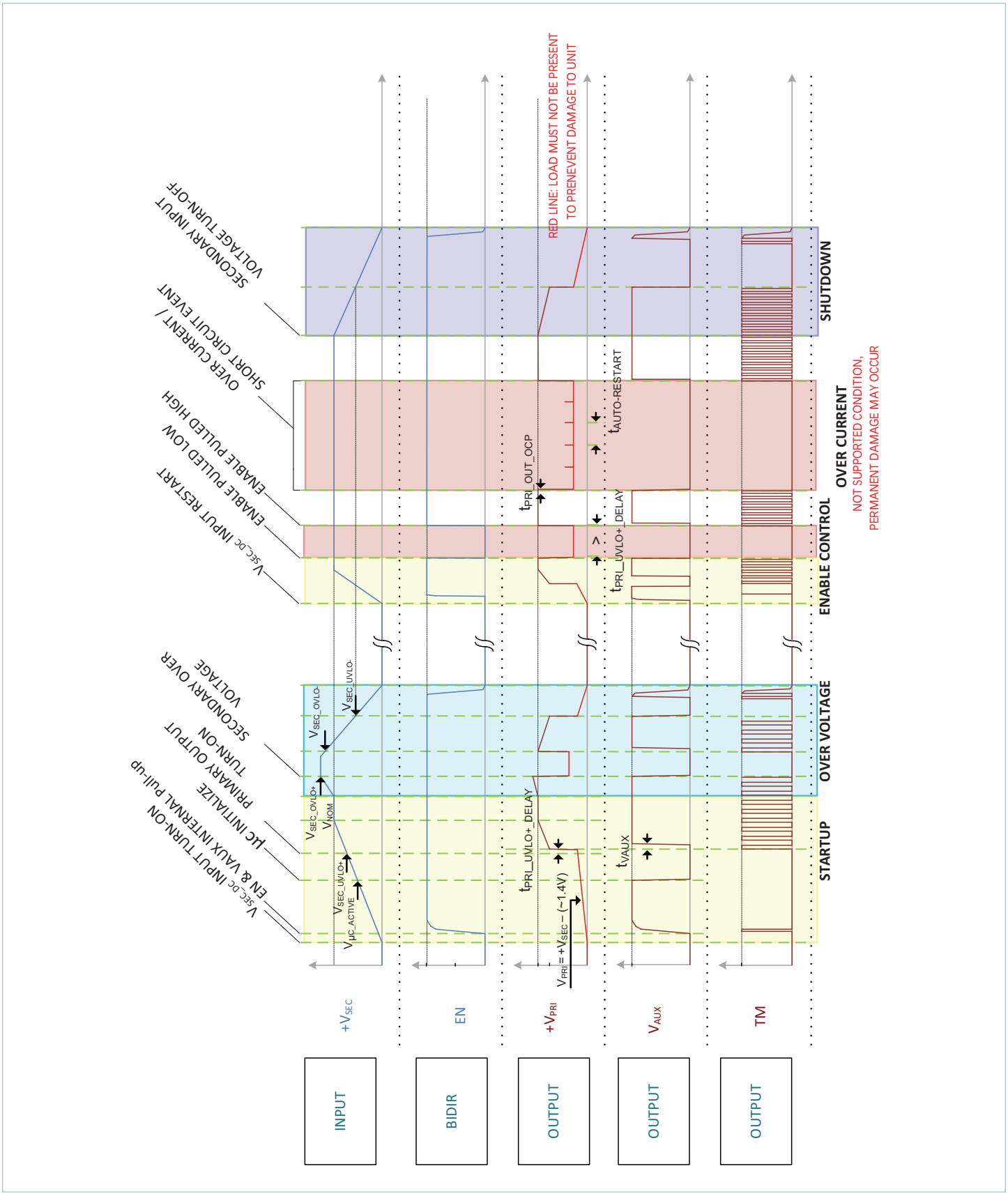
- The VAUX pin is a standard analog I/O configured as an output from an internal µC.
- VAUX is internally connected to µC output as internally pulled high to a 3.3V regulator with 2% tolerance, a 1% resistor of 1.5kΩ.
- VAUX can be used as a "Ready to process full power" flag. This pin transitions VAUX voltage after a 2ms delay from the start of powertrain activating, signaling the end of softstart.
- VAUX can be used as "Fault flag". This pin is pulled low internally when a fault protection is detected.

| SIGNAL TYPE | STATE | ATTRIBUTE | SYMBOL | CONDITIONS / NOTES | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| ANALOG OUTPUT | Startup | Powertrain active to VAUX time | $t_{VAUX}$ | Powertrain active to VAUX High | | **2** | | ms |
| | Regular Operation | VAUX Voltage | $V_{VAUX}$ | | **2.8** | | **3.3** | V |
| | | VAUX Available Current | $I_{VAUX}$ | | | | **4** | mA |
| | | VAUX Voltage Ripple | $V_{VAUX_PP}$ | | | 50 | | mV |
| | | | | $T_{INTERNAL}$ ≤ 100°C | | | **100** | |
| | | VAUX Capacitance (External) | $C_{VAUX_EXT}$ | | | | 0.01 | µF |
| | | VAUX Resistance (External) | $R_{VAUX_EXT}$ | $V_{PRI_DC} < V_{µC_ACTIVE}$ | 1.5 | | | kΩ |
| | Fault | VAUX Fault Response Time | $t_{VAUX_FR}$ | From fault to $V_{VAUX}$ = 2.8V, $C_{VAUX}$ = 0pF | | 10 | | µs |

**Signal Ground**

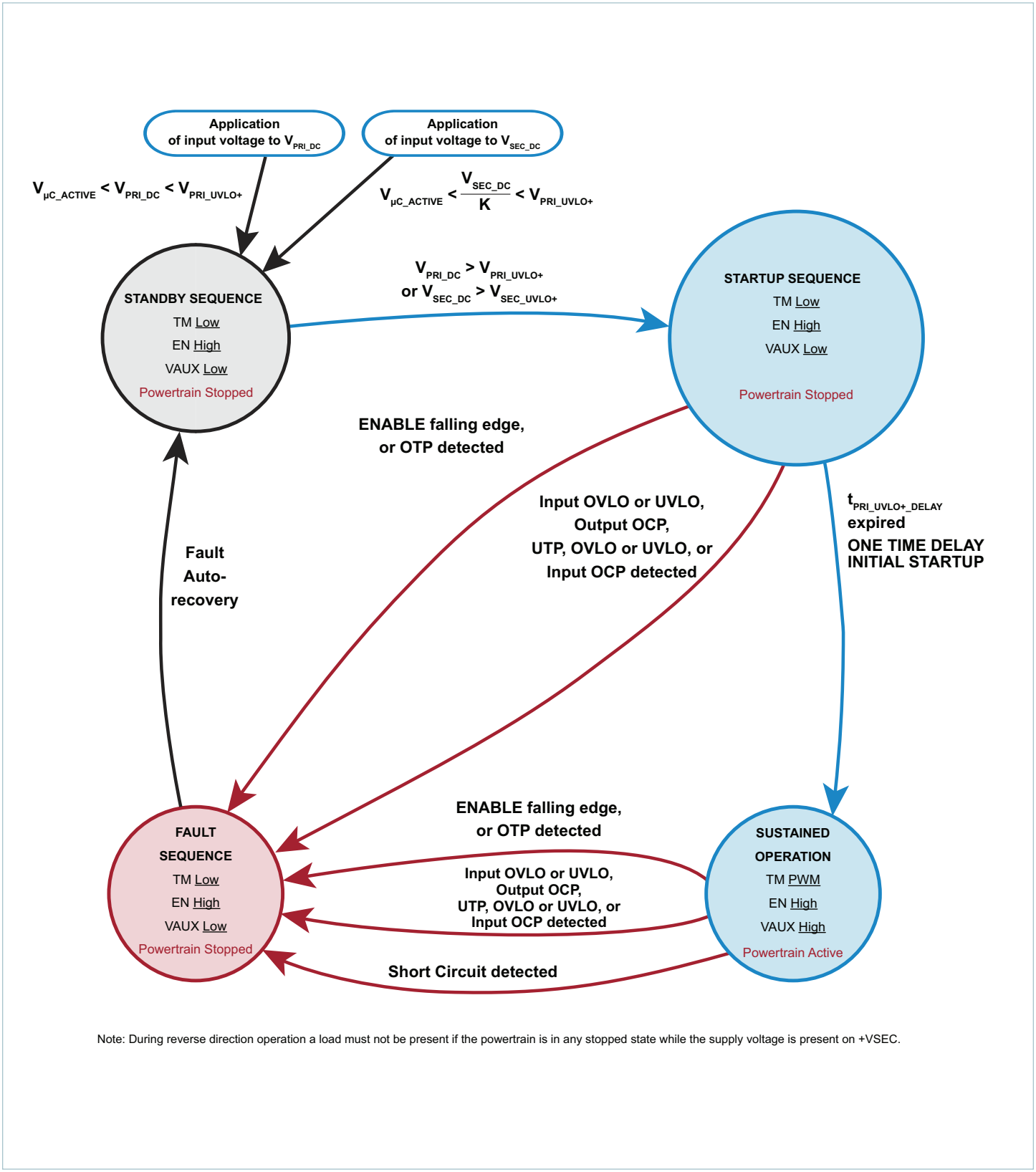
- Signal ground is internally connect to PGND through a zero ohm resistor.
- Internal SGND traces are not designed to support high current.

## NBM™ Reverse Direction Timing Diagram



## High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.




Note: During reverse direction operation a load must not be present if the powertrain is in any stopped state while the supply voltage is present on +VSEC.

## Application Characteristics

Product is mounted and temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected data from primary sourced units processing power in forward direction.See associated figures for general trend data.

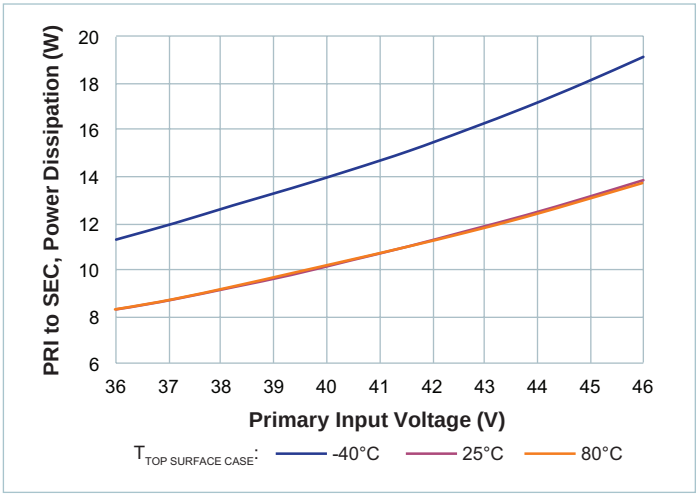



***Figure 4*** — *No load power dissipation vs. $V_{PRI_DC}$*

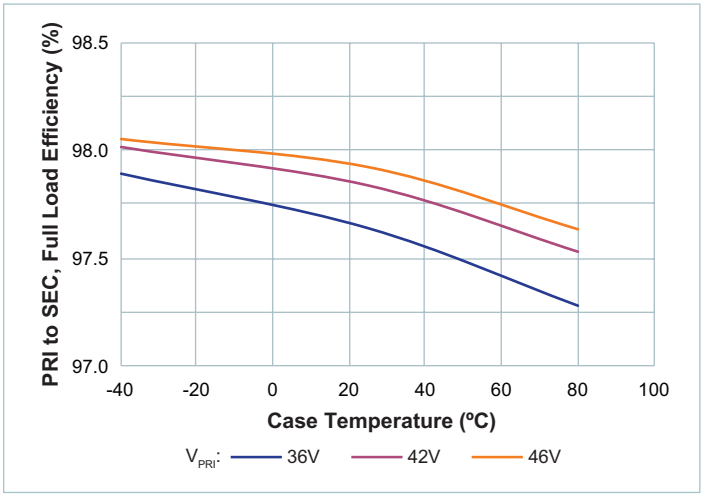



***Figure 5*** — *Full load efficiency vs. temperature; $V_{PRI_DC}$*

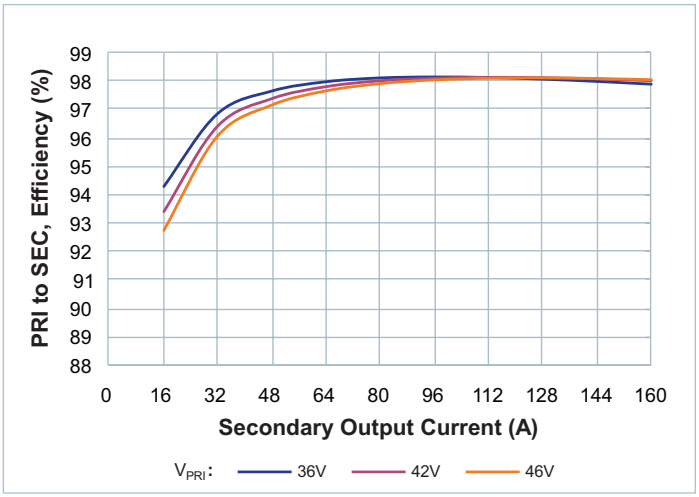



***Figure 6*** — *Efficiency at $T_{CASE}$ = -40°C*

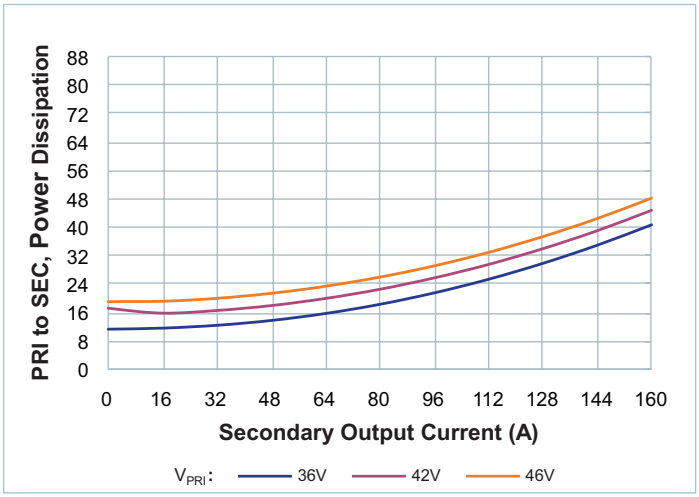



***Figure 7*** — *Power dissipation at $T_{CASE}$ = -40°C*

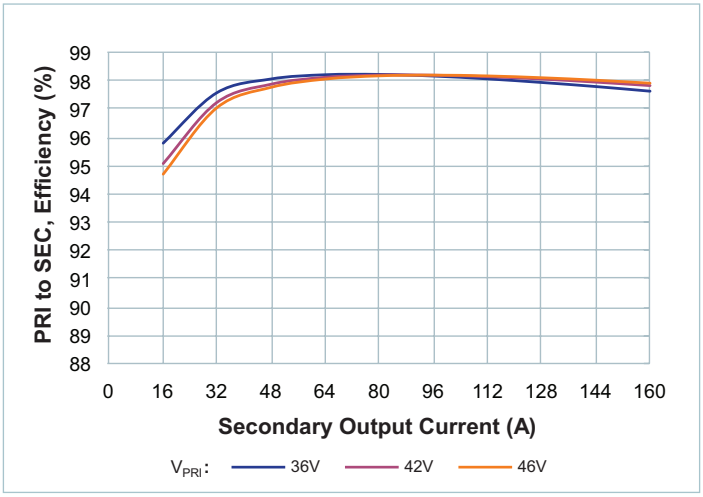



***Figure 8*** — *Efficiency at $T_{CASE}$ = 25°C*

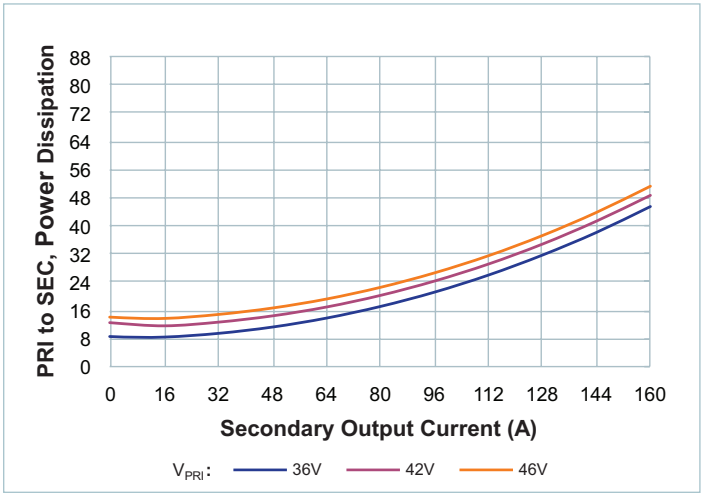



***Figure 9*** — *Power dissipation at $T_{CASE}$ = 25°C*

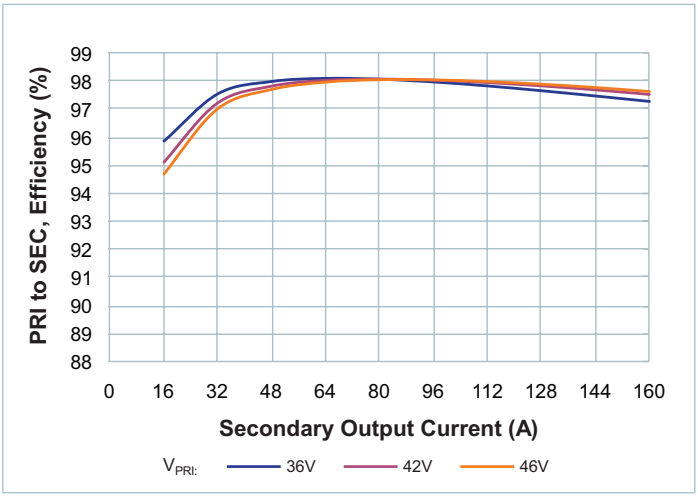



***Figure 10*** — *Efficiency at $T_{CASE}$ = 80°C*

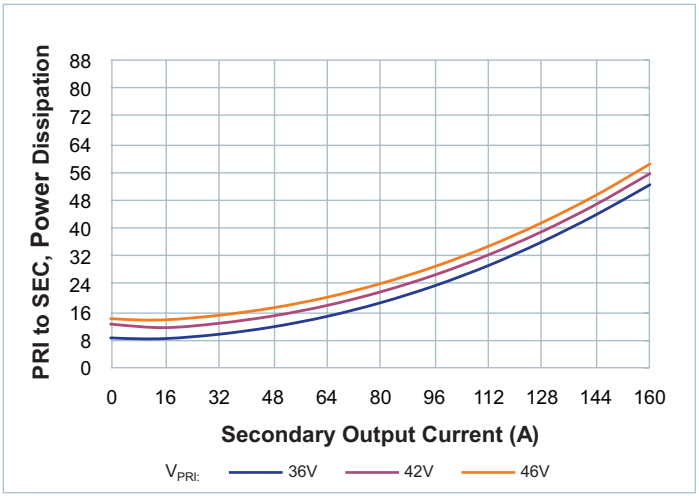



***Figure 11*** — *Power dissipation at $T_{CASE}$ = 80°C*

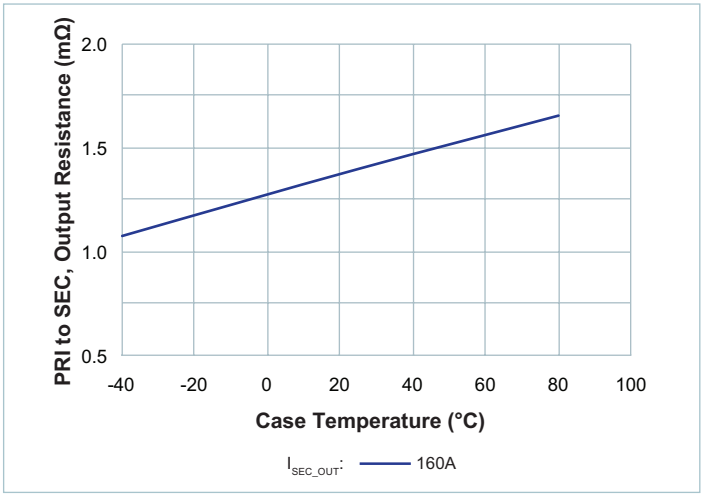



***Figure 12*** — *$R_{SEC}$ vs. temperature; Nominal $V_{PRI_DC}$ $I_{SEC_DC}$ = 160A at $T_{CASE}$ = 80°C*

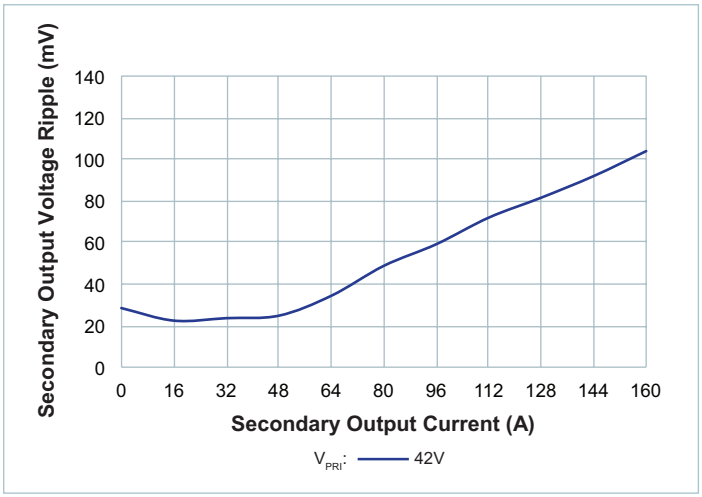



***Figure 13*** — *$V_{SEC_OUT_PP}$ vs. $I_{SEC_DC}$ ; No external $C_{SEC_OUT_EXT.}$ Board mounted module, scope setting: 20MHz analog BW*

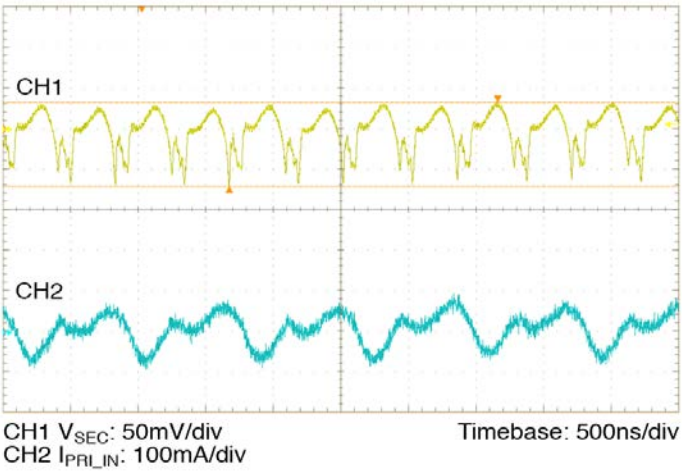



***Figure 14*** — *Full load ripple, 270µF $C_{PRI_IN_EXT}$; No external $C_{SEC_OUT_EXT}$. Board mounted module, scope setting: 20MHz analog BW*

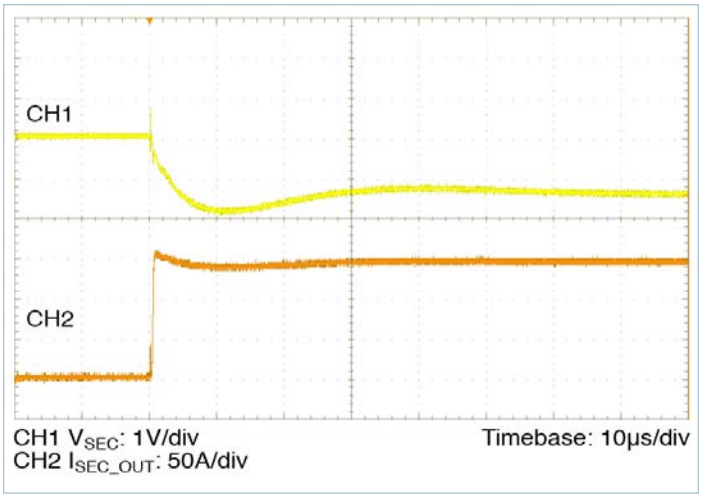



***Figure 15*** — *0A – 160A transient response: $C_{PRI_IN_EXT}$ = 270µF, no external $C_{SEC_OUT_EXT}$*

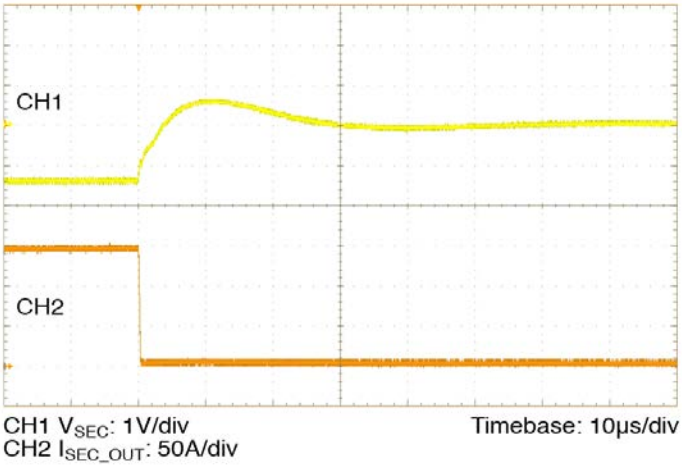



***Figure 16*** — *160A – 0A transient response: $C_{PRI_IN_EXT}$ = 270µF, no external $C_{SEC_OUT_EXT}$*

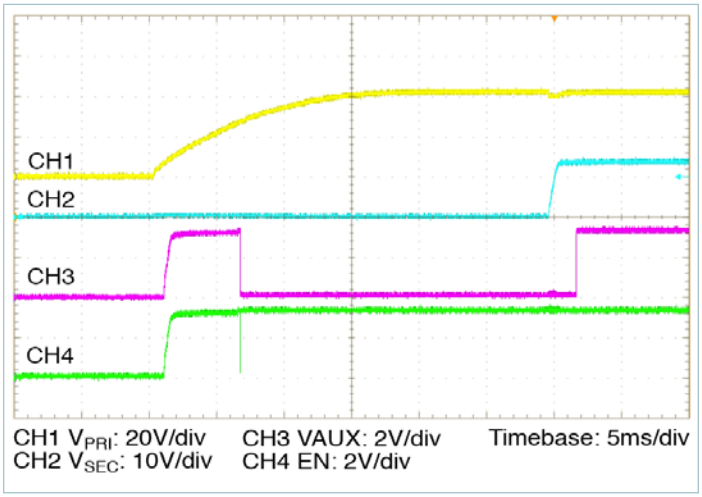



***Figure 17*** — *Start up from application of $V_{PRI_DC}$= 42V, 20% $I_{SEC_DC}$, 100% $C_{SEC_OUT_EXT}$*

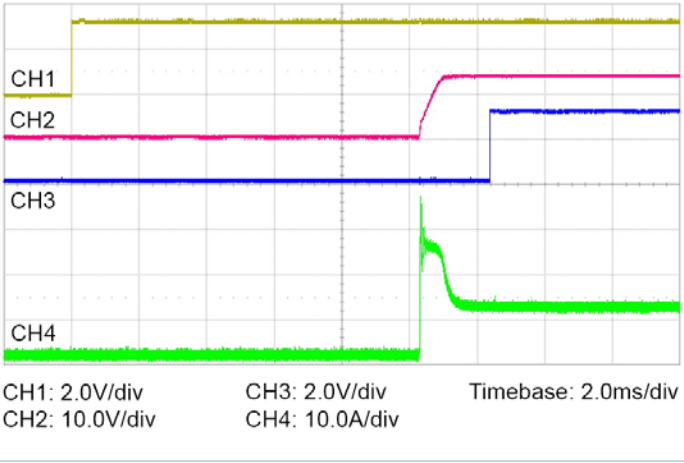



***Figure 18*** — *Start up from application of EN with pre-applied $V_{PRI_DC}$ = 42V, 20% $I_{SEC_DC}$, 100% $C_{SEC_OUT_EXT}$*

## General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Mechanical** | | | | | | |
| Length | L | | 60.87 / [2.396] | 61.00 / [2.402] | 61.13 / [2.407] | mm/[in] |
| Width | W | | 24.76 / [0.975] | 25.14 / [0.990] | 25.52 / [1.005] | mm/[in] |
| Height | H | | 7.21 / [0.284] | 7.26 / [0.286] | 7.31 / [0.288] | mm/[in] |
| Volume | Vol | Without Heatsink | | 11.13 / [0.679] | | $cm^3$/[$in^3$] |
| Weight | W | | | 41 / [1.45] | | g/[oz] |
| Lead finish | | Nickel | 0.51 | | 2.03 | µm |
| | | Palladium | 0.02 | | 0.15 | |
| | | Gold | 0.003 | | 0.051 | |
| **Thermal** | | | | | | |
| Operating Temperature | $T_{INTERNAL}$ | NBM6123T46C15A6T0R (T-Grade) | -40 | | 125 | °C |
| Thermal Resistance Top Side | $r\phi_{INT-TOP}$ | Estimated thermal resistance to maximum temperature internal component from isothermal top | | 1.36 | | °C/W |
| Thermal Resistance Leads | $\phi_{INT-LEADS}$ | Estimated thermal resistance to maximum temperature internal component from isothermal leads | | 1.36 | | °C/W |
| Thermal Resistance Bottom Side | $r\phi_{INT-BOTTOM}$ | Estimated thermal resistance to maximum temperature internal component from isothermal bottom | | 1.24 | | °C/W |
| Thermal Capacity | | | | 34 | | Ws/°C |
| **Assembly** | | | | | | |
| Storage temperature | | NBM6123T46C15A6T0R (T-Grade) | -40 | | 125 | °C |
| ESD Withstand | $ESD_{HBM}$ | Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV) | | | | |
| | $ESD_{CDM}$ | Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V) | | | | |

## General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| | | | | | | |
|---|---|---|---|---|---|---|
| **Soldering[1]** | | | | | | |
| Peak Temperature Top Case | | | | | 135 | °C |
| **Safety** | | | | | | |
| Isolation voltage / Dielectric test | $V_{HIPOT}$ | PRIMARY to SECONDARY | **N/A** | | | V |
| | | PRIMARY to CASE | **2250** | | | |
| | | SECONDARY to CASE | **2250** | | | |
| Isolation Capacitance | $C_{PRI_SEC}$ | Unpowered Unit | **N/A** | N/A | **N/A** | pF |
| Insulation Resistance | $R_{PRI_SEC}$ | At 500$V_{DC}$ | **0** | | | MΩ |
| MTBF | | MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer | | 3.34 | | MHrs |
| | | Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled | | 5.26 | | MHrs |
| Agency Approvals / Standards | | cTUVus; EN 60950-1 | | | | |
| | | cURus; UL 60950-1 | | | | |
| | | CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable | | | | |

[1] Product is not intended for reflow solder attach.

## Sine Amplitude Converter™ Point of Load Conversion

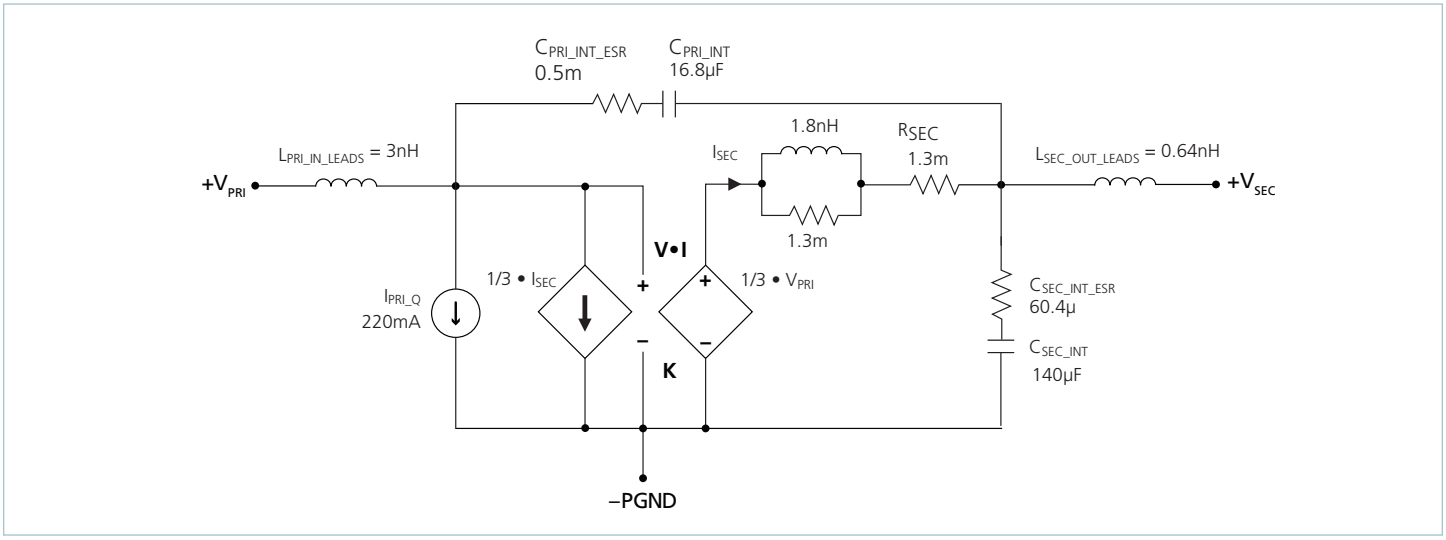



***Figure 19*** — *NBM module AC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from Primary to secondary and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of primary voltage and seconday current. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving high power density.

The NBM6123x46C15A6yzz SAC can be simplified into the preceeding model.

At no load:

$$V_{SEC} = V_{PRI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC.
Rearranging Eq (1):

$$K = \frac{V_{SEC}}{V_{PRI}} \qquad (2)$$

In the presence of load, $V_{SEC}$ is represented by:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{SEC} \qquad (3)$$

and $I_{SEC}$ is represented by:

$$I_{SEC} = \frac{I_{PRI} - I_{PRI_Q}}{K} \qquad (4)$$

$R_{SEC}$ represents the impedance of the SAC, and is a function of the $R_{DSON}$ of the primary and secondary MOSFETs and the winding resistance of the power transformer. $I_{PRI_Q}$ represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{SEC}$ = 0Ω and $I_{PRI_Q}$ = 0A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with $V_{PRI}$.

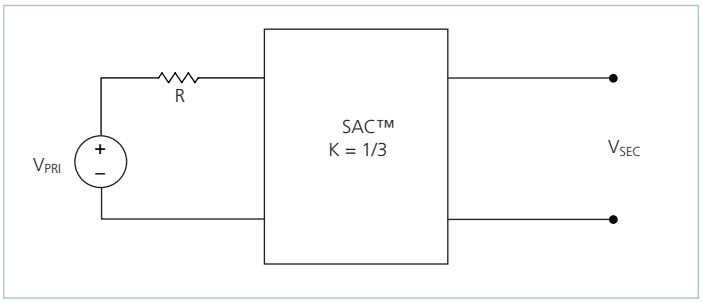



***Figure 20*** — *K = 1/3 Sine Amplitude Converter with series primary resistor*

The relationship between $V_{PRI}$ and $V_{SEC}$ becomes:

$$V_{SEC} = (V_{PRI} - I_{PRI} \bullet R) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) ($I_{PRI_Q}$ is assumed = 0A) into Eq. (5) yields:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where $R_{SEC}$ is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the primary side of the SAC is effectively scaled by $K^2$ with respect to the secondary.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 111mΩ, with K = 1/3.

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the primary of the SAC. A switch in series with $V_{PRI}$ is added to the circuit. This is depicted in Figure 21.

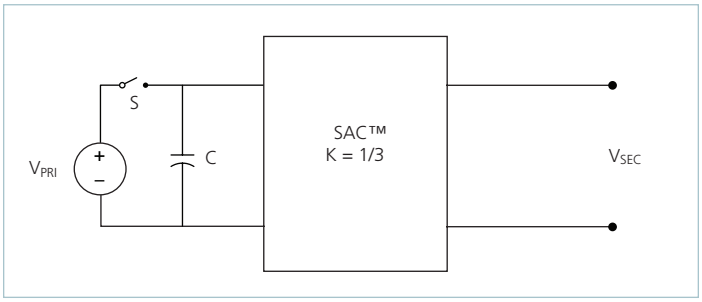



***Figure 21 —*** *Sine Amplitude Converter with primary capacitor*

A change in $V_{PRI}$ with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{PRI}}{dt} \quad (7)$$

Assume that with the capacitor charged to $V_{PRI}$, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{SEC} \bullet K \quad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{SEC} = \frac{C}{K^2} \bullet \frac{dV_{SEC}}{dt} \quad (9)$$

The equation in terms of the secondary has yielded a $K^2$ scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the secondary when expressed in terms of the primary. With a K = 1/3 as shown in Figure 21, C = 1µF would appear as C = 9µF when viewed from the secondary.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the NBM™ module are:

- No load power dissipation ($P_{PRI_NL}$): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{SEC}}$): refers to the power loss across the NBM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{PRI_NL} + P_{R_{SEC}} \quad (10)$$

Therefore,

$$P_{SEC_OUT} = P_{PRI_IN} - P_{DISSIPATED} = P_{PRI_IN} - P_{PRI_NL} - P_{R_{SEC}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{SEC_OUT}}{P_{PRI_IN}} = \frac{P_{PRI_IN} - P_{PRI_NL} - P_{R_{SEC}}}{P_{PRI_IN}} \quad (12)$$

$$= \frac{V_{PRI} \bullet I_{PRI} - P_{PRI_NL} - (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}}$$

$$= 1 - \left( \frac{P_{PRI_NL} + (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}} \right)$$

## Input and Output Filter Design

A major advantage of SAC™ systems versus conventional PWM converters is that the auto-transformer based SAC does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of primary voltage and secondary current and efficiently transfers charge through the auto-transformer. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:

  To take full advantage of the NBM™ module's dynamic response, the impedance presented to its primary terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the primary should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- Further reduce primary and/or secondary voltage ripple without sacrificing dynamic response:

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the primary source will appear at the secondary of the module multiplied by its K factor.

- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:

  The module primary/secondary voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating primary range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Total load capacitance of the NBM module shall not exceed the specified maximum. Owing to the wide bandwidth and low secondary impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the primary of the module. At frequencies <500kHz the module appears as an impedance of $R_{SEC}$ between the source and load.

Within this frequency range, capacitance at the primary appears as effective capacitance on the secondary per the relationship defined in Eq. (13).

$$C_{SEC_EXT} = \frac{C_{PRI_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

## Thermal Considerations

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum current that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for a NBM module 6123 in an application where the top, bottom, and leads are cooled. In this case, the NBM power dissipation is $PD_{TOTAL}$ and the three surface temperatures are represented as $T_{CASE_TOP}$, $T_{CASE_BOTTOM}$, and $T_{LEADS}$. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation would provide an estimate of heat flow through the various pathways as well as internal temperature.

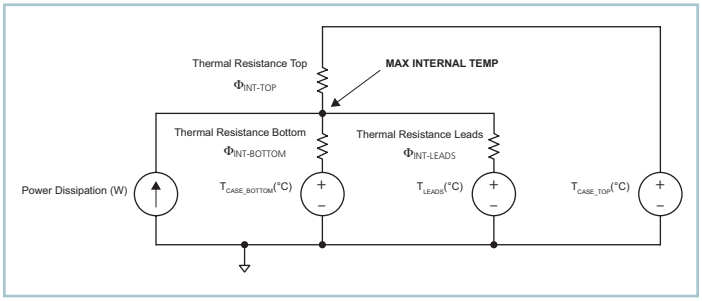



***Figure 22*** — *Top case, Bottom case and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE_TOP}$$
$$T_{INT} - PD_2 \bullet \Phi_{INT\text{-}BOTTOM} = T_{CASE_BOTTOM}$$
$$T_{INT} - PD_3 \bullet \Phi_{INT\text{-}LEADS} = T_{LEADS}$$
$$PD_{TOTAL} = PD_1 + PD_2 + PD_3$$

Where $T_{INT}$ represents the internal temperature and $PD_1$, $PD_2$, and $PD_3$ represent the heat flow through the top side, bottom side, and leads respectively.

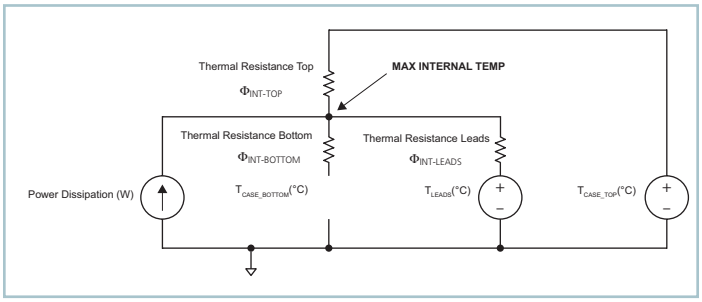



***Figure 23*** — *Top case and leads thermal model*

Figure 23 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE_TOP}$$

$$T_{INT} - PD_3 \bullet \Phi_{INT\text{-}LEADS} = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_3$$

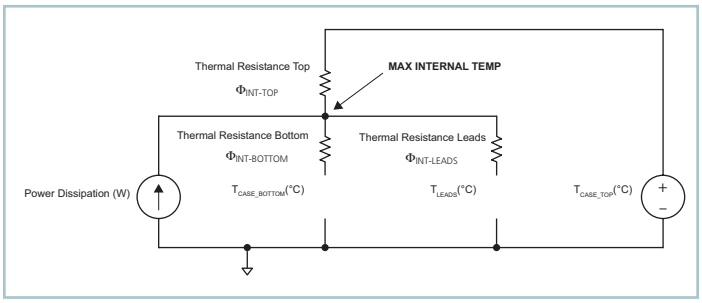



***Figure 24*** — *Top case thermal model*

Figure 24 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow paths to the bottom and leads are left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE_TOP}$$

$$PD_{TOTAL} = PD_1$$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a NBM™ thermal configuration is valid for a given condition. These tools can be found at: http://www.vicorpower.com/powerbench.

## Current Sharing

The performance of the SAC™ topology is based on efficient transfer of energy through an auto-transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal auto-transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple NBM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- An input filter is required for an array of NBMs in order to prevent circulating currents.

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

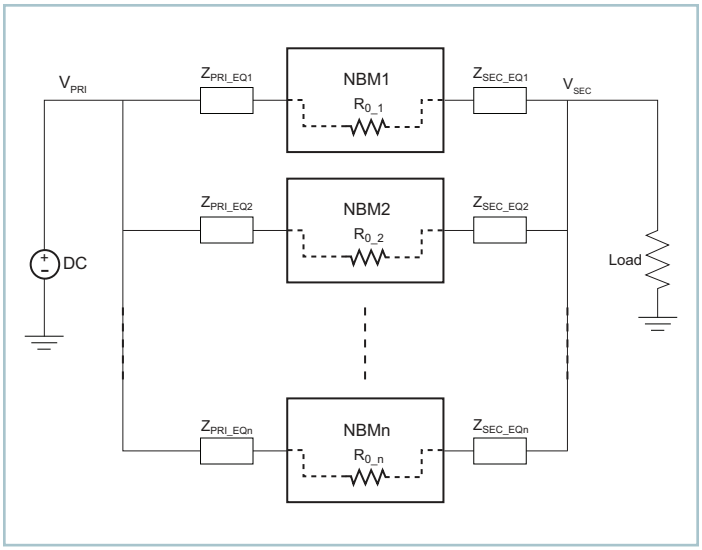



***Figure 25*** — *NBM module array*

## Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of NBM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting $I^2t$
- Recommend fuse: ≤ 60A Littelfuse TLS Series (primary side)

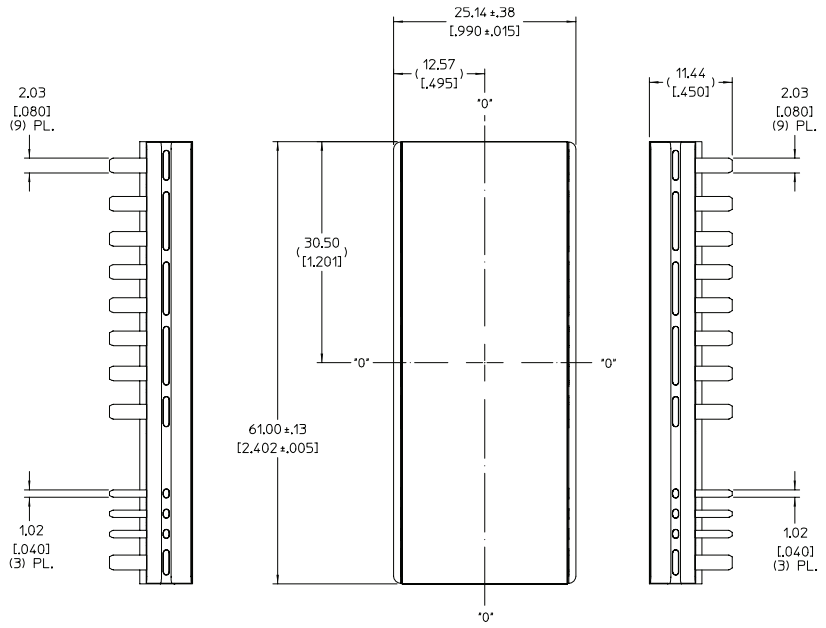
## Startup and Reverse Operation

The NBM6123T46C15A6T0R is capable of startup in forward and reverse direction once the applied voltage is greater than the undervoltage lockout threshold.

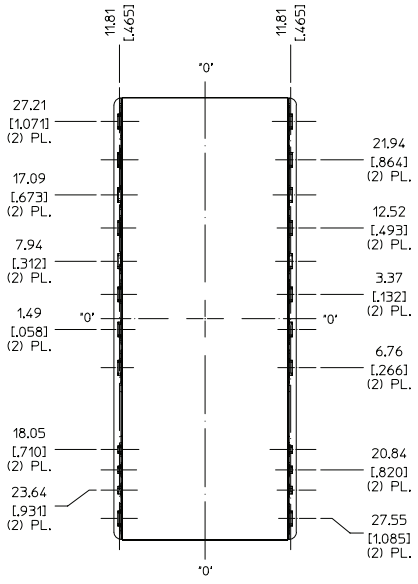
The non-isolated bus converter modules are capable of reverse power operation. Once the unit is enabled, energy can be transferred from secondary back to the primary whenever the secondary voltage exceeds $V_{PRI} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

Startup loading could be set to no greater than 20% of rated max current respectively in forward or reverse direction. A load must not be present on the $+V_{PRI}$ pin if the powertrain is not actively switching. Remove $+V_{PRI}$ load prior to disabling the module using EN pin. Primary MOSEFT body diode conduction will occur if unit stops switching while a load is present on the $+V_{PRI}$ and $+V_{SEC}$ voltage is two diodes drop higher than $+V_{PRI}$.

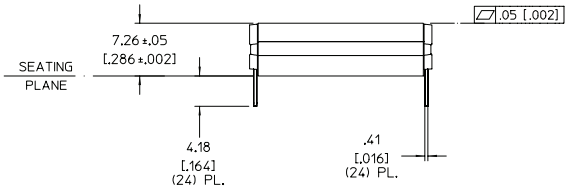
## NBM™ Module Through Hole Package Mechanical Drawing and Recommended Land Pattern




TOP VEIW (COMPONENT SIDE)

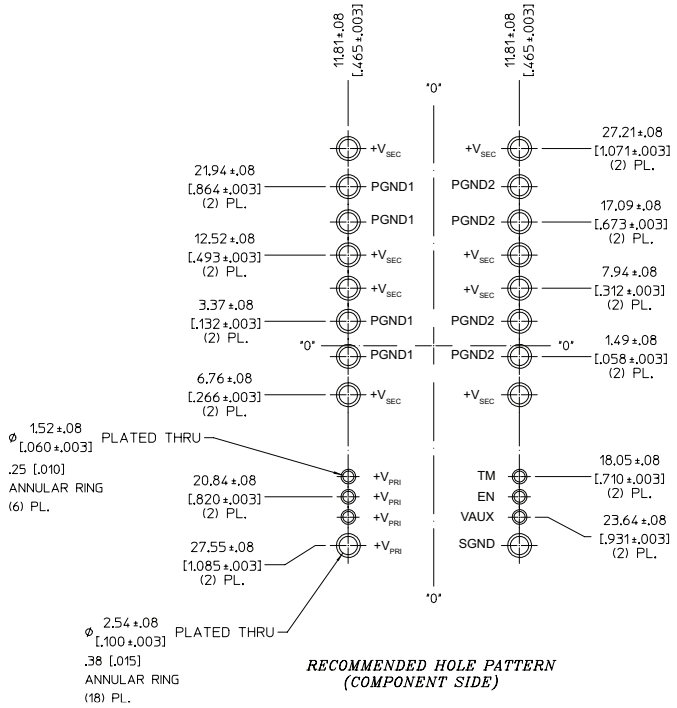



BOTTOM VIEW




NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.




RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)

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**Vicor Corporation**
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

**email**
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com