

JTAG Test Controller

Description

The AS91L1001 device provides an interface between the 60x bus on the Motorola MPC8260 processor and two totally independent IEEE1149.1 interfaces, namely, the primary and secondary ports. It handles all the protocol for the 60x bus to write and read directly to registers within the device with no additional glue logic.

The AS91L1001 has three distinct modes of operation, namely Slave mode, Master mode, and 3rd Party Support mode. These different modes control how data will be transferred on the IEEE1149.1 buses.

Slave mode: This is the default mode after the AS91L1001 has received a power-on reset. In this mode, there is a transparent connection between the primary and secondary JTAG ports. The processor interface is not used in the slave mode. This configuration is typically used to test a line card from a system back plane (the primary port is usually connected to the back plane and the secondary port is connected to the onboard JTAG

chain). Once testing from the system back plane is completed, the AS91L1001 is reconfigured for master mode operation through a register. The master mode of operation is used to test the onboard JTAG chain, using the microprocessor interface.

Master mode: This mode is accessed via a command to a AS91L1001 register. The key feature of this mode is that both the Primary and Secondary are now both totally independent IEEE1149.1 bus masters, which enable concurrent operation on both the IEEE1149.1 channels. The Master mode enables the primary IEEE1149.1 channel to be used to access other PCB's connected via the 5-wire IEEE1149.1 interface on the back plane.

The secondary IEEE1149.1 port is used to test the card that is hosting the AS91L1001. This mode may be used for performing Interconnect testing or Flash/CPLD programming.

Key Features

- Interprets between the Motorola MPC8260 processor and two IEEE1149.1 ports
- Three distinct modes of operation: Slave mode, Master mode, and 3rd Party support mode
- Supports a wide range of 3rd Party tools
- Pinout and feature set compatible (complete second source) with the Firecron JTS01 device
- Available in a 100-pin LQFP or a 100-pin FPBGA lead free package

Device Block Diagram

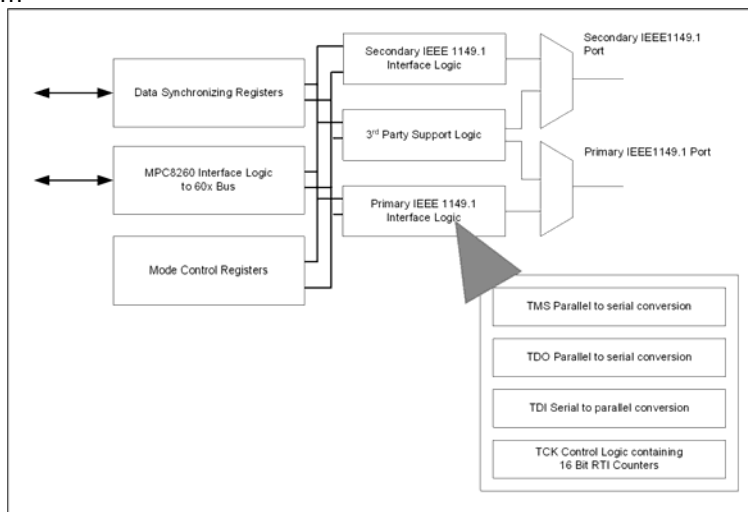


Figure 1 - AS91L1001 JTAG Test Controller



Description (Cont.)

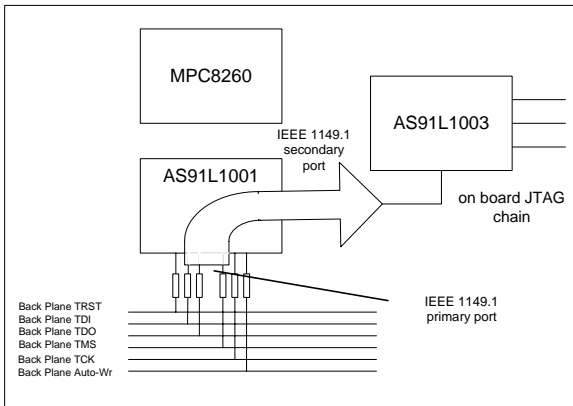


Figure 2 - Slave mode

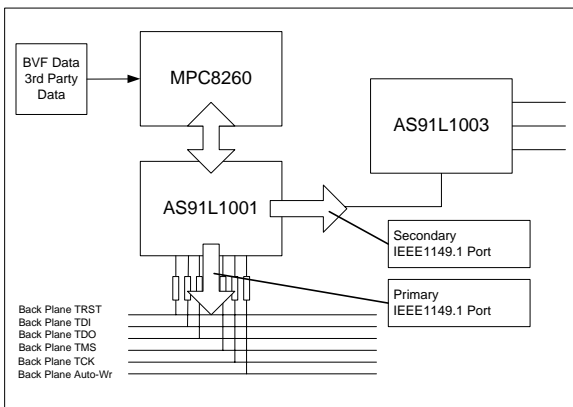


Figure 3 - Master mode

3rd Party Support mode: This mode is intended to support legacy FPGA/CPLD 1149.1 devices that require adaptive programming algorithms to ensure data retention, due to the fact that decision branching is not supported in Service Vector Format (SVF). This mode will not be required for devices that adhere to the IEEE1532 specification, as IEEE1532 compliant parts from all CPLD/FPGA vendors adhere to this open standard. The 3rd Party support mode which is accessible via control registers in the AS91L1001 selects one of the IEEE1149.1 ports to operate with the standard SVF->BVF flow while the remaining IEEE1149.1 port will support commands for the embedded C Code routines provided by FPGA/CPLD vendors. This eliminates any issues regarding data retention when using the AS91L1001 on a PCB.

Alliance Semiconductor supplies a Windows™ executable that converts industry standard SVF into Alliance Semiconductor proprietary BVF file format. Users of the ANSI C Code are only required to provide the base read and write function for the stream I/O. So in order to execute a BVF file, the user has to call the primary C function, which will then perform all the required setup of the AS91L1001 along with obtaining the BVF file to process at the required time or report any errors if applicable.

If the user wishes to embed the ANSI C routines from FPGA/CPLD vendors, then this is handled in a very similar manner. As one of the IEEE1149.1 ports will be operating in Alliance Semiconductor BVF mode, the method of reading and writing data is the same as before. However, the user will need to consult the 3rd party routines to see how the data flow is performed. Ultimately, the user will call a Alliance Semiconductor provided C routine that will set the AS91L1001 for 3rd party support on one of the IEEE1149.1 channels while the other will be used for executing the 3rd party code.

In summary, 3rd Party Support mode enables serial shifting of data on any of the two JTAG ports and is used to configure legacy FPGA/CPLD devices.

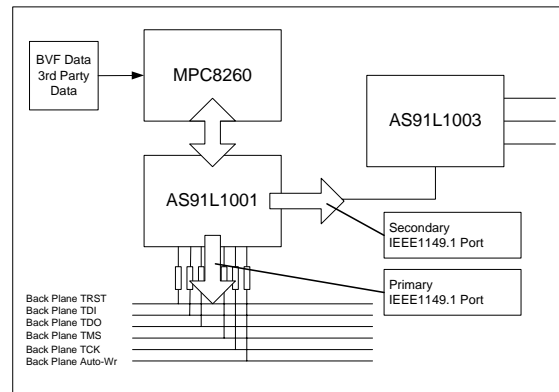


Figure 4 - 3rd Party support mode



Signal Description

| PIN NAME | PIN TYPE | PIN NUMBER LQFP | PIN NUMBER FPBGA | DESCRIPTION |
|--------------------------------|----------|-----------------|------------------|---|
| RESETn | IN | 14 | F4 | This active low reset signal resets the AS91L1001 and places the device in Slave mode |
| JTS03_06_SELECTEDn | IN | 65 | E10 | This active low input from either a AS91L1003 or AS91L1006 provides the control status of the AS91L1003/06 connected to the Secondary port of the AS91L1001 (operating in Slave mode) |
| Primary IEEE1149.1 Port | | | | |
| PRIM_TDI | INOUT | 19 | G3 | IEEE1149.1 Primary Test Data Input in Slave mode; in Master mode, this pin acts as Test Data Output |
| PRIM_TDO | INOUT | 20 | G1 | IEEE1149.1 Primary Test Data Output in Slave mode; in Master mode, this pin acts as Test Data Input |
| PRIM_TRST | INOUT | 22 | H2 | IEEE1149.1 Primary Test Reset Input in Slave mode; in Master mode, this pin is an output |
| PRIM_TMS | INOUT | 21 | G2 | IEEE1149.1 Primary Test Mode Select in Slave mode; in Master mode, this pin is an output |
| PRIM_TCK | INOUT | 87 | A6 | IEEE1149.1 Primary Test Clock in Slave mode; in Master mode, this pin is an output |
| PRIM_AUTOWR | IN | 16 | F1 | Primary Auto-write input controlled by test equipment to shorten Flash memory programming, signal is driven low for write pulse |
| SECONDARY IEEE1149.1 | | | | |
| SEC_TDO | OUT | 57 | G10 | IEEE1149.1 Test Data Output on Secondary port |
| SEC_TDI | IN | 58 | G8 | IEEE1149.1 Test Data Input on Secondary port |
| SEC_TRST | OUT | 64 | E9 | IEEE1149.1 Test Logic Reset on Secondary port |
| SEC_TMS | OUT | 60 | F9 | IEEE1149.1 Test Mode Select Out on Secondary port |
| SEC_TCK | OUT | 61 | F10 | IEEE1149.1 Test Clock Out on Secondary port |
| SEC_AUTOWR | OUT | 63 | F7 | Secondary Auto-Write Output controlled by test equipment to shorten Flash memory programming, signal is driven low for write pulse |



| PIN NAME | PIN TYPE | PIN NUMBER LQFP | PIN NUMBER FPBGA | DESCRIPTION |
|-------------|----------|---------------------------------------|--|---|
| SLAVE_MODE | OUT | 71 | | This signal, when low, indicates that the AS91L1001 is in Slave mode of operation |
| MASTER_MODE | OUT | 72 | | This signal, when low, indicates that the AS91L1001 is in the Master mode of operation |
| PRIM_TDO_OE | OUT | 27 | | This active low signal derived while in Slave Mode, provides the control for additional current drive to the buffer on the primary TDO signal |
| DATA(7:0) | INOUT | 98,97,96,94,93,92,85,84 LSB-MSB | A3,B3,A4,B4,C4,C5,C6,C7 LSB-MSB) | 8-bit data bus for the processor interface |
| ADDR(31:28) | IN | 83,81,80,79 LSB-MSB | B7,A7,B8,A8 LSB-MSB) | 4-bit address bus for the processor interface |
| WRn | IN | 77 | B9 | Active low, write enable signal for the processor interface |
| RDn | IN | 76 | B10 | Active low read enable signal for the processor interface |
| CSn | IN | 78 | A9 | Active low, chip select signal for the processor interface |
| OSC_IN | IN | 75 | C10 | This is the master clock into the AS91L1001 device |
| TOE | IN | 88 | B6 | Test output enable this signal when taken low tristates all devices I/O |
| GND | POWER | 11,26,43,59,74,95,2,17,90,55,56,38,86 | D6,G5,C3,J9,G9,D7,E5,F6,G4,H8,A5,F2,B1 | AS91L1001 Ground connection |
| VCC | POWER | 39,91,3,18,34,51,66,82,23,54 | D5, G6, C8, D4, E6, F5, G7, H3, H1, H9 | AS91L1001 VCC connection |
| ASIC_TCK | IN | 62 | F8 | IEEE1149.1 ASIC Test |
| ASIC_TMS | IN | 15 | F3 | IEEE1149.1 ASIC Test |
| ASIC_TDO | OUT | 73 | | IEEE1149.1 ASIC Test |
| ASIC_TDI | IN | 4 | | IEEE1149.1 ASIC Test |



| PIN NAME | PIN TYPE | PIN NUMBER LQFP | PIN NUMBER FPBGA | DESCRIPTION |
|-------------|----------|--|--|-------------|
| No connects | | 1,5,6,7,8,9, 10,12,13,24 ,25,27,28, 29,30,31,32 ,33, 35,36,37,40 ,41, 42,44,45,46 ,47, 48,49,50,52 ,53, 67,68,69,70 ,71, 72,89,99,10 0 | C1,B5,E4,E3, E1,E2,A2,B2, C2,D3,D1,D2, J1,K1,K2,C9, D8,D10,D9,E 7,E8,J2,K3,J3 ,H4,J4,K4,H5, J5,K5,K6,J6,H 6,K7,J7,H7,J8 ,K8,K10,J10, H10 | |

Table 1 - AS91L1001 Signal Description

Absolute Maximum Ratings

| Parameter | Maximum Range |
|--|----------------------|
| Supply Voltage (Vcc) | -0.3V to 5.5V |
| DC Input Voltage (Vi) | -0.5V to Vcc +0.5V |
| Max sink current when Vi = -0.5V | -20mA |
| Max source current when Vi = Vcc + 0.5V | +20mA |
| Max Junction Temperature with power applied Tj | +125 degrees C |
| Max Storage temperature | -55 to +150 degree C |

Table 2 - Absolute Maximum Ratings



Note: Stress above the stated maximum values may cause irreparable damage to the device, correct operation of the device at these values is not guaranteed.



Recommended Operating Conditions

| Parameter | Operating Range |
|--|---------------------------------------|
| Supply Voltage (Vcc) | 3.0V to 3.6V |
| Input Voltage (Vi) | 0V to Vcc |
| Output Voltage (Vo) | 0V to Vcc |
| Operating Temperature (Ta) Commercial | 0 C to 70 C |
| Industrial (Ta) | -40 deg C to +85 deg C, 3.00V to 3.6V |

Table 3 - Recommended Operating Conditions

DC Electrical Characteristics

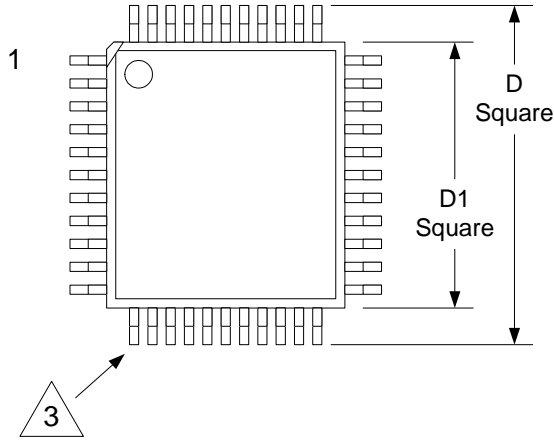
| Symbol | Parameter | Min | Max | Condition |
|------------------|----------------------------------|-------|--------------|--|
| V _{IH} | Minimum High Input Voltage | 2.0 | 5.25 | |
| V _{IL} | Maximum Low Input Voltage | -0.3V | 0.8V | |
| | | | | |
| Symbol | Parameter | | Value | Condition |
| V _{OH} | Minimum High Output Voltage | | 2.4V | I _{oh} =24mA or 8mA as defined by pin |
| V _{OL} | Minimum Low Output Voltage | | 0.4V | I _{ol} =24mA or 8mA as defined by pin |
| I _{oz} | Tristate output leakage | | -10 or 10 mA | |
| I _{cc} | Maximum quiescent supply current | | 2mA | |
| I _{ccd} | Maximum dynamic supply current | | 80mA | TCK freq equal to 10 MHz |

Table 4 - AS91L1001 DC Electrical Characteristics



Packaging Information

The AS91L1001 is available in a 100-pin LQFP or a 100-pin FPBGA lead free package.



| SYMBOL | LEADS | | 100 LEAD | |
|-------------|-------|-----|----------|--------------------|
| | TOL. | | | |
| A | MAX. | | 1.60 | |
| A1 | MIN | MAX | 0.05 | 0.15 |
| A2 | MIN | NOM | MAX | 1.35 / 1.40 / 1.45 |
| D | BASIC | | 18.00 | |
| D1 | BASIC | | 14.00 | |
| L | ±0.15 | | 0.60 | |
| L1 | REF | | 1.00 | |
| b | MIN | MAX | 0.17 | 0.27 |
| e | BASIC | | 0.50 | |
| ccc | MAX | | 0.08 | |
| ddd | NOM | | 0.08 | |
| JEDEC REF # | | | MS-026 | |

- NOTES:
 1. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
 2. PLASTIC BODY DIMENSIONS DO NOT INCLUDE FLASH OR PROTUSION. MAX ALLOWABLE 0.25 PER SIDE.
 3. LEAD COUNT ON DRAWING NOT REPRESENTATIVE OF ACTUAL PACKAGE.

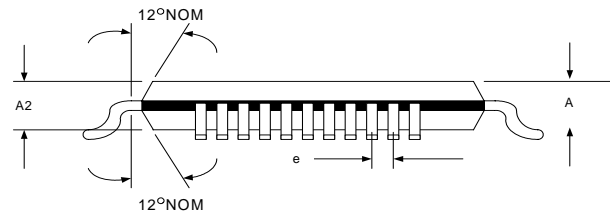
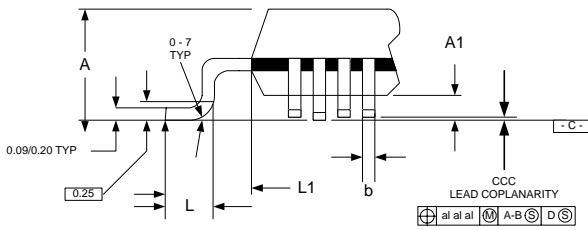
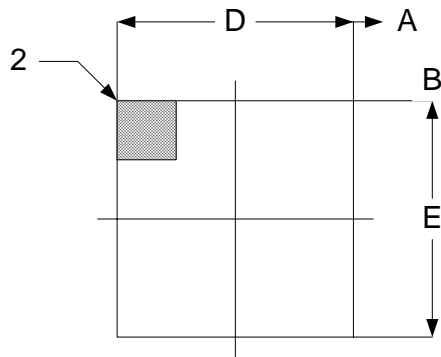
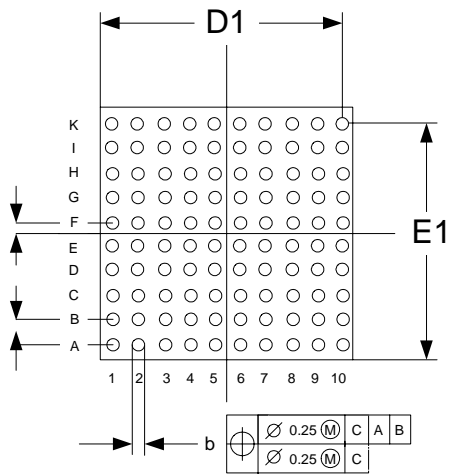
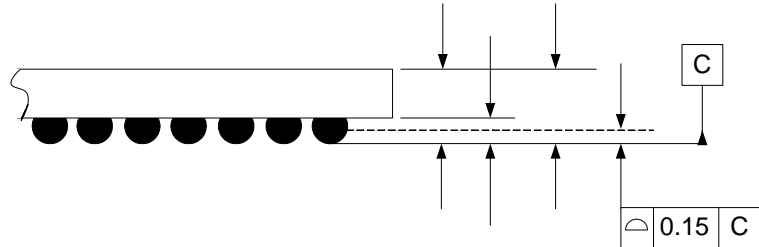


Figure 6 - LQFP-100



| Revisions | | | |
|-----------|--|-------|----------|
| REV. | DESCRIPTION | ECN | DATE |
| A | Initial document release. | 91253 | 12-04-01 |
| B | Updated ball coplanarity limits from 0.20mm to 0.15mm. | | |



| DIMENSIONS | | | |
|----------------|-------------------|------|------|
| SYMBOL | MIN. | NOM. | MAX. |
| A | -- | -- | 1.70 |
| A1 | 0.30 | -- | -- |
| A2 | 0.25 | -- | 1.10 |
| b | 0.50 | 0.60 | 0.70 |
| D | 11.00 BSC | | |
| D1 | 9.00 BSC | | |
| E | 11.00 BSC | | |
| E1 | 9.00 BSC | | |
| e | 1.00 | | |
| PACKAGE NUMBER | FBGA0100-11F | | |
| JEDEC REF # | MO-192 VAR. AAC-1 | | |

Figure 7 - FPBGA-100



Device Selector Guide and Ordering Information

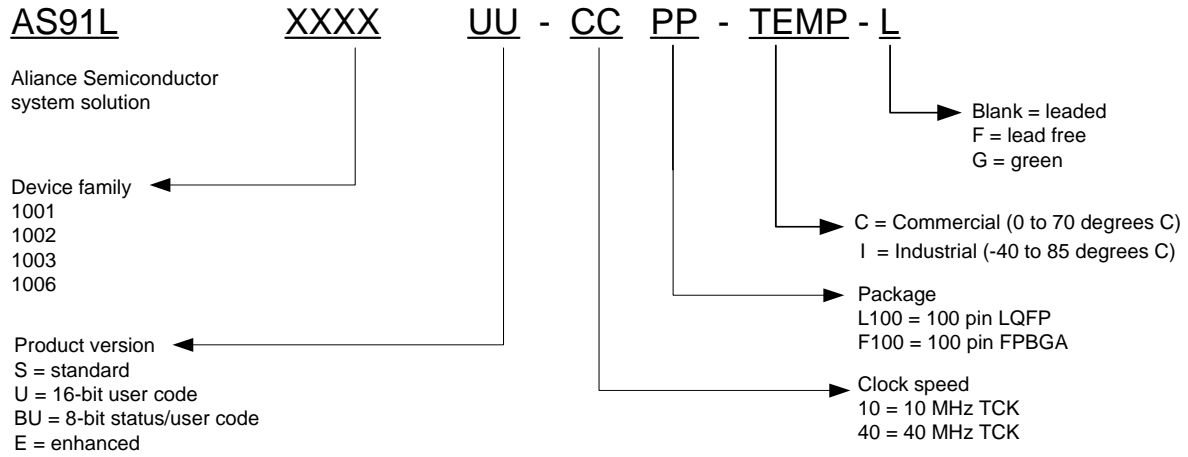


Figure 8 - Part Numbering Guide



| Part Number | Description |
|------------------------|---|
| AS91L1001S – 10L100-C | JTAG Test Controller, 100-pin LQFP package, commercial |
| AS91L1001S – 10L100-CF | JTAG Test Controller, 100-pin LQFP package, commercial, lead free |
| AS91L1001S – 10L100-I | JTAG Test Controller, 100-pin LQFP package, industrial |
| AS91L1001S – 10L100-IF | JTAG Test Controller, 100-pin LQFP package, industrial, lead free |
| AS91L1001S – 10F100-C | JTAG Test Controller 100-pin FPBGA package, commercial |
| AS91L1001S – 10F100-CG | JTAG Test Controller 100-pin FPBGA, commercial, green package |
| AS91L1001S – 10F100-I | JTAG Test Controller 100-pin FPBGA package, industrial |
| AS91L1001S – 10F100-IG | JTAG Test Controller 100-pin FPBGA, industrial, green package |
| AS91L1001S – 40L100-CF | JTAG Test Controller, 100-pin LQFP package, commercial, lead free, 40 MHz TCK |
| AS91L1001S – 40L100-IF | JTAG Test Controller, 100-pin LQFP package, industrial, lead free, 40 MHz TCK |
| AS91L1001S – 40F100-CG | JTAG Test Controller 100-pin FPBGA, commercial, green package, 40 MHz TCK |
| AS91L1001S – 40F100-IG | JTAG Test Controller 100-pin FPBGA, industrial, green package, 40 MHz TCK |

Table 5 - Valid Part Number Combinations



| Device Master | Description | Package Options | |
|---------------|----------------------|--------------------------|----------|
| | | FPBGA-100 (1mm pitch) | LQFP-100 |
| AS91L1001 | JTAG Test Controller | X | X |
| AS91L1002 | JTAG Test Sequencer | X | X |
| AS91L1003U | 3-Port Gateway | X | X |
| AS91L1006BU | 6-Port Gateway | X | X |

Table 6 - JTAG Controller Product Family

