

### Features

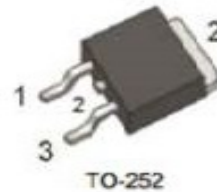
- $R_{DS(ON)} < 110m\Omega @ V_{GS}=10V$
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent  $CdV/dt$  effect decline
- Lead free in compliance with EU RoHS directive.
- Green molding compound

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
100	110@ $V_{GS}=10V$	15

### Mechanical Data

- Case: TO-252



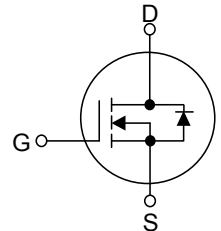
Pin Definition:

1. Gate
2. Drain
3. Source

### Ordering Information

Part No.	Package	Packing
DMD15N10-TR	TO-252	2.5Kpcs / 13" Reel
DMD15N10-TU	TO-252	75pcs / Tube

### Block Diagram



### ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ C$ , unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup>	$I_D @ T_C=25^\circ C$	15.0	A
Continuous Drain Current <sup>1</sup>	$I_D @ T_C=70^\circ C$	13.8	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	24	A
Total Power Dissipation <sup>4</sup>	$P_D @ T_C=25^\circ C$	34.7	W
Total Power Dissipation	$P_D @ T_A=25^\circ C$	2	W
Single Pulse Avalanche Energy <sup>3</sup>	EAS	8	mJ
Avalanche Current	$I_{AS}$	11	A
Operating Junction and Storage Temperature Range	$T_j, T_{stg}$	-55 ~ +150	$^\circ C$

### THERMAL DATA

Parameter	Symbol	Max. Value	Unit
Thermal Resistance Junction-ambient <sup>1</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$
Thermal Resistance Junction-case <sup>1</sup>	$R_{\theta JC}$	3.6	$^\circ C/W$

**ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	100	-	-	V	V <sub>GS</sub> =0, I <sub>D</sub> =250μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.0	-	2.5	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
Gate-Source Leakage Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V
Drain-Source Leakage Current	I <sub>DSS</sub>	-	-	1.0	μA	V <sub>DS</sub> =80V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	-	-	110	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =8A
		-	-	120		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>		26.2		nC	I <sub>D</sub> =10A V <sub>DS</sub> =80V V <sub>GS</sub> =10V
Gate-Source Charge	Q <sub>gs</sub>		4.6			
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>		5.1			
Turn-on Delay Time <sup>2</sup>	T <sub>d(on)</sub>	-	4.2	-	ns	V <sub>DS</sub> =50V I <sub>D</sub> =10A V <sub>GS</sub> =10V R <sub>G</sub> =3.3Ω
Rise Time	T <sub>r</sub>	-	8.2	-		
Turn-off Delay Time	T <sub>d(off)</sub>	-	35.6	-		
Fall Time	T <sub>f</sub>	-	9.6	-		
Input Capacitance	C <sub>iss</sub>	-	1535	-	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =15V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	60	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	37	-		
Gate Resistance	R <sub>g</sub>	-	2	-	Ω	f=1.0MHz

**Guaranteed Avalanche Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy <sup>5</sup>	EAS	1.25	-	-	mJ	V <sub>DD</sub> =25V, L=0.1mH, I <sub>AS</sub> =5A

**Source-Drain Diode**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Continuous Source Current <sup>1,6</sup>	I <sub>S</sub>	-	-	15	A	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current
Pulsed Source Current <sup>2,6</sup>	I <sub>SM</sub>	-	-	24	A	
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	1.2	V	V <sub>GS</sub> =0V, I <sub>S</sub> =8A, T <sub>J</sub> =25°C
Reverse Recovery Time	t <sub>rr</sub>	-	37	-	ns	I <sub>F</sub> =10A, dI/dt=100A/μs, T <sub>J</sub> =25°C
Reverse Recovery Charge	Q <sub>rr</sub>	-	27.3	-	nC	

Notes: 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, ≤10sec, 125°C/W at steady state.

2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.

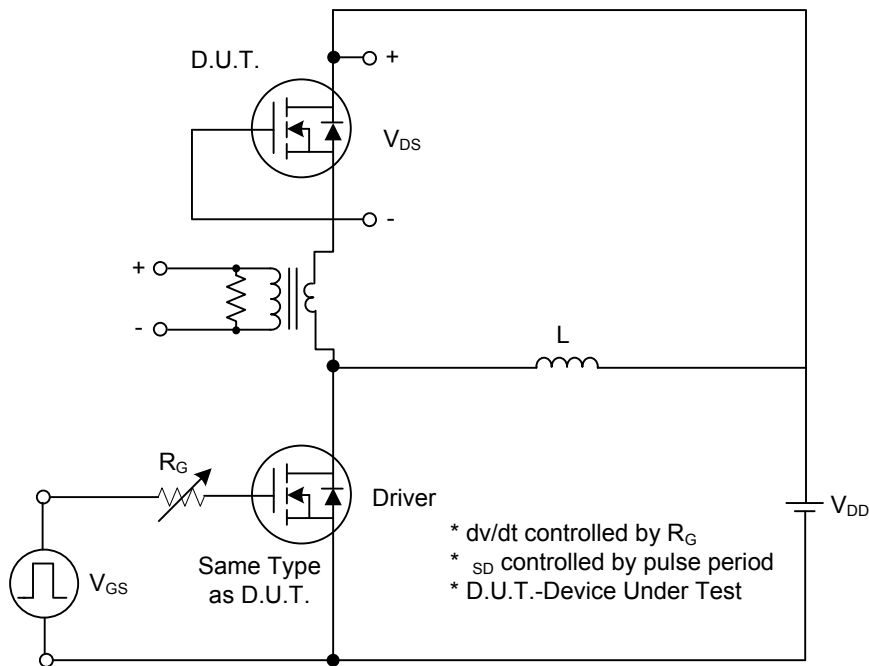
3. The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=11A.

4. The power dissipation is limited by 150°C junction temperature.

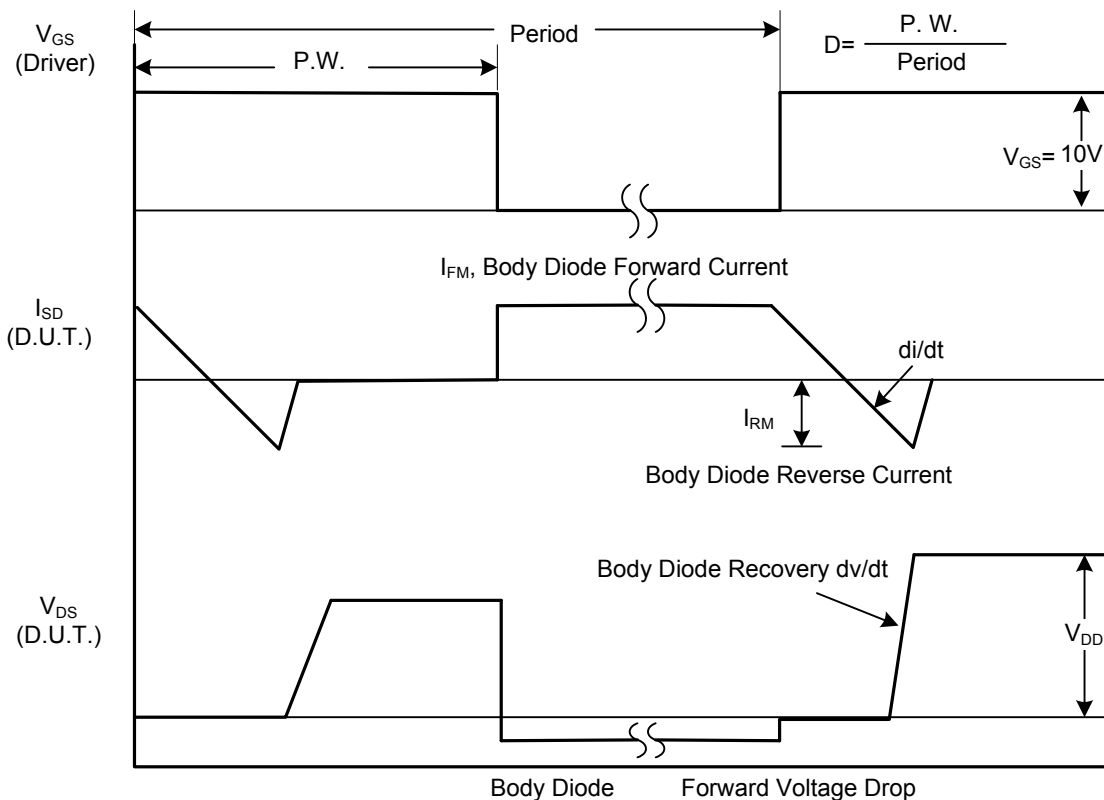
5. The Min. value is 100% EAS tested guarantee.

6. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

### TEST CIRCUITS AND WAVEFORMS

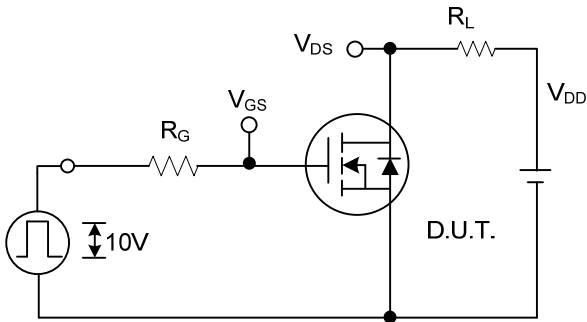


**Peak Diode Recovery dv/dt Test Circuit**

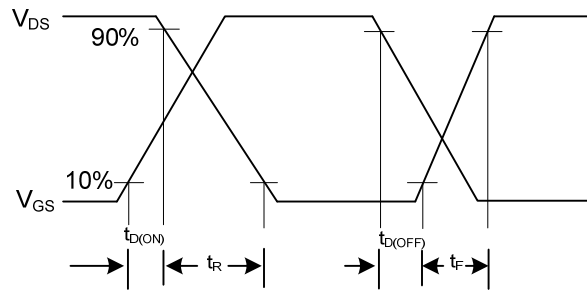


**Peak Diode Recovery dv/dt Waveforms**

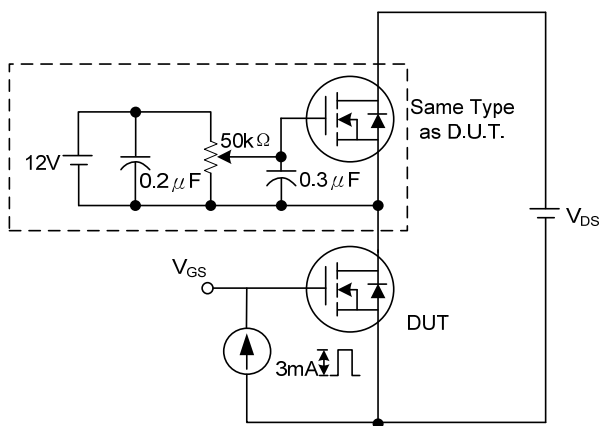
### TEST CIRCUITS AND WAVEFORMS(Cont.)



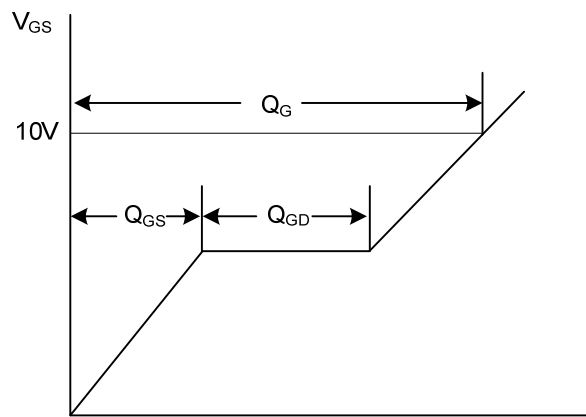
Switching Test Circuit



Switching Waveforms

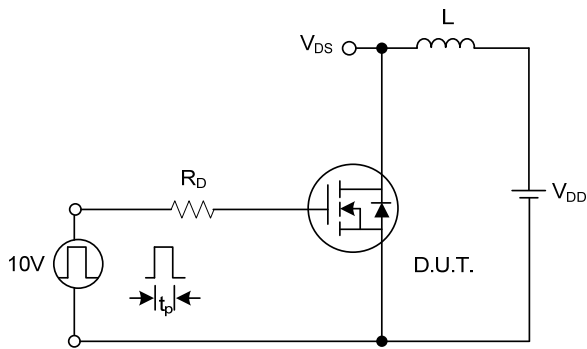


Gate Charge Test Circuit

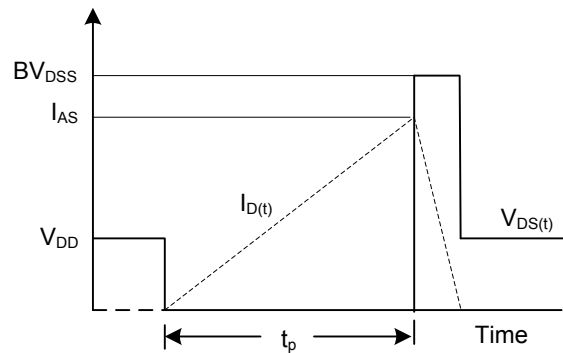


Charge

Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

### TYPICAL CHARACTERISTICS

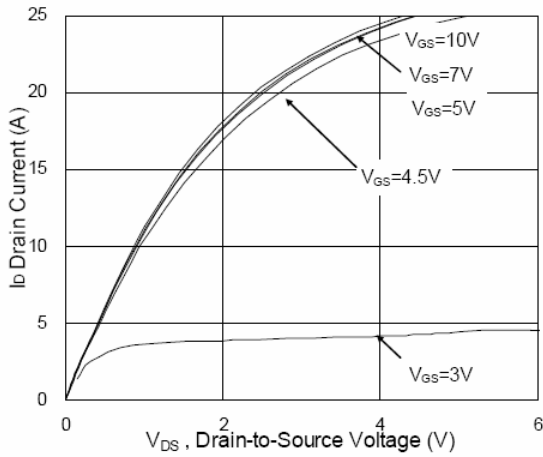


Fig.1 Typical Output Characteristics

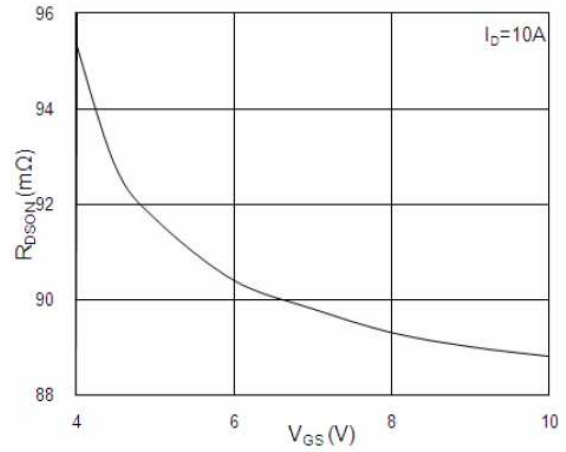


Fig.2 On-Resistance vs. G-S Voltage

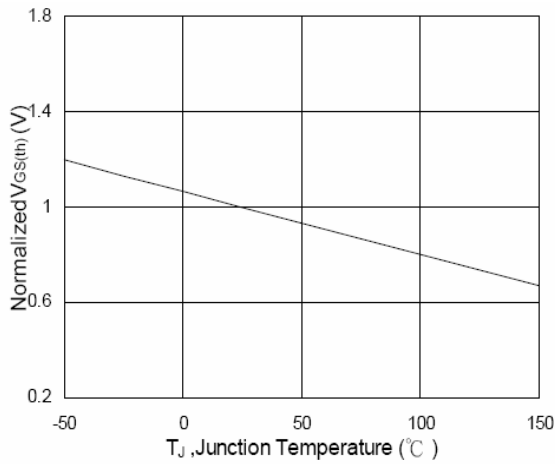


Fig.3 Normalized  $V_{GS(th)}$  vs.  $T_J$

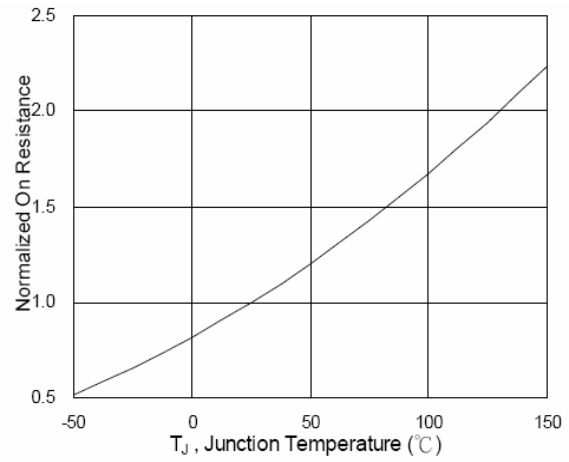


Fig.4 Normalized  $R_{DS(on)}$  vs.  $T_J$

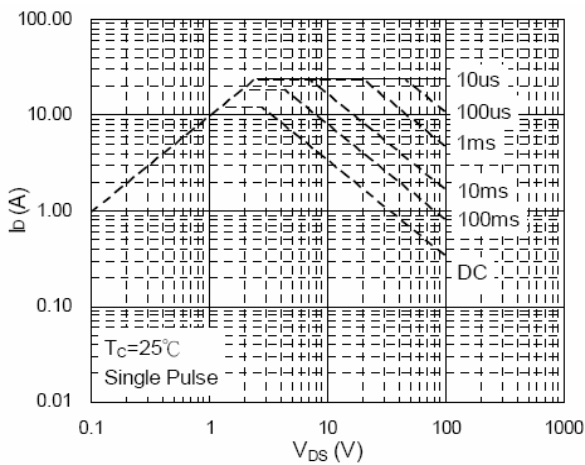


Fig.5 Safe Operating Area

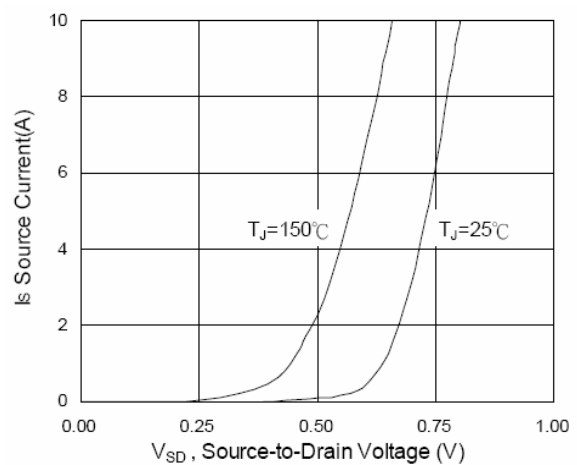


Fig.6 Forward Characteristics of Reverse

### TYPICAL CHARACTERISTICS(Cont.)

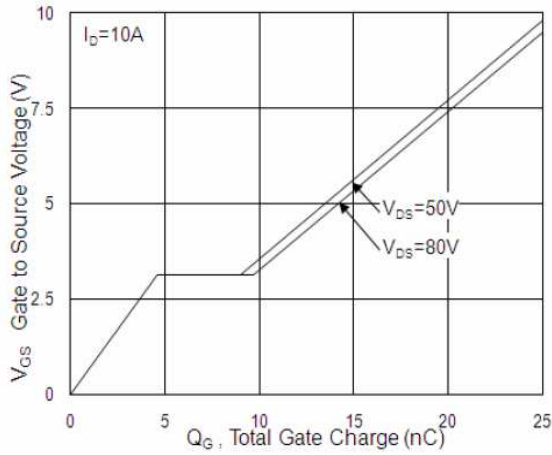


Fig.7 Gate Charge Characteristics

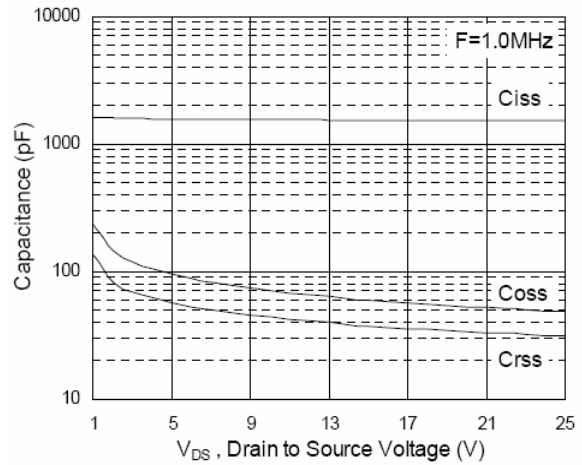


Fig.8 Capacitance Characteristic

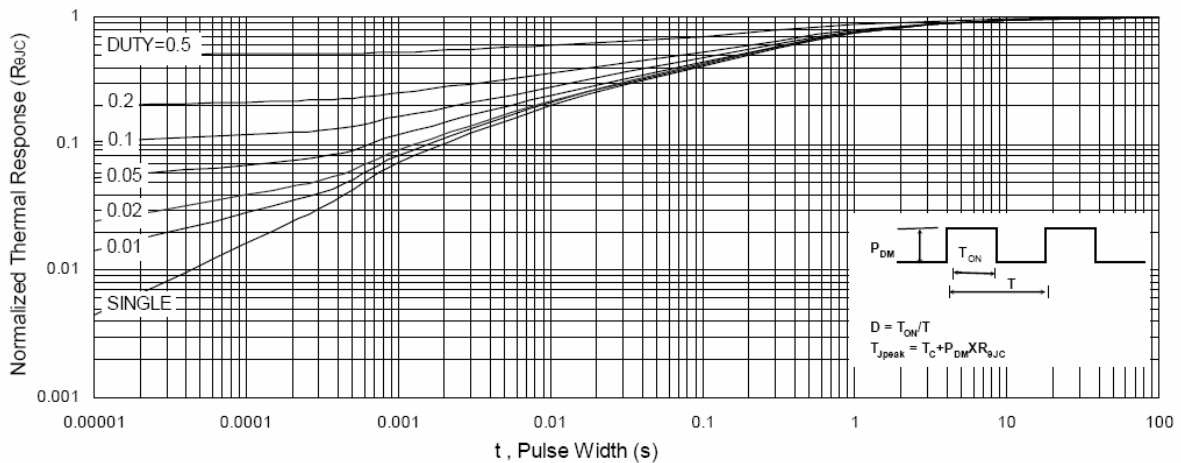


Fig.9 Normalized Maximum Transient Thermal Impedance

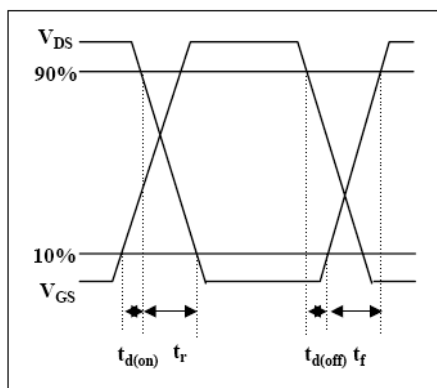


Fig.10 Switching Time Waveform

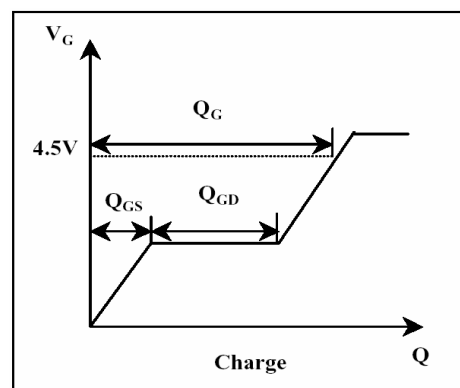
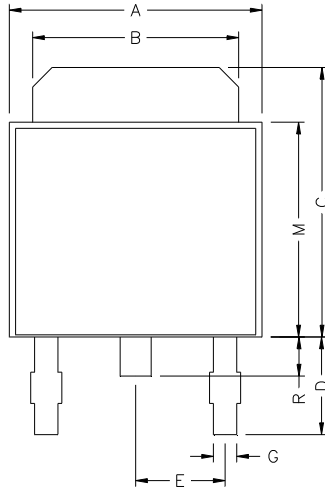


Fig.11 Gate Charge Waveform

**TO-252 Mechanical Drawing**



REF.	Millimeter	
	Min.	Max.
A	6.40	6.80
B	5.13	5.53
C	6.80	7.25
D	2.90	3.30
E	2.19	2.39
G	0.45	0.85
H	2.20	2.40
J	0.41	0.61
K	0	0.15
L	1.40	1.85
M	5.90	6.30
R	0.60	1.20



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