ICmic™
IC MICROSYSTEMS

12-Bit 1.2v Low Power Single DAC With Serial Interface and Voltage Output

FEATURES

- **12-Bit 1.2v Single DAC in 8 Lead TSSOP Package**
- **Ultra-Low Power Consumption**
- **Guaranteed Monotonic**
- **Wide Voltage Output Swing Buffer**
- **Three-wire SPI/QSPI and Micro-wire Interface Compatible**
- **Schmitt-Triggered Inputs for Direct Interfacing to opto-couplers**

APPLICATION

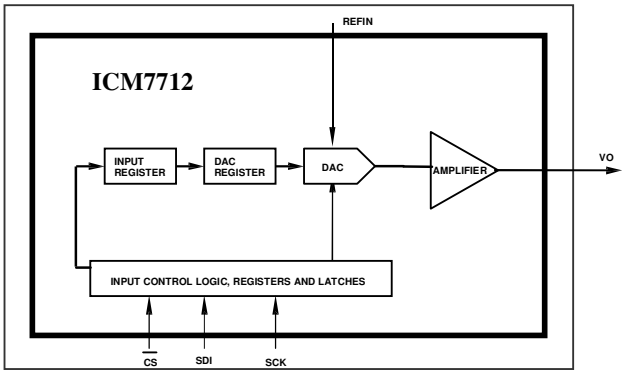
- Battery-Powered Applications
- Audio Applications
- Industrial Process Control
- Digital Gain and Offset Adjustment

OVERVIEW

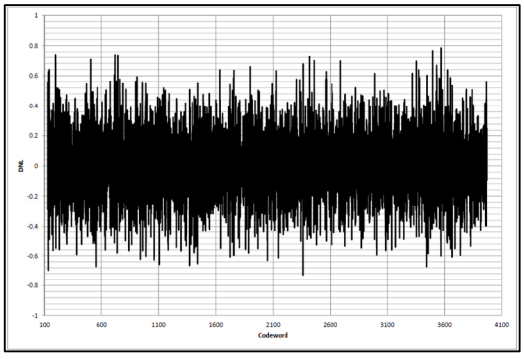
The ICM7712 is a 12-Bit Voltage Output, ultra Low Power, Single DAC, with guaranteed monotonic behavior. This DAC is available in 8- Lead TSSOP package.

The input interface is an easy to use three-wire SPI, QSPI and Micro-wire compatible interface. The DAC has Schmitt- Triggered inputs for Direct Interfacing to opto-couplers easily.

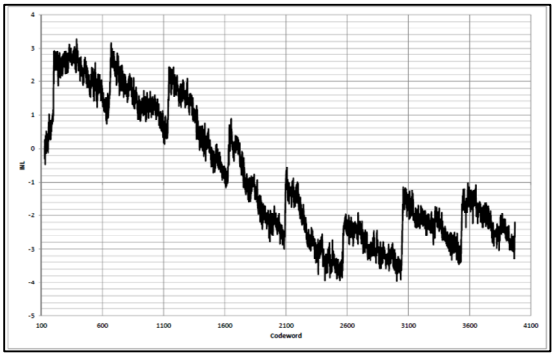
BLOCK DIAGRAM



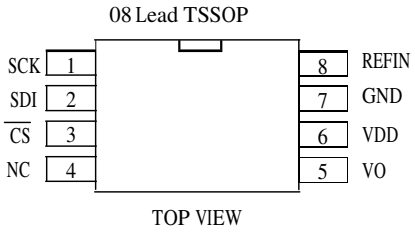
DNL PLOT



INL PLOT



PACKAGE



PIN DESCRIPTION (8 Lead TSSOP)

Pin	Name	I/O	Description
1	SCK	I	Serial Clock Input (CMOS)
2	SDI	I	Serial Data Input (CMOS)
3	$\overline{CS}$	I	Active Low Chip Select (CMOS)
4	NC	-	No Connection
5	VO	O	DAC Output Voltage
6	VDD	I	Supply Voltage
7	GND	I	Ground
8	REFIN	I	Reference Voltage Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	0.9 to 1.32	V
I_{IN}	Input Current	+/- 25.0	mA
V_{IN}	Digital Input Voltage (SCK, SDI, $\overline{CS}$)	-0.3 to 1.32	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 1.32	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOL}	Soldering Temperature	300	°C

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Operating Temperature Range	Package
ICM7712	-40 °C to 85 °C	08-Lead TSSOP

DC ELECTRICAL CHARACTERISTICS

(Specification: VDD=1.2V, VREFIN=1.15v, Temp=25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
N	Resolution			12		Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.4	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		1	±12	LSB
STATIC ACCURACY						
GE	Gain Error				±0.5	% of FS
OE	Offset Error				25	mV
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		0.9	1.2	1.32	V
I_{DD}	Supply Current	Full Scale at VDD=1.2		490	1000	µA
OUTPUT CHARACTERISTICS						
Vout	Output Voltage Range	(Note 3)	0		V_{DD}	V
V_{OSC}	Short Circuit Current			4	13	mA

AC ELECTRICAL CHARACTERISTICS

(Specification: VDD=1.2V, REFIN=1.15v,Temp=25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SR	Slew Rate			4		V/µ
Ts	Settling Time	(Note 5)		2		µs
Fs	Conversion Speed			200		ksps
Td	Analog output Delay	(Note 4)		150		ns

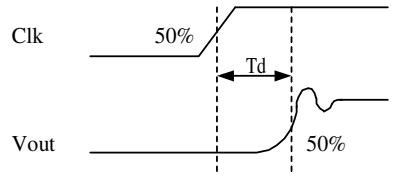
Note 1: Linearity is defined from code 127 to 3970 (ICM7712)
Note 2: Guaranteed by design; not tested in production
Note 3: See Applications Information
Note 4: Output delay measured from the 50% point of the rising edge of input data to the full scale transition
Note 5: Settling time measured from the 50% point of full scale transition to the output remaining within 1/2LSB.

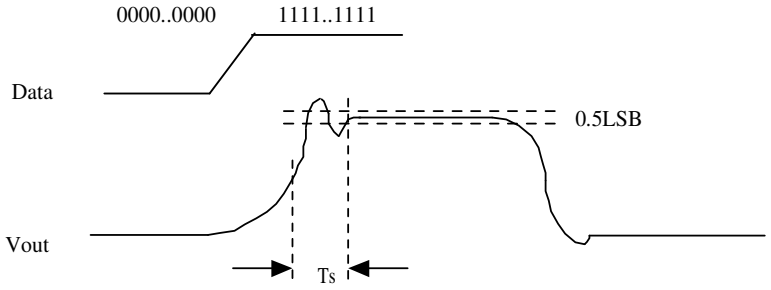
TIMING CHARACTERISTICS

(V_{DD} = 0.9V to 1.32v, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_1	SCK Cycle Time	(Note 2)	30			ns
t_2	Data Setup Time	(Note 2)	10			ns
t_3	Data Hold Time	(Note 2)	10			ns
t_4	SCK Falling edge to $\overline{CS}$ Rising Edge	(Note 2)	0			ns
t_5	$\overline{CS}$ Falling Edge to SCK Rising Edge	(Note 2)	10			ns
t_6	$\overline{CS}$ Pulse Width	(Note 2)	20			ns

TIMING DIAGRAM





SERIAL INTERFACE TIMING AND OPERATION DIAGRAM

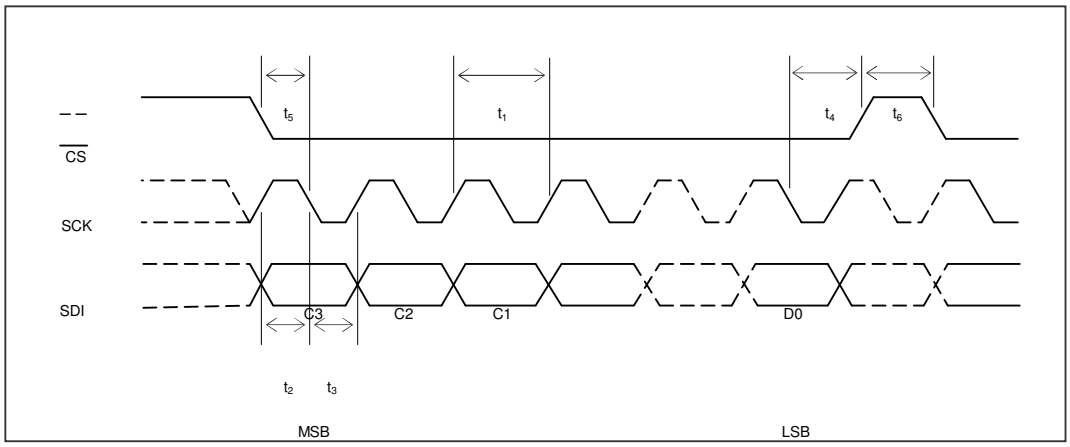


Figure 1. Serial Interface Timing Diagram

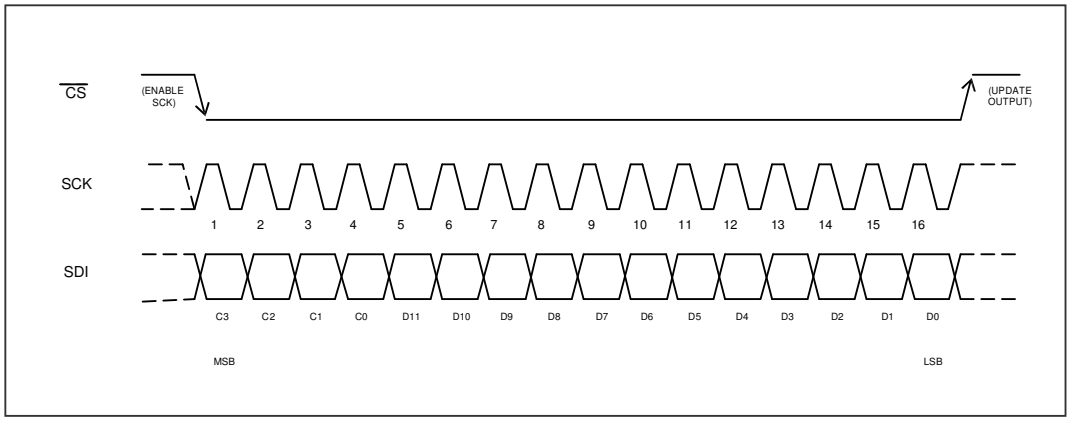


Figure 2. Serial Interface Operation Diagram

CONTENTS OF INPUT SHIFT REGISTER

DEVICE	CONTROL WORD				DATA WORD											
	MSB															LSB
ICM7712	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 3. Contents of Input Shift Register

FUNCTION

C3	C2	C1	C0	DATA	FUNCTION
0	0	0	0	(D11~D0)	Input loaded into DAC, VO updated

Table 1. Serial Interface Input Word

DETAILED DESCRIPTION

The ICM7712 is a 12-bit voltage output DAC. This device has a 16-bit input shift register and the DAC has a double buffered digital input. This DAC has a guaranteed monotonic behavior and the operating supply range is from 0.9v to 1.32v.

Reference Input

The reference input accepts positive DC and AC signals. The voltage at REFIN sets the full-scale output voltage of the DAC. To determine the output voltage for any code, use the following equation.

$$VOUT = VREF \times (D / (2^n))$$

Where D is the numeric value of DAC's decimal input code, VREF is the reference voltage and n is number of bits, i.e. 12 for ICM7712.

Output Buffer Amplifier

This amplifier has a wide output voltage swing. The actual swing of the output amplifier will be limited by offset error and gain error. See the Applications Information Section for a more detailed discussion.

The output amplifier can drive a load of 2.0 K Ω to VDD or GND in parallel with a 500 pF load capacitance.

The output amplifier has a full-scale typical settling time of 2 µs and it dissipates about 500 µA with a 1.2V supply voltage.

Serial Interface and Input Logic

This DAC uses a standard 3-wire connection compatible with SPI/QSP and Micro wire interfaces. Data is always loaded in 16-bit words which consist of 4 control bits (MSBs) followed by 12 bits (see Figure 3).

Serial Data Input

SDI (Serial Data Input) pin is the data input pin for the DAC. Data is clocked in on the falling edge of SCK which has a Schmitt trigger internally to allow for noise immunity on the SCK pin. This specially eases the use for opto-coupled interfaces.

The Chip Select pin which is the 3rd pin of 8 Lead TSSOP package is active low. This pin frames the input data for synchronous loading and must be low when data is being clocked into the part. There is an onboard counter on the clock input and after the 16th clock pulse the data is automatically transferred to a 16-bit input latch and the 4 bit control word (C3~C0) is then decoded and the appropriate command is performed depending on the control word (see Table 1). Chip Select pin must be pulled high (level-triggered) and back low for the next data word to be loaded in. This pin also disables the SCK pin internally when pulled high.

APPLICATIONS INFORMATION

Power Supply Bypassing and Layout Considerations

As in any precision circuit, careful consideration has to be given to layout of the supply and ground. The return path from the GND to the supply ground should be short with low impedance. Using a ground plane would be ideal. The supply should have some bypassing on it. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic with a low ESR can be used. Ideally these would be placed as close as possible to the device. Avoid crossing digital and analog signals, specially the reference, or running them close to each other.

Output Swing Limitations

The ideal rail-to-rail DAC would swing from GND to VDD. However, offset and gain error limit this ability. Figure 4 illustrates how a negative offset error will affect the output. The output will limit close to ground since this is single supply part, resulting in a dead-band area. As a larger input is loaded into the DAC the output will eventually rise above ground. This is why the linearity is specified for a starting code greater than zero.

Figure 5 illustrates how a gain error or positive offset error will affect the output when it is close to VDD. A positive gain error or positive offset will cause the output to be limited to the positive supply voltage resulting in a dead-band of codes close to full-scale.

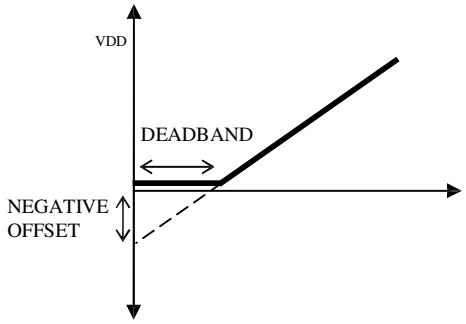


Figure 4. Effect of Negative Offset

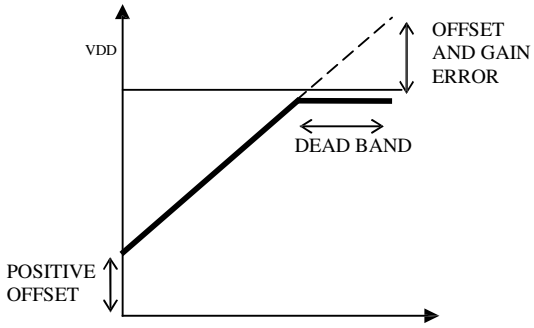
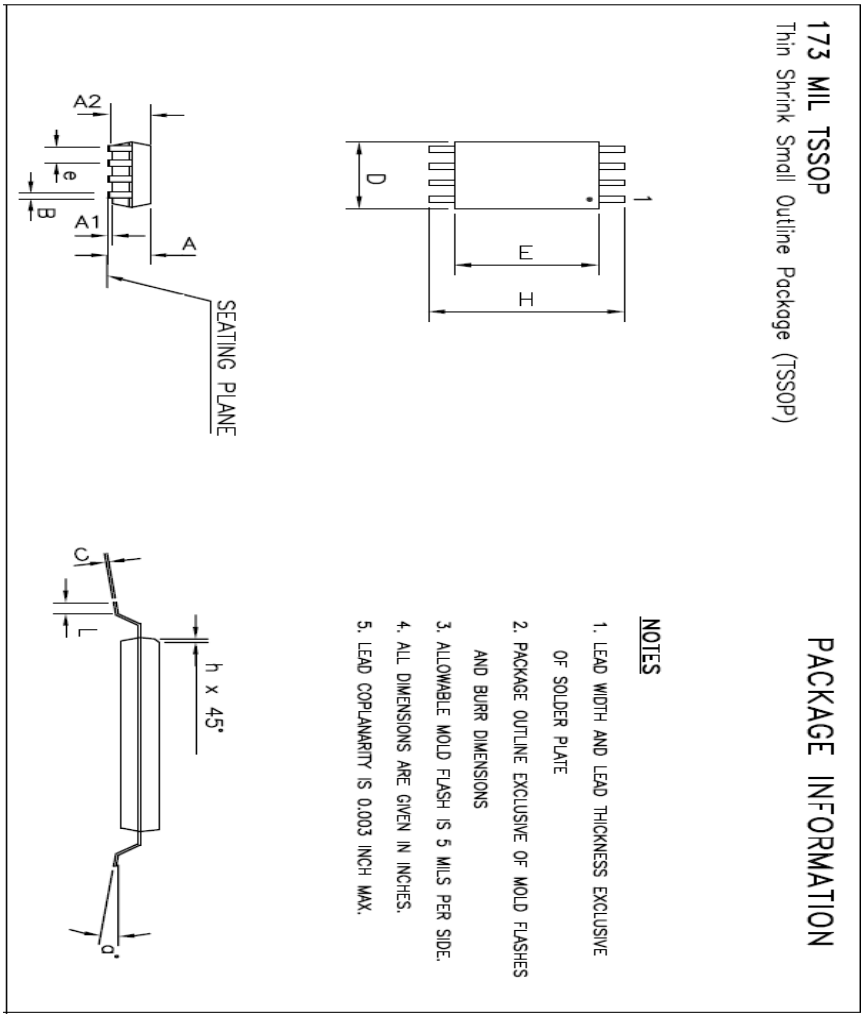


Figure 5. Effect of Gain Error and Positive Offset

PACKAGE INFORMATION

8 Lead TSSOP



PACKAGE INFORMATION