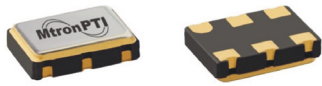


# M630x Series

5x7 mm, 1.8/2.5/3.3 V, LVPECL/LVDS/CML/CMOS, TCXO/TCVCXO



## Ordering Information

	<b>M6300</b>	<b>2</b>	<b>J</b>	<b>B</b>	<b>V</b>	<b>P</b>	<b>N</b>	<b>00.0000 MHz</b>	
<b>Product Series</b>									
<b>M6300</b> = 3.3 V									
<b>M6301</b> = 2.5 V									
<b>M6302</b> = 1.8 V									
<b>Temperature Range</b>									
<b>1:</b> 0 °C to +70 °C				<b>3:</b> -55 °C to +105 °C					
<b>6:</b> -20 °C to +70 °C				<b>4:</b> -55 °C to +125 °C					
<b>2:</b> -40 °C to +85 °C									
<b>Stability</b>									
<b>G:</b> ±0.5 ppm			<b>J:</b> ±1.0 ppm			<b>K:</b> ±2.0 ppm			
<b>H:</b> ±2.5 ppm			<b>L:</b> ±4.6 ppm			<b>E:</b> ±10 ppm			
<b>Enable/Disable Function</b>									
<b>B:</b> Enable High (Pad 1)				<b>G:</b> Enable High (Pad 2)					
<b>S:</b> Enable Low (Pad 1)				<b>M:</b> Enable Low (Pad 2)					
<b>U:</b> No Enable/Disable Function									
<b>Output Type</b>									
<b>F:</b> No Voltage Control (TCXO)									
<b>V:</b> Voltage Control (TCVCXO)									
<b>Output Waveform</b>									
<b>P:</b> LVPECL			<b>L:</b> LVDS			<b>M:</b> CML			
						<b>C:</b> CMOS			
<b>Package/Lead Configurations</b>									
<b>N:</b> Leadless Ceramic (9 Pad)				<b>C:</b> Leadless Ceramic (6 Pad)					
<b>Frequency (customer specified)</b>									

M6300Sxxx, M6301Sxxx & M6302Sxxx - Custom datasheets.

## Features:

- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 50 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

## Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

## PIN 1 ENABLE

- Pad 1: Enable/Disable
- Pad 2: N/C
- Pad 3: GND
- Pad 4: Output Q (LVPECL, LVDS, CML, CMOS)
- Pad 5: Output  $\bar{Q}$  (LVPECL, LVDS, CML)
- Pad 6:  $V_{CC}$

## PIN 2 ENABLE

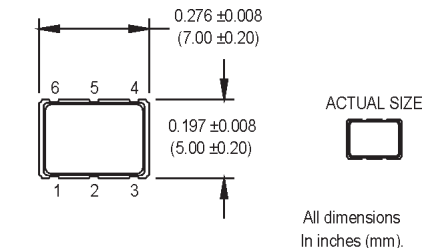
- Pad 1: N/C, V Control
- Pad 2: Enable/Disable
- Pad 3: GND
- Pad 4: Output Q (LVPECL, LVDS, CML, CMOS)
- Pad 5: Output  $\bar{Q}$  (LVPECL, LVDS, CML)
- Pad 6:  $V_{CC}$

## Temperature vs. Stability

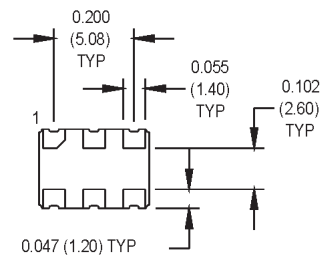
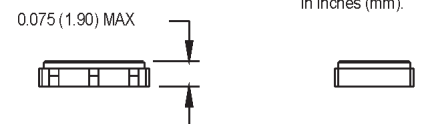
	±0.5 ppm	±1.0 ppm	±2.0 ppm	±2.5 ppm	±4.6 ppm
0 °C to +70 °C	A	A	A	A	A
-20 °C to +70 °C	N	A	A	A	A
-40 °C to +85 °C	N	A	A	A	A
-55 °C to +105 °C	N	N	N	N	A
-55 °C to +125 °C	N	N	N	N	A

A = Available

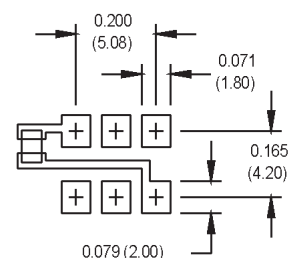
N = Contact Factory



All dimensions in inches (mm).



## SUGGESTED SOLDER PAD LAYOUT



# M630x Series

5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/CMOS, TCXO/TCVCXO



		Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions/Notes
Electrical Specifications	Frequency Range	$F_R$	50			1400	MHz	LVPECL, LVDS, CML (See Note 1)
			50			135	MHz	CMOS
	Initial Accuracy	$F_I$	-1			+1	ppm	@ +25 °C
	Frequency Stability	$\Delta F_T/F$	See Ordering Information				ppm	(Fmax - Fmin)/2 (See Note 2)
	Frequency Vs. Aging	$\Delta F_{TIME}/F$	-3			+3	ppm	First year
			-1			+1	ppm	Thereafter (per year)
	Frequency Vs. Supply Voltage	$\Delta F_{VDD}/F$			$\pm 0.40$		ppm	5% voltage variation
	Frequency Vs. Reflow				$\pm 0.75$		ppm	2 reflows max.
	Frequency Vs. Load	$\Delta F_{LOAD}/F$			$\pm 0.20$		ppm	5% supply voltage variation
	Operating Temperature	$T_A$	See Ordering Information				°C	
	Storage Temperature	$T_{STG}$	-55			+125	°C	
	Operating Voltage	$V_{CC}/V_S/V_{DD}$	3.135	3.3	3.465		V	M6300
			2.375	2.5	2.625		V	M6301
			1.71	1.8	1.89		V	M6302
	Operating Current	$I_{CC}$			125		mA	LVPECL
					100		mA	LVDS
					110		mA	CML
					90		mA	CMOS
	Rise/Fall Time	$t_R/t_F$			0.35		ns	LVPECL, LVDS, CML
					6		ns	CMOS
	Logic "1" Level	$V_{OH}$	$V_{CC} - 1.02$				V	LVPECL
			90				% $V_{DD}$	CMOS
	Logic "0" Level	$V_{OL}$			$V_{CC} - 1.63$		V	LVPECL
					10		% $V_{DD}$	CMOS
	Common Mode Output Voltage	$V_{CM}$		1.2			V	LVDS
	Symmetry (Duty Cycle)	$t_{DC}$	45		55		%	@ 50% $V_{DD}$ (CMOS)
			45		55		%	@ 50% of waveform (LVPECL)
			45		55		%	@ 1.25 V (LVDS)
Output Voltage Level		0.7	0.95	1.2		$V_{pk-pk}$	CML	
Tuning Range		$\pm 5$				ppm	VCTCXO only (See Note 3)	
Voltage Control Range	$V_C$	0.18	0.90	1.62		V	@ 1.8 V supply (VCTCXO only - Pad 2)	
		0.25	1.25	2.25		V	@ 2.5 V supply (VCTCXO only - Pad 2)	
		0.30	1.65	3.00		V	@ 3.3 V supply (VCTCXO only - Pad 2)	
Output Skew			20			ps	LVPECL	
			15			ps	CML	
			20			ps	LVDS	
Output Load		50 $\Omega$ to ( $V_{CC} - 2$ ) $V_{DC}$ 100 $\Omega$ Differential 15 pF					LVPECL (See Note 4)	
							LVDS, CML (See Note 4)	
							CMOS (See Note 4)	
Enable/Disable Function (Option B or G)		80		0.5		%	Output Enabled	
						V	Output Disabled	
Enable/Disable Function (Option S or M)		80		0.5		%	Output Enabled	
						V	Output Disabled	
Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz		Offset from carrier	
@ 622.080 MHz (LVPECL)	-60	-90	-120	-127	-133		dBc/Hz	
@ 100.000 MHz (HCMOS)	-70	-103	-123	-131	-136		dBc/Hz	
@ 50.000 MHz (HCMOS)	-77	-109	-129	-137	-141		dBc/Hz	
Environmental	Shock	Per MIL-STD-202, Method 213, Condition C						
	Vibration	Per MIL-STD-202, Methods 201 & 204						
	Solderability	Per EIAJ-STD-002						
	Hermeticity	$1 \times 10^{-8}$ atm cc/sec of helium (Crystal only)						
	Thermal Shock	Per MIL-STD-883, Method 1011, Condition A						
	Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B						

Note 1: Contact factory for frequencies over 945 MHz.

Note 2: Contact factory for less than  $\pm 1$  ppm frequency stability.

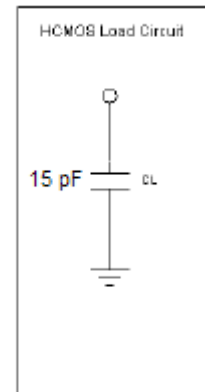
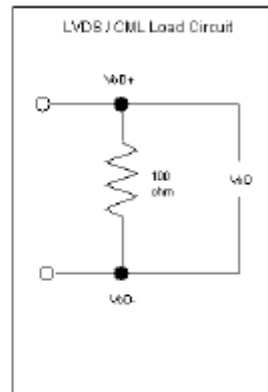
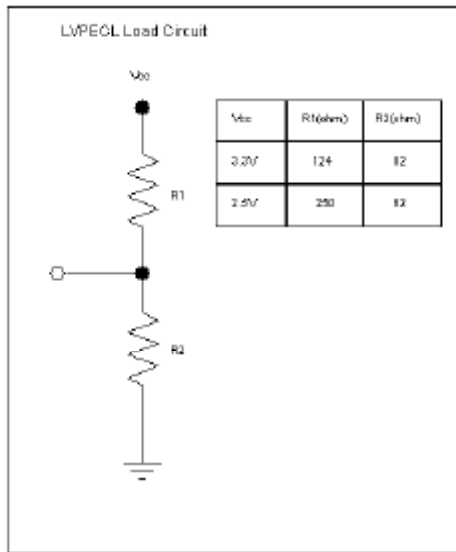
Note 3: Contact factory for other tuning range options.

Note 4: Refer to the load circuit diagram in this data sheet.

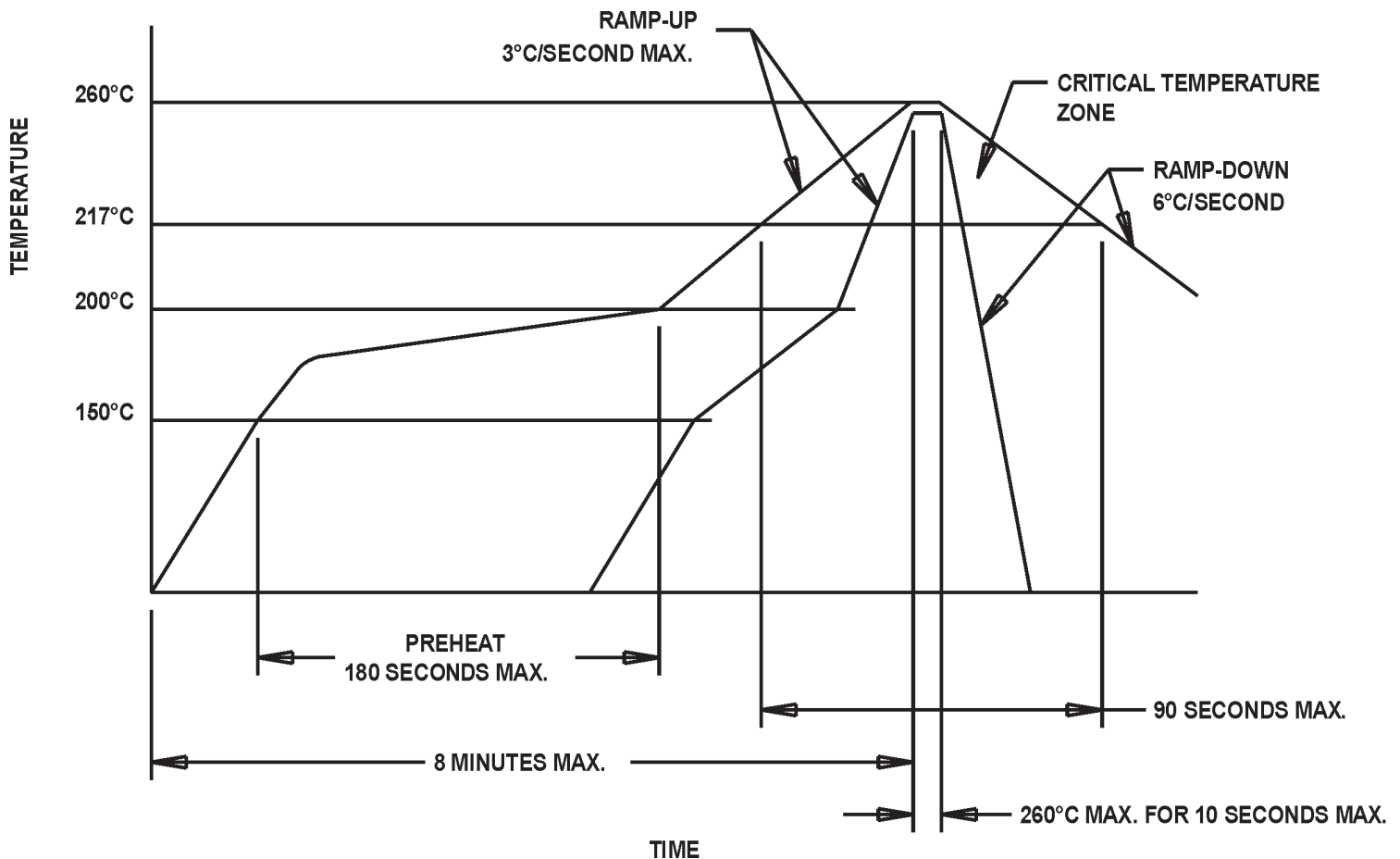
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# Load Circuit Diagrams



## Lead Free Solder Profile



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