A Business Partner of Renesas Electronics Corporation.
California Eastern Laboratories

PS9551AL4

Data Sheet

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Rev.1.00
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Optically Isolated Delta-Sigma Modulator

DESCRIPTION

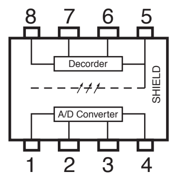
The PS9551AL4 is an optically isolated Delta – Sigma Modulator that includes high-Accuracy A/D convertor and converts an analog voltage input into one-bit data stream. PS9551AL4 provides Effective Number of Bit (ENOB) is 12 bits (typ) with a Sinc^3 digital filter.

The PS9551AL4 is designed specifically for high common mode transient immunity (CMR) and high linearity (nonlinearity). The PS9551AL4 is suitable for current sensing and voltage sensing in motor drives.

FEATURES

- Internal Reference Voltage Tolerance (G_E = ±1% MAX.)
- Effective Number of Bit (ENOB = 12 bits TYP.)
- Operating Ambient Temperature (T_A = –40 to 105°C)
- Non-linearity (INL = 0.14% MAX.)
- Input Offset Voltage (V_{OS} = 3 mV MAX.)
- Input Offset Voltage Drift vs. Temperature ($|dV_{os}/dT_A|$ = 2 μV/°C TYP.)
- Output Clock Frequency (f_{CLK} = 10 MHz TYP.)
- High common mode transient immunity (CMR= 15 kV/μs MIN.)
- Package: 8-pin DIP lead bending type (Gull-wing) for long creepage distance for surface mount (L4)
- Embossed tape product: PS9551AL4-E3: 1 000 pcs/reel
- Pb-Free product
- <R> Safety standards
  - UL approved: No. E72422
  - CSA approved: No. CA 101391 (CA5A, CAN/CSA-C22.2 60065, 60950)
  - SEMKO approved (EN 60065, EN60950)
  - DIN EN 60747-5-5 (VDE 0884-5) approved (Option)

PIN CONNECTION
(Top View)



1. V_{DD1}
2. V_{IN+}
3. V_{IN-}
4. GND1
5. GND2
6. MDAT
7. MCLK
8. V_{DD2}

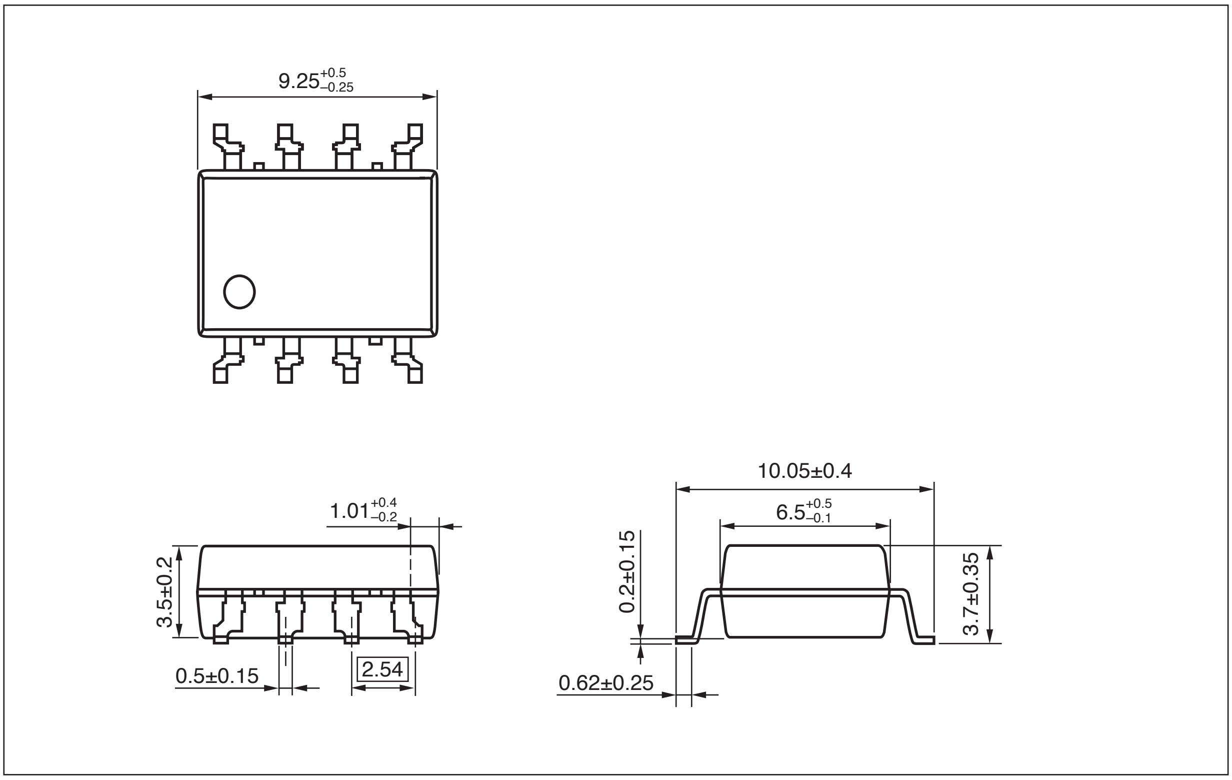
APPLICATIONS

- AC Servo, inverter
- Solar inverter
- Measurement equipment

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

PACKAGE DIMENSIONS (UNIT: mm)

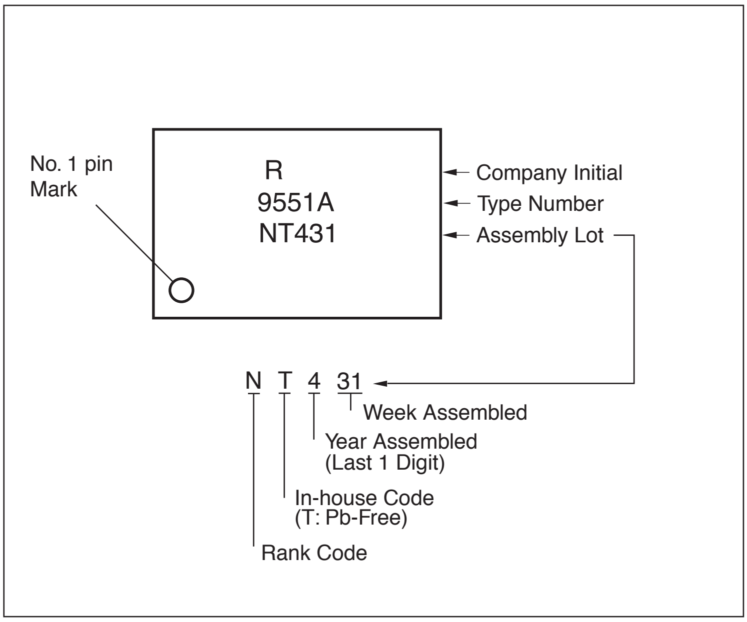
Lead Bending Type (Gull-wing) For Long Creepage Distance For Surface Mount (L4)



PHOTOCOUPLER CONSTRUCTION

Parameter	MIN.
Air Distance	8 mm
Outer Creepage Distance	8 mm
Isolation Distance	0.4 mm

<R> MARKING EXAMPLE



<R> ORDERING INFORMATION

Part Number	Order Number	Solder Plating Specification	Packing Style	Safety Standard Approval	Application Part Number*1
PS9551AL4	PS9551AL4-AX	Pb-Free (Ni/Pd/Au)	Magazine case 50 pcs	Standard products (UL, CSA, SEMKO approved)	PS9551AL4
PS9551AL4-E3	PS9551AL4-E3-AX		Embossed Tape 1 000 pcs/reel		
PS9551AL4-V	PS9551AL4-V-AX		Magazine case 50 pcs	UL,CSA,SEMKO, DIN EN 60747-5-5 (VDE 0884-5)	
PS9551AL4-V-E3	PS9551AL4-V-E3-AX		Embossed Tape 1 000 pcs/reel		

***1** For the application of the Safety Standard, following part number should be used.

<R> ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Operating Ambient Temperature	T_A	–40 to +105	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Supply Voltage	V_{DD1}, V_{DD2}	0 to 5.5	V
Input Voltage	V_{IN+}, V_{IN-}	–2 to V_{DD1} +0.5	V
2 Seconds Transient Input Voltage	V_{IN+}, V_{IN-}	–6 to V_{DD1} +0.5	V
Output Voltage	V_{OUT+}, V_{OUT-}	–0.5 to V_{DD2} +0.5	V
Isolation Voltage[*1]	BV	5 000	Vr.m.s.

***1** AC voltage for 1 minute at T_A = 25°C, RH = 60% between input and output.
Pins 1-4 shorted together, 5-8 shorted together.

<R> RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Operating Ambient Temperature	T_A	–40		105	°C
Supply Voltage	V_{DD1}, V_{DD2}	4.5	5	5.5	V
Input Voltage (Accurate and Linear)[*1]	V_{IN+}, V_{IN-}	–200		200	mV

***1** Using V_{IN-} = 0 V (to be connected to GND1) is recommended. Avoid using V_{IN-} of 2.5 V or more, because the internal test mode is activated when the voltage V_{IN-} reaches more than 2.5 V.

<R> ELECTRICAL CHARACTERISTICS (TYP.: T_A = 25°C, V_{IN+} = V_{IN-} = 0 V, V_{DD1} = V_{DD2} = 5 V, MIN., MAX.: refer to RECOMMENDED OPERATING CONDITIONS, unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Supply Current	I_{DD1}	V_{IN+} = 350 mV		12	15	mA
Output Supply Current	I_{DD2}	V_{IN+} = –350 mV		6	15	mA
Input Bias Current	I_{IN}		–5	–0.6	5	μA
Low Level Saturated Output Voltage	V_{OL}	I_{OUT} = 1.6 mA		0.1	0.6	V
High Level Saturated Output Voltage	V_{OH}	I_{OUT} = –100 μA	3.9	4.9		V
Output Short-circuit Current	$\|I_{OSC}\|$	V_{OUT} = V_{DD2} or V_{OUT} = GND2		17	40	mA
Equivalent Input Resistance	R_{IN}			450		kΩ
Output Clock Frequency	f_{CLK}		8.2	10	13.2	MHz
Isolation Resistance	R_{I-O}	V_{I-O} = 1 kV_{DC}, T_A = 25°C	10^{11}			Ω
Isolation Capacitance	C_{I-O}	f = 1 MHz		0.7		pF
Data Hold Time [*1]	t_{HDDAT}		4	10	16	ns
Common Mode Transient Immunity [*2]	CMR	V_{CM} = 1 kV, T_A = 25°C	15			kV/μs

***1** The data hold time (t_{HDDAT}) is that the data (MDAT) will stay stable following the rising edge of the clock (MCLK). t_{HDDAT} is shown in the below timing chart.

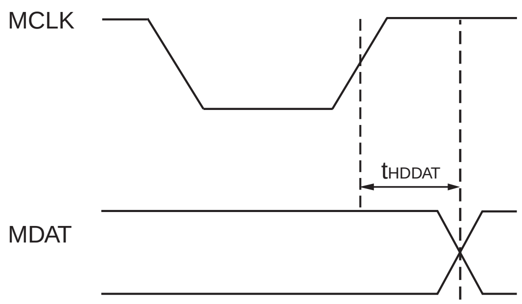


Fig. Timing Chart

***2** Common Mode Transient Immunity (CMR) is specified by the rate of rise / fall of a pulse applied between GND1 on the input side and GND2 on the output side (pins 4 and 5) by using the circuit shown in **Fig. 6 CMR Test Circuit**. CMR is defined at the point that clock signals are corrupted.

<R> ELECTRICAL CHARACTERISTICS (Tested with Sinc^3 filter, 256 decimation ratio.) (TYP.: T_A = 25°C, V_{IN+} = V_{IN-} = 0 V, V_{DD1} = V_{DD2} = 5 V, MIN., MAX.: refer to RECOMMENDED OPERATING CONDITIONS, unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Integral Non-linearity *3	INL	–200 mV ≤ V_{IN+} ≤ 200 mV		3	30	LSB
				0.01	0.14	%
Differential Non-linearity *4	DNL	–200 mV ≤ V_{IN+} ≤ 200 mV			1	LSB
Input Offset Voltage *5	V_{OS}		–3	0	3	mV
Input Offset Voltage Drift vs. Temperature	$\lvert dV_{OS}/dT_A \rvert$			2	10	μV/°C
Input Offset Voltage Drift vs. Supply Voltage	$\lvert dV_{OS}/dV_{DD1} \rvert$			0.1		mV/V
Internal Reference Voltage *6	V_{REF}			320		mV
Absolute Internal Reference Voltage Tolerance	G_E	T_A = 25°C	–1		1	%
		T_A = –40 to 105°C	–4		4	%
Internal Reference Voltage Drift vs. Temperature	$\lvert dV_{REF}/dT_A \rvert$			60		ppm/°C
Internal Reference Voltage Drift vs. Supply Voltage	$\lvert dV_{REF}/dV_{DD1} \rvert$			0.2		mV/V
Input DC Common-Mode Rejection Ratio *7	$CMRR_{IN}$			70		dB

***3** Integral non-linearity (INL) is the maximum deviation between the ideal conversion line (best-fit line) and measured points. The best-fit line is obtained by using the least-squares method from the differential input voltage (V_{IN+} – V_{IN-}: V_{IN+} = –200 mV to 200 mV, V_{IN-} = 0 V) and the output data that is measured under the circuit shown in **Fig. 7 INL Test Circuit**. INL is defined as the ratio (%) obtained by dividing [Half of the peak to peak value of the deviation] by [full-scale differential input voltage 400 mV].
For example, if the differential input voltage is V_{IN+} = –200 mV to 200 mV, and the peak to peak value of the deviation is 1.12 mV, Integral non-linearity is obtained as follows:
INL = 1.12 mV/(2 × 400 mV) = 0.14%
And Input Full-Scale 640 mV (–320 to 320 mV) of PS9551A is assigned 15 bits (2^{15} = 32768).
Therefore, Least Significant Bit (LSB) is 19.5 μV.
By LSB indication, above-mentioned INL is 1.12 mV/(2 × 0.0195 mV) = 29 LSBs.

***4** Differential non-linearity (DNL) is the difference between a measured code width and ideal 1 LSB in the ADC transfer curve.

***5** Input offset voltage (V_{OS}) is a measured value after Sinc^3 digital filter when the input voltage is 0 V (V_{IN+} = V_{IN-} = 0 V).

***6** Absolute Internal Reference Voltage Tolerance (G_E) is the gap rate between the ideal conversion line slope (Slope = 1) and a best-fit line slope that provided by the least-squares method from a real conversion level output for the differential input voltage (V_{IN+} – V_{IN-}: V_{IN+} = –200 mV to 200 mV, V_{IN-} = 0 V).

***7** Input DC Common-Mode Rejection Ratio ($CMRR_{IN}$) is the ratio of the differential signal (V_{IN+} = –200 mV to 200 mV, V_{IN-} = 0 V) to the common-mode signal (V_{IN+} = V_{IN-} = –200 mV to 200 mV: Both input pins are connected). $CMRR_{IN}$ is defined as follows,

$CMRR_{IN}$ (dB) = 20log (Vdo/Vco)
Vdo : Output voltage when the differential signal voltage input
Vco : Output voltage when the common-mode signal voltage input

<R> ELECTRICAL CHARACTERISTICS (Tested with Sinc^3 filter, 256 decimation ratio.) (TYP.: T_A = 25°C, V_{IN+} = V_{IN-} = 0 V, V_{DD1} = V_{DD2} = 5 V, MIN., MAX.: refer to RECOMMENDED OPERATING CONDITIONS, unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Signal to Noise Ratio *8	SNR	V_{IN+} = 35 Hz, 400 mVpk-pk (141 mVr.m.s.) sine wave	62	74		dB
Total Harmonic Distortion *9	THD			–80		dB
Signal to Noise and Distortion Ratio *10	SNDR			72		dB
Effective Number of Bit *11	ENOB		10	12		bits

***8** Signal to Noise Ratio (SNR) is the ratio of the AC signal power to the noise power that excludes harmonic signals and DC. SNR is defined as follows,

SNR (dB) = 10log(P_S/P_N)
P_S: Signal power (fundamental)
P_N: Noise power (excluding harmonic signals and DC)

***9** Total Harmonic Distortion (THD) is the ratio of the AC signal power (fundamental) to the sum of harmonic signals that are occurred by the non-linearity. THD is defined as follows,

THD (dB) = 10log((P_{H2} + P_{H3} + ... + P_{H5})/P_S)
P_S: Signal power (fundamental)
P_{H2}, P_{H3} ... P_{H5}: Second through fifth harmonics power

***10** Signal to Noise and Distortion ratio (SNDR) is the ratio of the AC signal power (fundamental) to the noise power plus distortion power. SNDR is defined as follows,

SNDR (dB) = 10log(P_S/(P_N + P_{H2} + P_{H3} + ... + P_{H5}))
P_S: Signal power (fundamental)
P_N: Noise power (excluding harmonic signals and DC)
P_{H2}, P_{H3} ... P_{H5}: Second through fifth harmonics power

***11** Effective Number of Bit (ENOB) is the effective resolution of ADC that is considered the noise.
ENOB is defined as follows,

ENOB (bits) = (SNR–1.76)/6.02

<R> TEST CIRCUIT

Fig.1 IDD1 Test Circuit

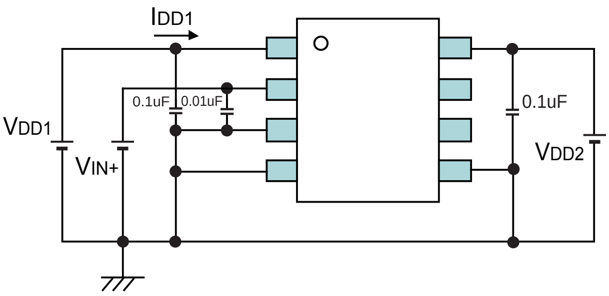


Fig.2 IDD2 Test Circuit

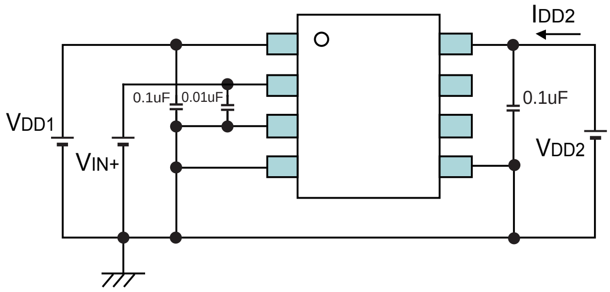


Fig.3 IIN Test Circuit

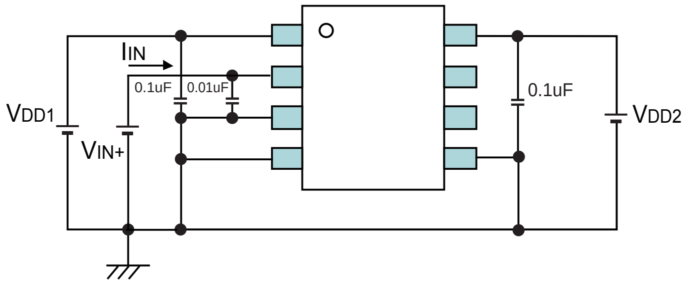
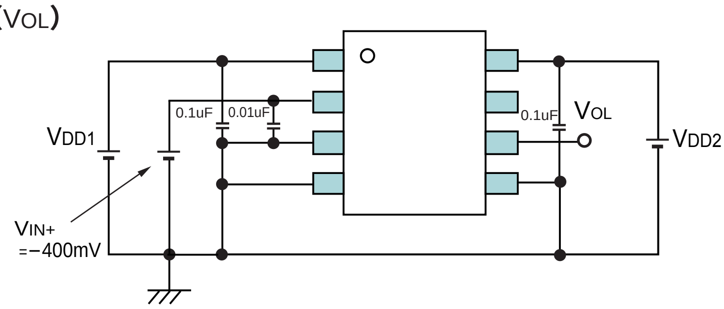


Fig.4 Vout Test Circuit

(VOL)



(VOH)

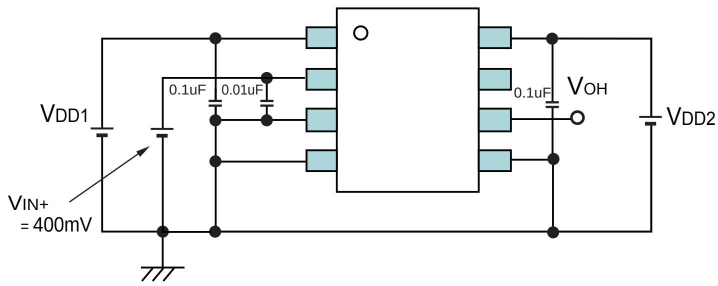


Fig.5 IOSC Test Circuit

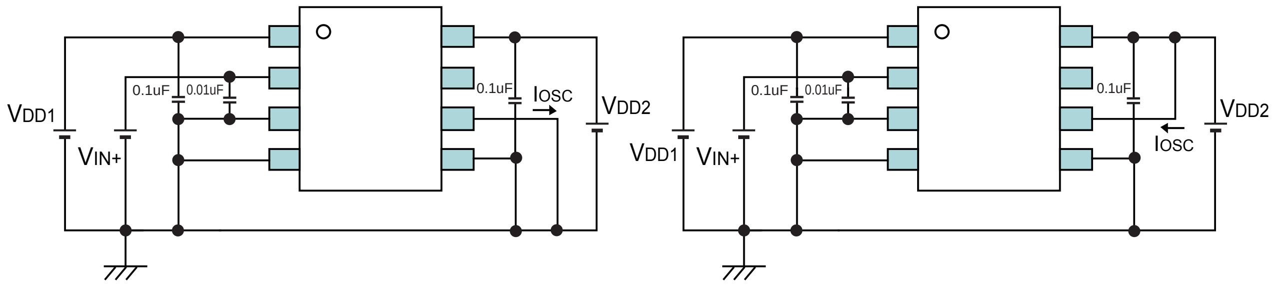


Fig.6 CMR Test Circuit

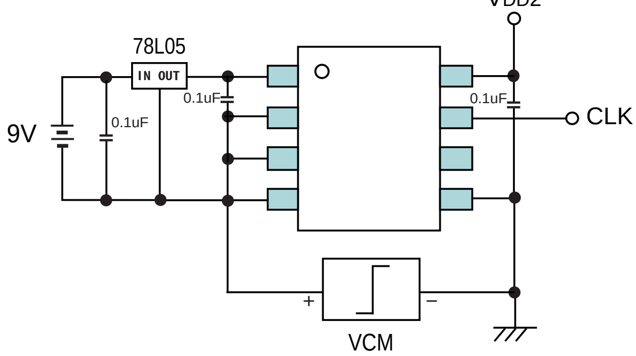
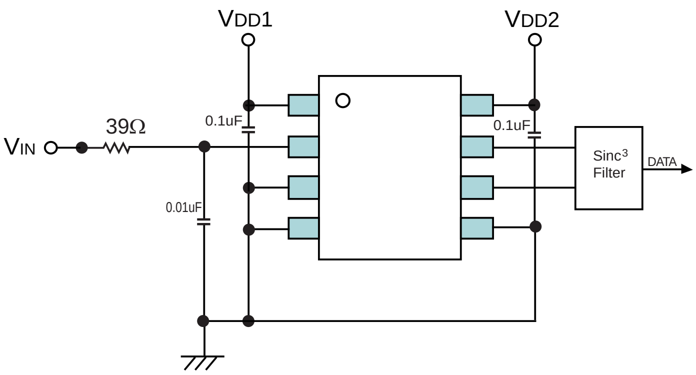
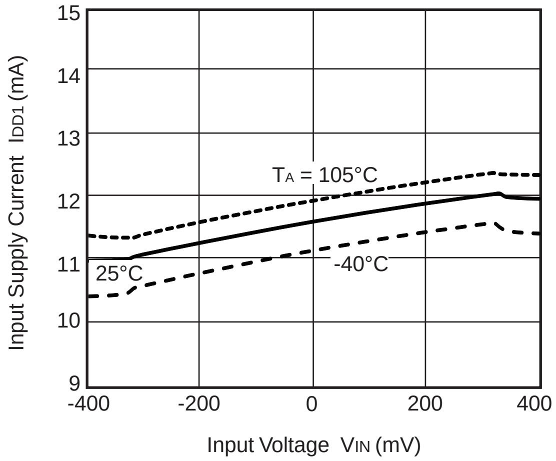


Fig.7 Vos, INL, DNL, GE, SNR, THD, SNDR, ENOB Test Circuit

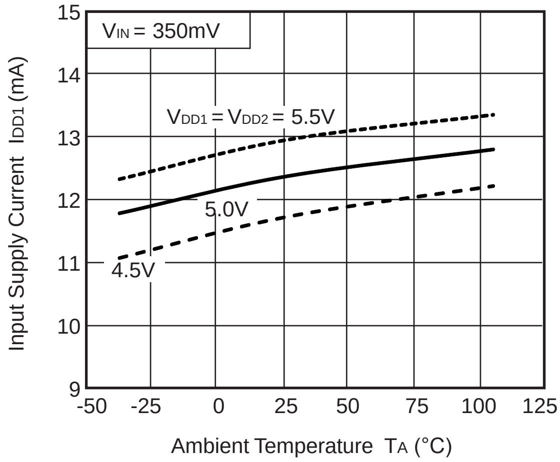


<R> TYPICAL CHARACTERISTICS (T_A = 25°C, V_{IN+} = V_{IN-} = 0 V, V_{DD1} = V_{DD2} = 5 V, tested with Sinc^3 filter, 256 decimation ratio, unless otherwise specified)

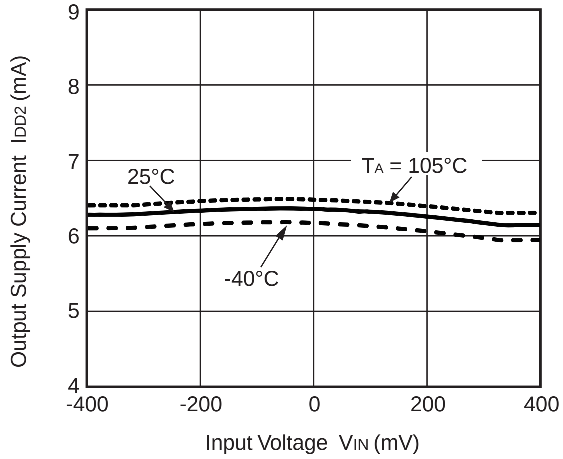
INPUT SUPPLY CURRENT vs.
INPUT VOLTAGE



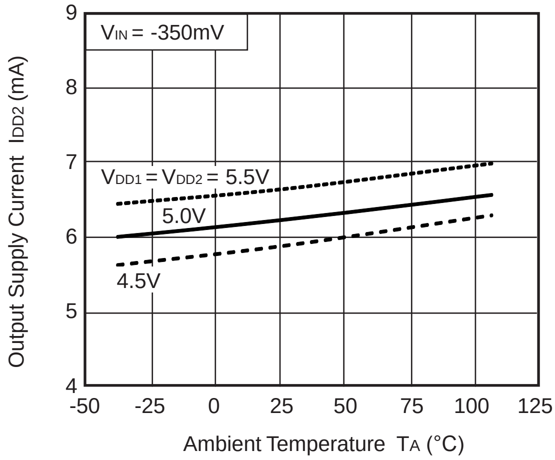
INPUT SUPPLY CURRENT vs.
AMBIENT TEMPERATURE



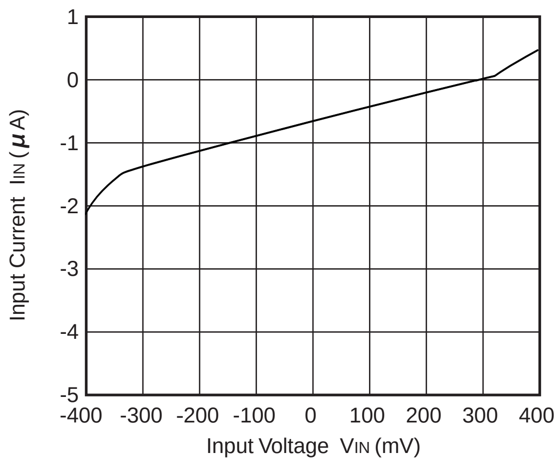
OUTPUT SUPPLY CURRENT vs.
INPUT VOLTAGE



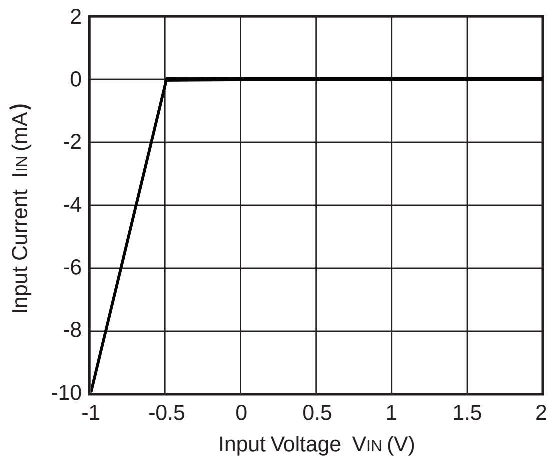
OUTPUT SUPPLY CURRENT vs.
AMBIENT TEMPERATURE



INPUT CURRENT vs. INPUT VOLTAGE

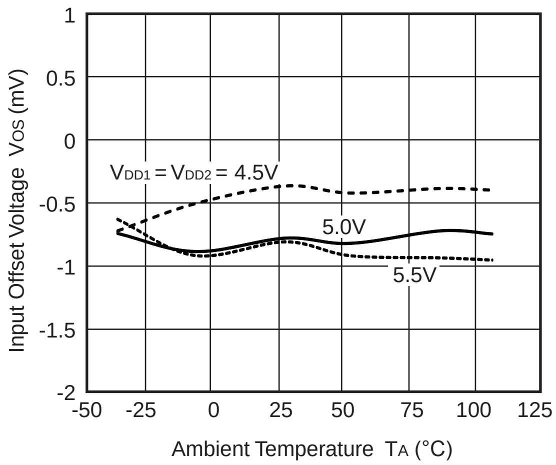


INPUT CURRENT vs. INPUT VOLTAGE

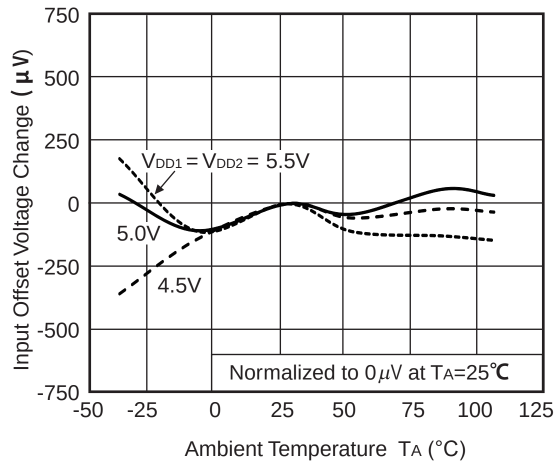


Remark The graphs indicate nominal characteristics.

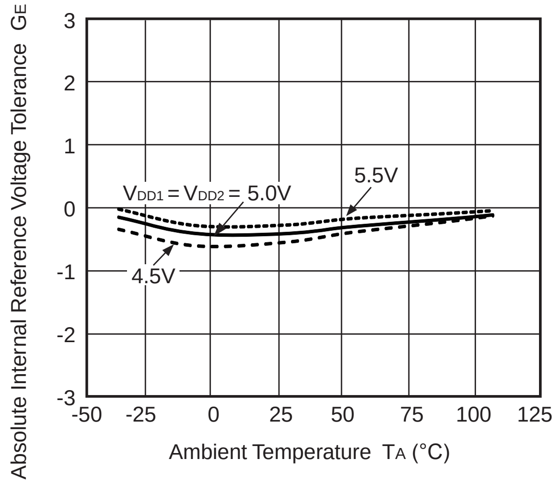
INPUT OFFSET VOLTAGE vs.
AMBIENT TEMPERATURE



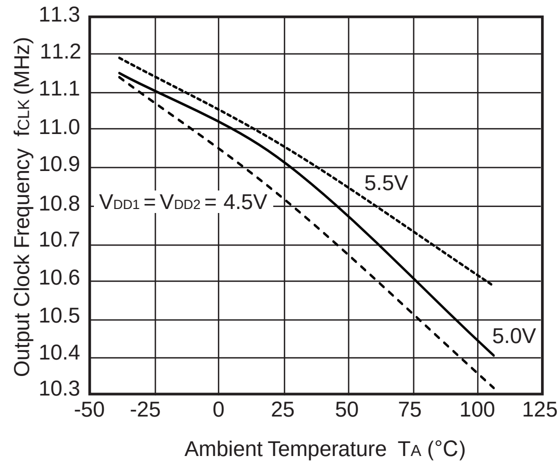
INPUT OFFSET VOLTAGE CHANGE
vs. AMBIENT TEMPERATURE



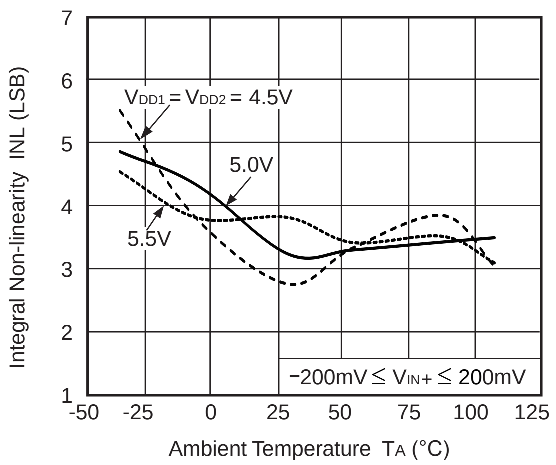
ABSOLUTE INTERNAL REFERENCE VOLTAGE
TOLETANCE vs. AMBIENT TEMPERATURE



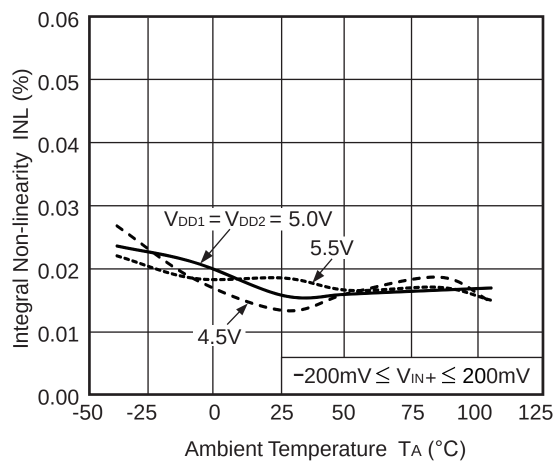
OUTPUT CLOCK FREQUENCY vs.
AMBIENT TEMPERATURE



INTEGRAL NON-LINEARITY(LSB)
vs. AMBIENT TEMPERATURE

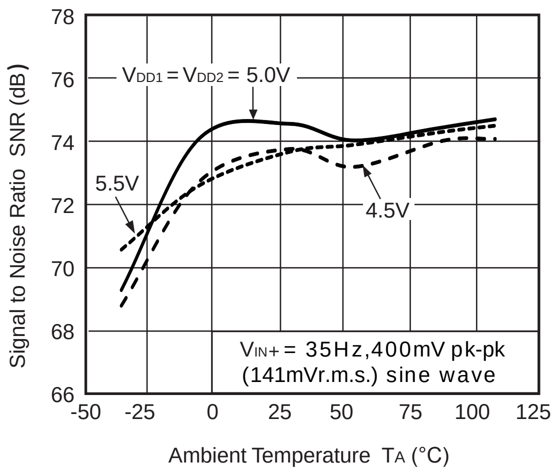


INTEGRAL NON-LINEARITY(%) vs.
AMBIENT TEMPERATURE

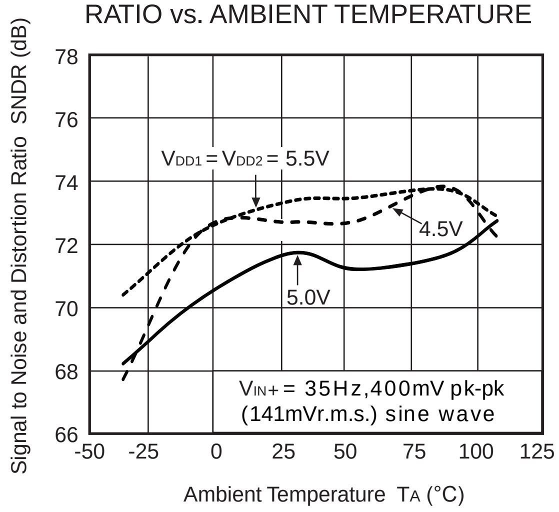


Remark The graphs indicate nominal characteristics.

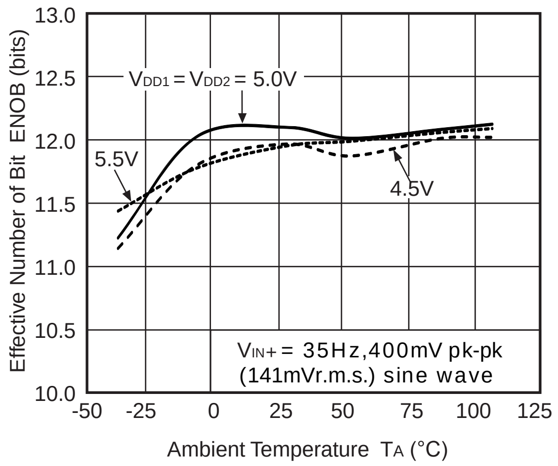
SIGNAL TO NOISE RATIO vs.
AMBIENT TEMPERATURE



SIGNAL TO NOISE AND DISTORTION
RATIO vs. AMBIENT TEMPERATURE



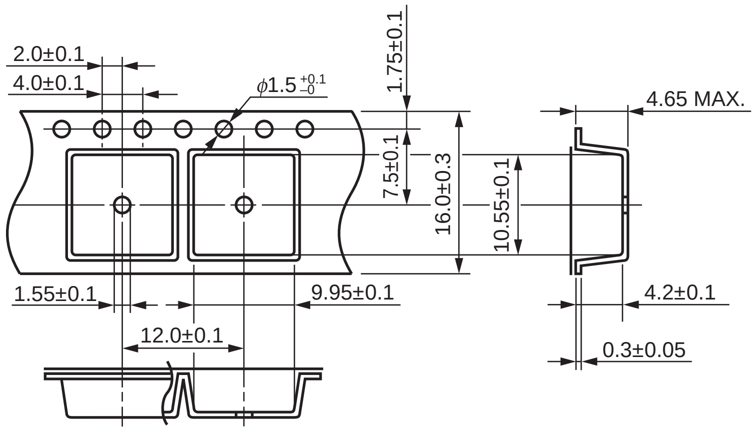
EFFECTIVE NUMBER OF BIT vs.
AMBIENT TEMPERATURE



Remark The graphs indicate nominal characteristics.

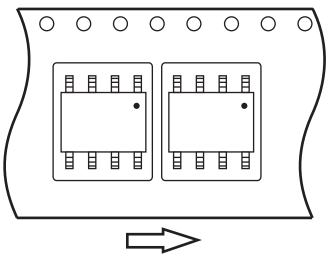
TAPING SPECIFICATIONS (UNIT: mm)

Outline and Dimensions (Tape)

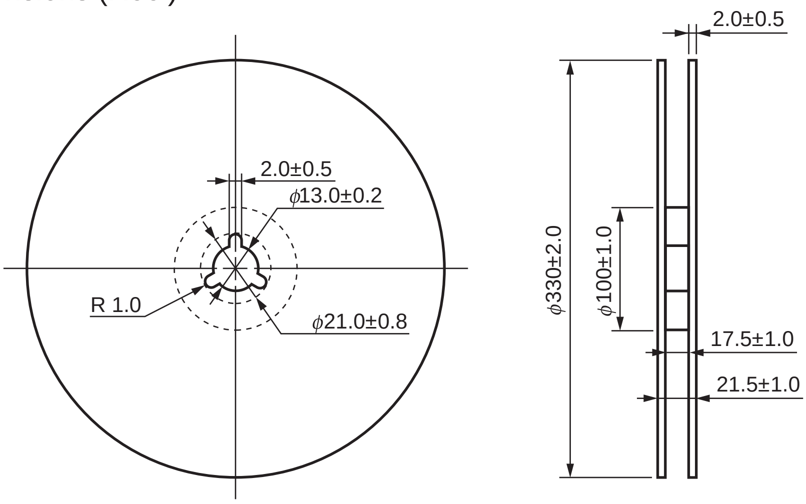


Tape Direction

PS9551AL4-E3

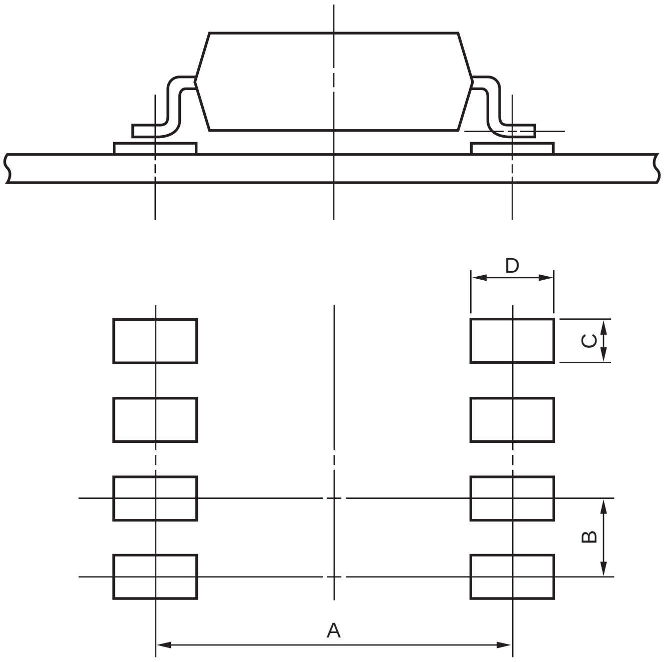


Outline and Dimensions (Reel)



Packing: 1 000 pcs/reel

<R> RECOMMENDED MOUNT PAD DIMENSIONS (UNIT: mm)



Part Number	Lead Bending	A	B	C	D
PS9551AL4	lead bending type (Gull-wing) for surface mount	9.0	2.54	1.7	2.0

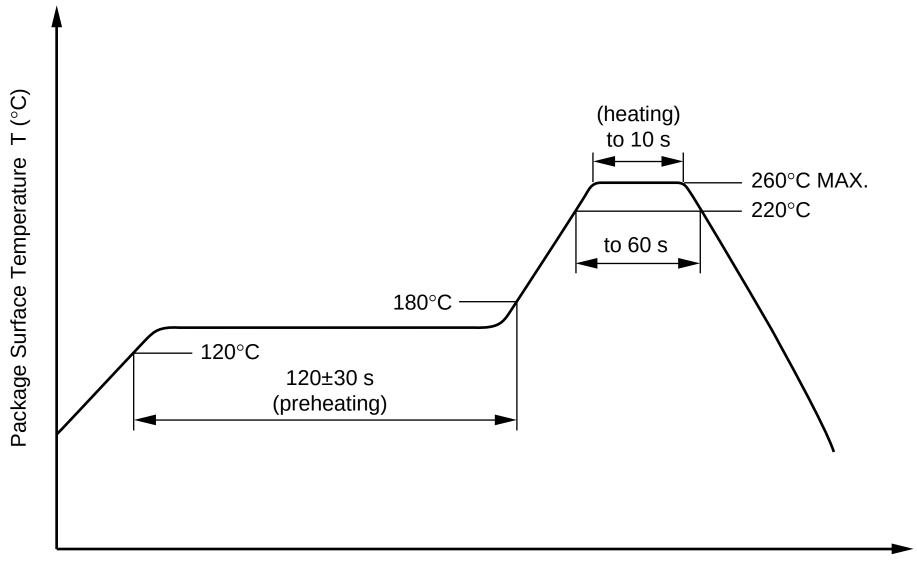
NOTES ON HANDLING

1. Recommended soldering conditions

(1) Infrared reflow soldering

• Peak reflow temperature	260°C or below (package surface temperature)
• Time of peak reflow temperature	10 seconds or less
• Time of temperature higher than 220°C	60 seconds or less
• Time to preheat temperature from 120 to 180°C	120±30 s
• Number of reflows	Three
• Flux	Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

Recommended Temperature Profile of Infrared Reflow



(2) Wave soldering

• Temperature	260°C or below (molten solder temperature)
• Time	10 seconds or less
• Preheating conditions	120°C or below (package surface temperature)
• Number of times	One (Allowed to be dipped in solder including plastic mold portion.)
• Flux	Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

(3) Soldering by Soldering Iron

• Peak Temperature (lead part temperature)	350°C or below
• Time (each pins)	3 seconds or less
• Flux	Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

(a) Soldering of leads should be made at the point 1.5 to 2.0 mm from the root of the lead

(4) Cautions

• Fluxes

Avoid removing the residual flux with freon-based and chlorine-based cleaning solvent.

2. Cautions regarding noise

Be aware that when voltage is applied suddenly between the photocoupler's input and output at startup, the output transistor may enter the on state, even if the voltage is within the absolute maximum ratings.

<R> USAGE CAUTIONS

1. This product is weak for static electricity by designed with high-speed integrated circuit so protect against static electricity when handling.
2. Board designing

(1) Below figure shows a typical application circuit where the PS9551A is used. A digital filter (Sinc^3 filter) reduces high frequency quantization noise from the PS9551A and convers from one-bit data stream to 3-wire serial data.

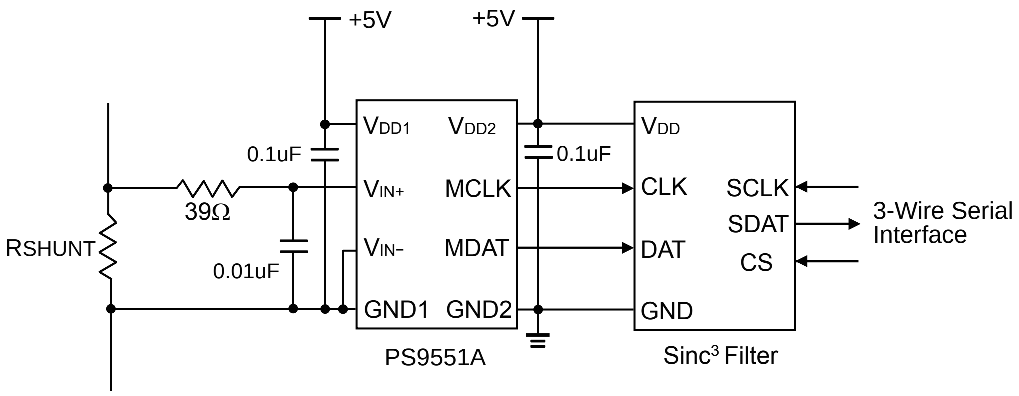


Fig. PS9551A Typical application circuit

(2) By-pass capacitor of more than 0.1 μF is used between V_{DD} and GND near device. Also, ensure that the distance between the leads of the photocoupler and capacitor is no more than 10 mm.

(3) Keep the pattern connected the input (V_{IN+}, V_{IN-}) and the output (MCLK, MDAT), respectively, as short as possible. MCLK and MDAT are digital signal, but when the lines between the photocoupler and a digital filter are long, the digital filter might not read the data.
When using long lines, use a line driver between the photocoupler and the digital filter, and keep the pattern between the output (MCLK, MDAT) and the line driver as short as possible.

(4) Do not connect any routing to the portion of the frame exposed between the pins on the package of the photocoupler. If connected, it will affect the photocoupler's internal voltage and the photocoupler will not operate normally.

(5) Because the maximum frequency of the signal input to the photocoupler must be lower than the allowable frequency band, be sure to connect an anti-aliasing filter (an RC filter with R = 39 Ω and C = 0.01 μF, for example).

(6) When VDD is lower than 4.5 V that is the outside of recommended operating condition, the output (MCLK, MDAT) of this product is unstable, and this might produce undesirable operation. Be sure to check the operation of an IC that is connected to this product during Power-up and Power-down process. And we recommend to use a disable function (shutdown function) of the connected IC or a reset IC to avoid this undesirable operation.

3. Avoid storage at a high temperature and high humidity.

<R> SPECIFICATION OF VDE MARKS LICENSE DOCUMENT

Parameter	Symbol	Spec.	Unit
Climatic test class (IEC 60068-1/DIN EN 60068-1)		40/105/21	
Dielectric strength maximum operating isolation voltage Test voltage (partial discharge test, procedure a for type test and random test) $U_{pr} = 1.6 \times U_{IORM}$, $P_d < 5$ pC	 U_{IORM} U_{pr}	 1 130 1 808	 V_{peak} V_{peak}
Test voltage (partial discharge test, procedure b for all devices) $U_{pr} = 1.875 \times U_{IORM}$, $P_d < 5$ pC	U_{pr}	2 119	V_{peak}
Highest permissible overvoltage	U_{TR}	8 000	V_{peak}
Degree of pollution (DIN EN 60664-1 VDE 0110 Part 1)		2	
Comparative tracking index (IEC 60112/DIN EN 60112 (VDE 0303 Part 11))	CTI	175	
Material group (DIN EN 60664-1 VDE 0110 Part 1)		III a	
Storage temperature range	T_{stg}	–55 to +125	°C
Operating temperature range	T_A	–40 to +105	°C
Isolation resistance, minimum value $V_{IO} = 500$ V dc at $T_A = 25$°C $V_{IO} = 500$ V dc at T_A MAX. at least 100°C	 Ris MIN. Ris MIN.	 10^{12} 10^{11}	 Ω Ω
Safety maximum ratings (maximum permissible in case of fault, see thermal derating curve) Package temperature Current (input current I_F, Psi = 0) Power (output or total power dissipation) Isolation resistance $V_{IO} = 500$ V dc at T_A = Tsi	 Tsi Isi Psi Ris MIN.	 175 400 700 10^9	 °C mA mW Ω

Caution GaAs Products	This product uses gallium arsenide (GaAs). GaAs vapor and powder are hazardous to human health if inhaled or ingested, so please observe the following points. • Follow related laws and ordinances when disposing of the product. If there are no applicable laws and/or ordinances, dispose of the product as recommended below. 1. Commission a disposal company able to (with a license to) collect, transport and dispose of materials that contain arsenic and other such industrial waste materials. 2. Exclude the product from general industrial waste and household garbage, and ensure that the product is controlled (as industrial waste subject to special control) up until final disposal. • Do not burn, destroy, cut, crush, or chemically dissolve the product. • Do not lick the product or in any way allow it to enter the mouth.

Revision History	PS9551AL4 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Mar 20, 2014	Throughout	Preliminary Data Sheet -> Data Sheet
		Throughout	Safety standards approved
		p.3	Modification of MARKING EXAMPLE Addition of ORDERING INFORMATION
		p.4	Modification of ABSOLUTE MAXIMUM RATINGS Modification of RECOMMENDED OPERATING CONDITIONS
		p.5 to 7	Modification of ELECTRICAL CHARACTERISTICS
		p.8 to 9	Addition of TEST CIRCUIT
		p.10 to 12	Addition of TYPICAL CHARACTERISTICS
		p.14	Addition of RECOMMENDED MOUNT PAD DIMENSIONS
		p.16	Modification of USAGE CAUTIONS
		p.17	Addition of SPECIFICATION OF VDE MARKS LICENSE DOCUMENT

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