

## Quad high-side smart power solid-state relay

Datasheet - production data



- Open drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2
- ESD according to IEC 61000-4-2 up to +/- 25 kV

### Features

Type	$V_{\text{demag}}^{(1)}$	$R_{\text{DS(on)}}^{(1)}$	$I_{\text{out}}^{(1)}$	$V_{\text{CC}}$
VNI4140K	$V_{\text{CC}}-41 \text{ V}$	$0.08 \Omega$	$0.7 \text{ A}$	$41 \text{ V}$

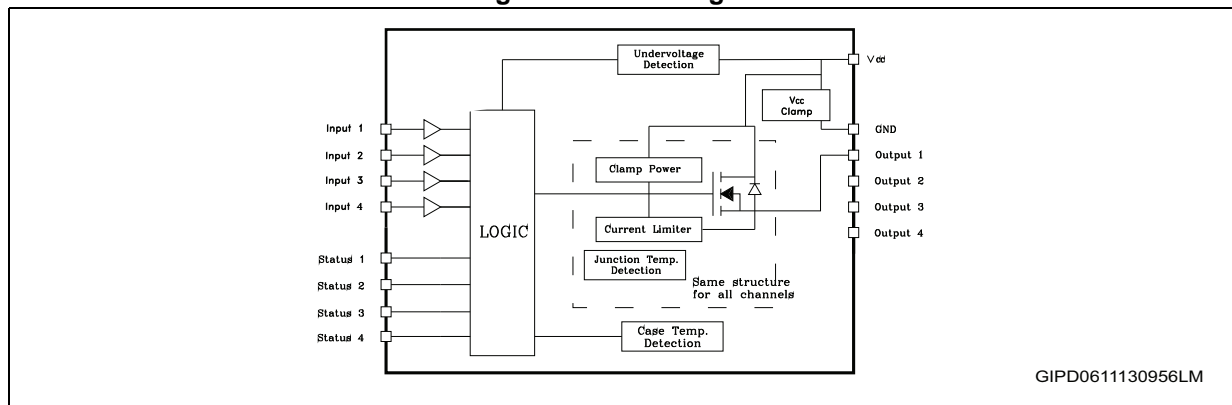
1. Per channel.

- Output current: 0.7 A per channel
- Shorted load protections
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shutdown restart not simultaneous for the various channels
- Protection against loss of ground
- Current limitation
- Undervoltage shutdown

### Description

The VNI4140K is a monolithic device made using STMicroelectronics VIPower technology, intended to drive four independent resistive or inductive loads with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. In overload conditions, channel turns OFF and back ON automatically so to maintain junction temperature between  $T_{\text{TSD}}$  and  $T_{\text{R}}$ . If this condition makes case temperature reach  $T_{\text{CSD}}$ , overloaded channel is turned OFF and restart only when case temperature has decreased down to  $T_{\text{CR}}$ . In case of more than one channel in overload, restart of the overloaded channels is not simultaneous, in order to avoid high peak current from the supply. Non-overloaded channels continue operating normally. The open drain diagnostics outputs indicate overtemperature conditions.

Figure 1. Block diagram



# Contents

<b>1</b>	<b>Pin connection</b> .....	<b>3</b>
<b>2</b>	<b>Maximum ratings</b> .....	<b>5</b>
	2.1 Thermal data .....	5
<b>3</b>	<b>Electrical characteristics</b> .....	<b>6</b>
<b>4</b>	<b>Truth table</b> .....	<b>9</b>
<b>5</b>	<b>Typical application circuit</b> .....	<b>9</b>
<b>6</b>	<b>Switching waveforms</b> .....	<b>11</b>
<b>7</b>	<b>Pin functions</b> .....	<b>12</b>
<b>8</b>	<b>Package and PC board thermal data</b> .....	<b>14</b>
	8.1 VNI4140K thermal data .....	14
<b>9</b>	<b>Reverse polarity protection</b> .....	<b>16</b>
<b>10</b>	<b>Demagnetization energy</b> .....	<b>17</b>
<b>11</b>	<b>Package mechanical data</b> .....	<b>18</b>
<b>12</b>	<b>Ordering information</b> .....	<b>23</b>
<b>13</b>	<b>Revision history</b> .....	<b>24</b>

# 1 Pin connection

Figure 2. Pin connection (top view)

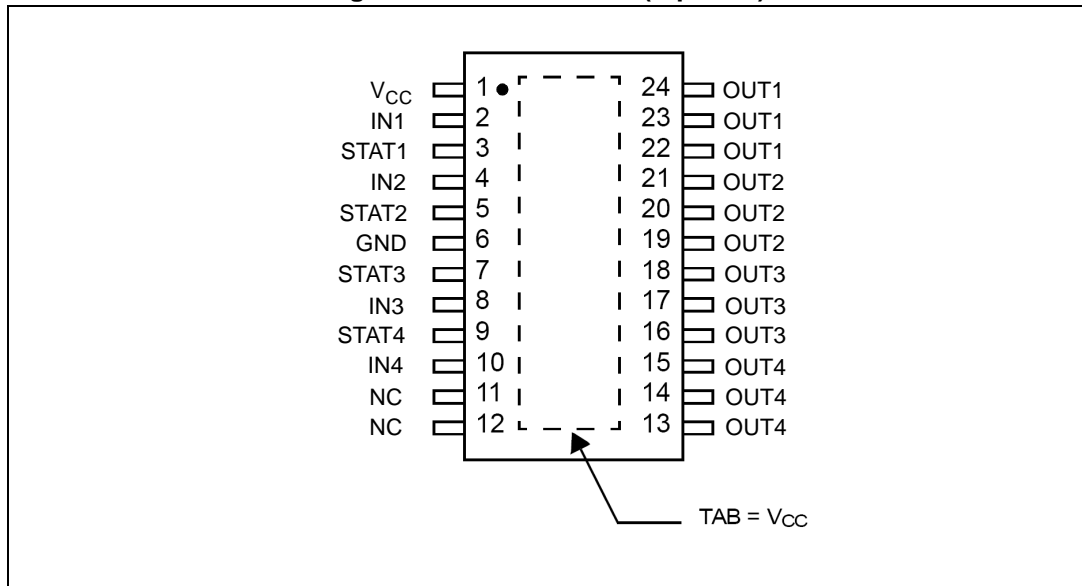


Table 1. Pin description

Pin	Name	Description
Tab	TAB	Exposed tab internally connected to V <sub>CC</sub>
1	V <sub>CC</sub>	Supply voltage
2	IN1	Channel 1 input 3.3 V CMOS/TTL compatible
3	STAT1	Channel 1 status in open drain configuration
4	IN2	Channel 2 input 3.3 V CMOS/TTL compatible
5	STA2	Channel 2 status in open drain configuration
6	GND	Device ground connection
7	STAT3	Channel 3 status in open drain configuration
8	IN3	Channel 3 input 3.3 V CMOS/TTL compatible
9	STAT4	Channel 4 status in open drain configuration
10	IN4	Channel 4 input 3.3 V CMOS/TTL compatible
11	NC	
12	NC	
13	OUT4	Channel 4 power stage output, internally protected
14	OUT4	Channel 4 power stage output, internally protected
15	OUT4	Channel 4 power stage output, internally protected
16	OUT3	Channel 3 power stage output, internally protected
17	OUT3	Channel 3 power stage output, internally protected

Table 1. Pin description (continued)

Pin	Name	Description
18	OUT3	Channel 3 power stage output, internally protected
19	OUT2	Channel 2 power stage output, internally protected
20	OUT2	Channel 2 power stage output, internally protected
21	OUT2	Channel 2 power stage output, internally protected
22	OUT1	Channel 1 power stage output, internally protected
23	OUT1	Channel 1 power stage output, internally protected
24	OUT1	Channel 1 power stage output, internally protected

## 2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	Power supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$I_{GND}$	DC ground reverse current	-250	mA
$I_{OUT}$	Output current (continuous)	Internally limited	A
$I_R$	Reverse output current (per channel)	-5	A
$I_{IN}$	Input current (per channel)	$\pm 10$	mA
$V_{IN}$	Input voltage	$+V_{CC}$	V
$V_{STAT}$	Status pin voltage	$+V_{CC}$	V
$I_{STAT}$	Status pin current	$\pm 10$	mA
$V_{ESD}$	Electrostatic discharge (R = 1.5 k $\Omega$ ; C = 100 pF)	2000	V
$E_{AS}$	$I_{OUT} = 500$ mA $T_{AMB} = 125$ °C	5	J
$P_{TOT}$	Power dissipation at $T_C = 25$ °C	Internally limited	W
$T_J$	Junction operating temperature	Internally limited	°C
$T_{STG}$	Storage temperature	-55 to 150	°C

### 2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case <sup>(1)</sup>	Max. 2	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	Max. see <a href="#">Figure 11</a>	°C/W

1. Per channel.

### 3 Electrical characteristics

10.5 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>J</sub> < 125 °C; unless otherwise specified

**Table 4. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply voltage		10.5		36	V
R <sub>DS(on)</sub>	On-state resistance	I <sub>OUT</sub> = 0.5 A at T <sub>J</sub> = 25 °C I <sub>OUT</sub> = 0.5 A			0.080 0.140	Ω Ω
V <sub>clamp</sub>		I <sub>s</sub> = 20 mA	41	45	52	V
I <sub>S</sub>	Supply current	All channels in OFF state ON state with V <sub>IN</sub> = 5 V (T <sub>J</sub> = 125 °C)		250 2.4	4	μA mA
I <sub>LGND</sub>	Output current at turn-off	V <sub>CC</sub> = V <sub>STAT</sub> = V <sub>IN</sub> = V <sub>GND</sub> = 24 V, V <sub>OUT</sub> = 0 V			1	mA
V <sub>OUT(OFF)</sub>	Off state output voltage	V <sub>IN</sub> = 0 V and I <sub>OUT</sub> = 0 A			1	V
I <sub>OUT(OFF)</sub>	Off state output current	V <sub>IN</sub> = V <sub>OUT</sub> = 0 V	0		5	μA
F <sub>CP</sub>	Charge pump frequency	Channel in ON state <sup>(1)</sup>		1450		kHz

1. To cover EN55022 class A and class B normative.

V<sub>CC</sub> = 24 V; -40 °C < T<sub>J</sub> < 125 °C, R<sub>L</sub> = 48 Ω, input rise time < 0.1 μs

**Table 5. Switching**

Symbol	Parameter	Min.	Typ.	Max.	Unit
t <sub>d(ON)</sub>	Turn on delay	-	20	-	μs
t <sub>r</sub>	Rise time	-	10	-	μs
t <sub>d(OFF)</sub>	Turn off	-	30	-	μs
t <sub>f</sub>	Fall time	-	8	-	μs
dV/dt <sub>(ON)</sub>	Turn on voltage slope	-	3	-	V/μs
dV/dt <sub>(OFF)</sub>	Turn off voltage slope	-	4	-	V/μs

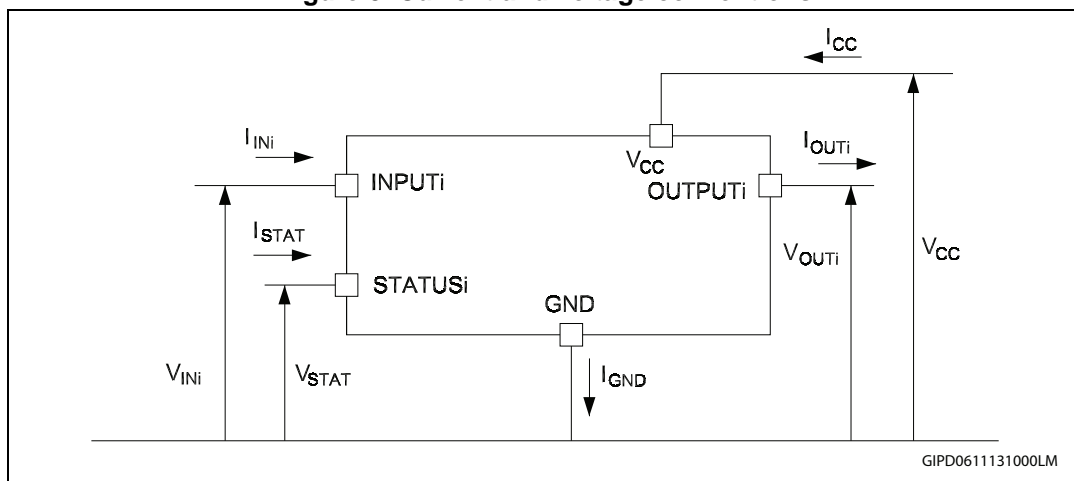
Table 6. Logical input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.8	V
$V_{IH}$	Input high level voltage		2.20			V
$V_{I(HYST)}$	Input hysteresis voltage			0.15		V
$I_{IN}$	Input current	$V_{IN} = 15\text{ V}$			10	$\mu\text{A}$
		$V_{IN} = 36\text{ V}$			210	

Table 7. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{STAT}$	Status voltage output low	$I_{STAT} = 1.6\text{ mA}$			0.6	V
$V_{USD}$	Undervoltage protection		7		10.5	V
$V_{USDHYS}$	Undervoltage hysteresis		0.4	0.5		V
$I_{LIM}$	DC short-circuit current	$V_{CC} = 24\text{ V}; R_{LOAD} < 10\text{ m}\Omega$	0.7	1	1.7	A
$I_{PEAK}$	Maximum DC output current	Dynamic load		1.3		A
HYST	Tracking limits			0.2		A
$I_{LSTAT}$	Status leakage current	$V_{CC} = V_{STAT} = 36\text{ V}$		30		$\mu\text{A}$
$T_{TSD}$	Junction shutdown temperature		150	170	190	$^{\circ}\text{C}$
$T_R$	Junction reset temperature		135			$^{\circ}\text{C}$
$T_{HYST}$	Junction thermal hysteresis		7	15		$^{\circ}\text{C}$
$T_{CSD}$	Case shutdown temperature		125	130	135	$^{\circ}\text{C}$
$T_{CR}$	Case reset temperature		110			$^{\circ}\text{C}$
$T_{CHYST}$	Case thermal hysteresis		7	15		$^{\circ}\text{C}$
$V_{demag}$	Output voltage at turn-off	$I_{OUT} = 0.5\text{ A}; L_{LOAD} \geq 1\text{ mH}$	$V_{CC}-41$	$V_{CC}-45$	$V_{CC}-52$	V

Figure 3. Current and voltage conventions





## 4 Truth table

Table 8. Truth table

Condition	INPUTn	OUTPUTn	STATUSn
Normal operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Shorted load (current limitation)	L	L	H
	H	X	H

## 5 Typical application circuit

Figure 4. Typical application circuit

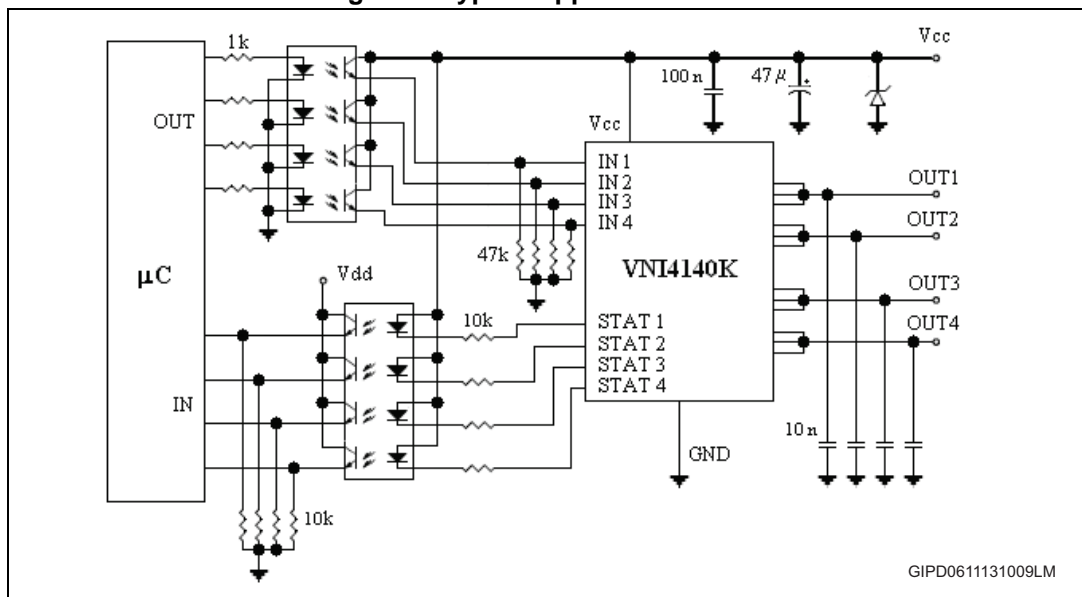
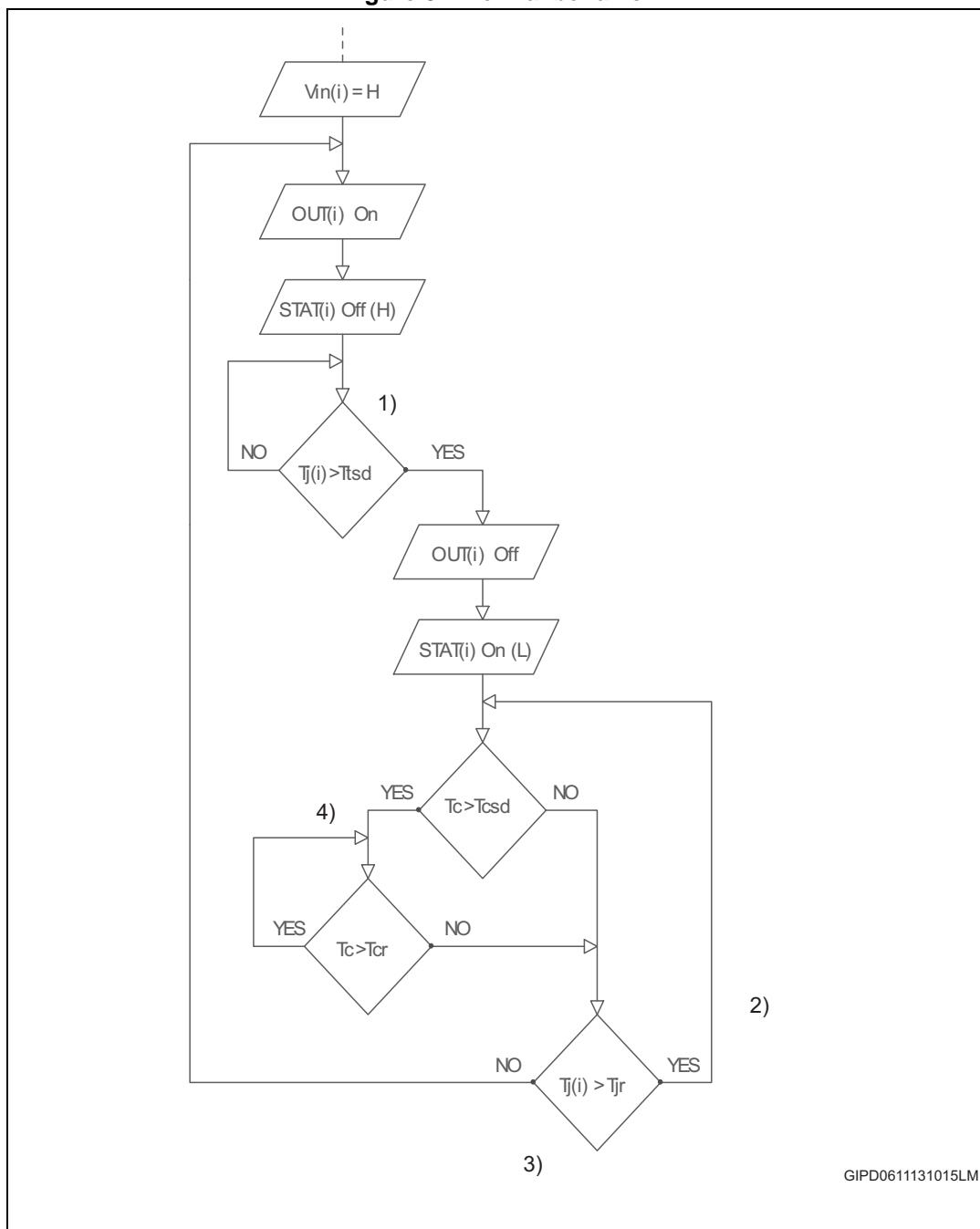
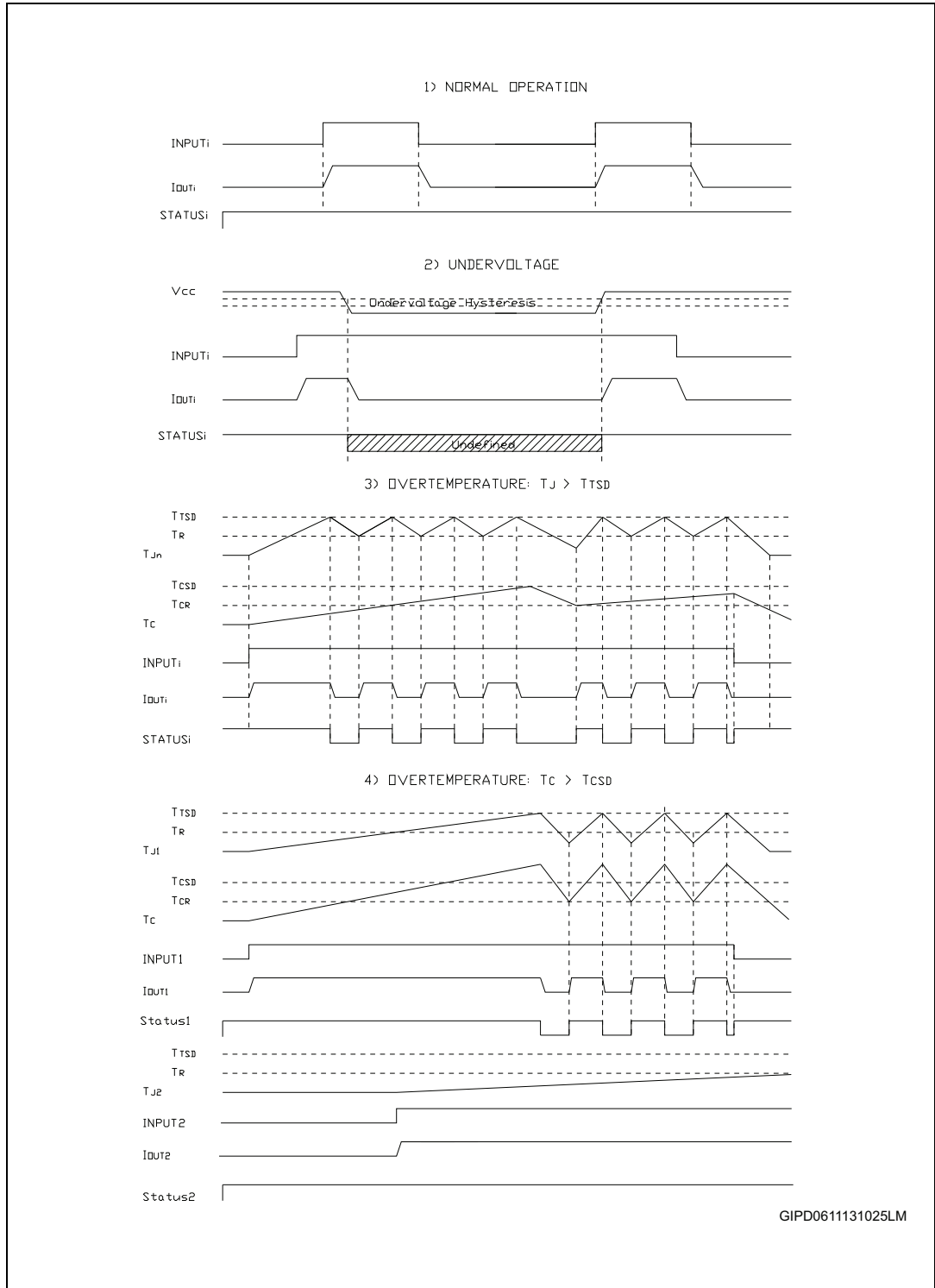


Figure 5. Thermal behavior



# 6 Switching waveforms

Figure 6. Switching waveforms



# 7 Pin functions

Figure 7. Input circuit

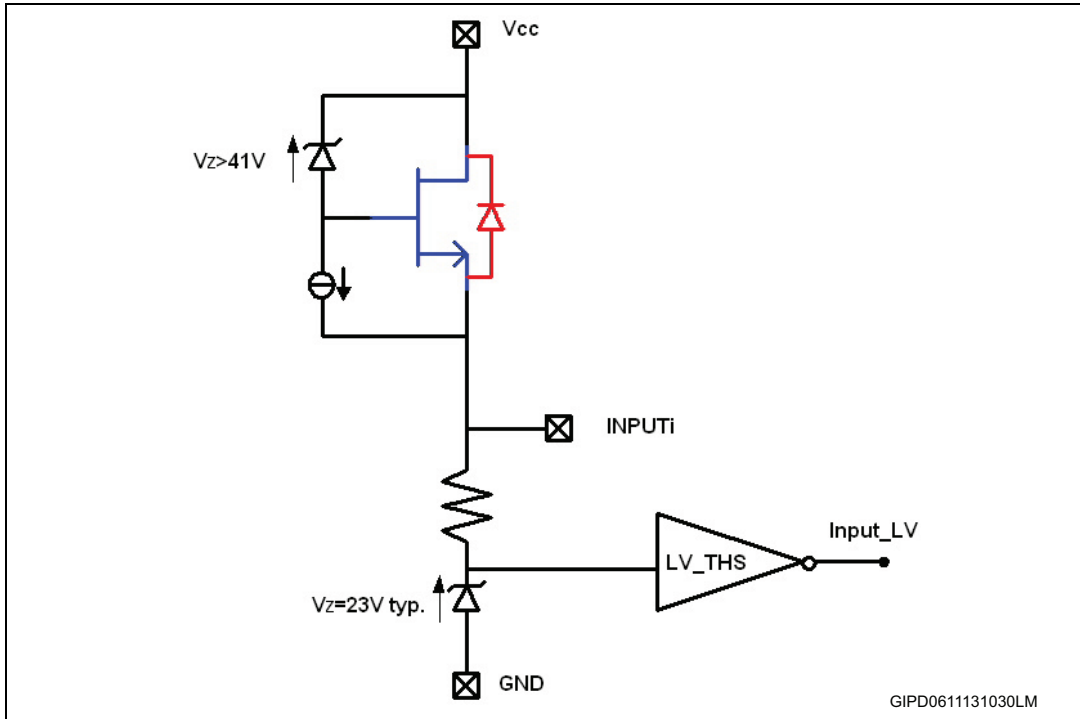


Figure 8. Status circuit

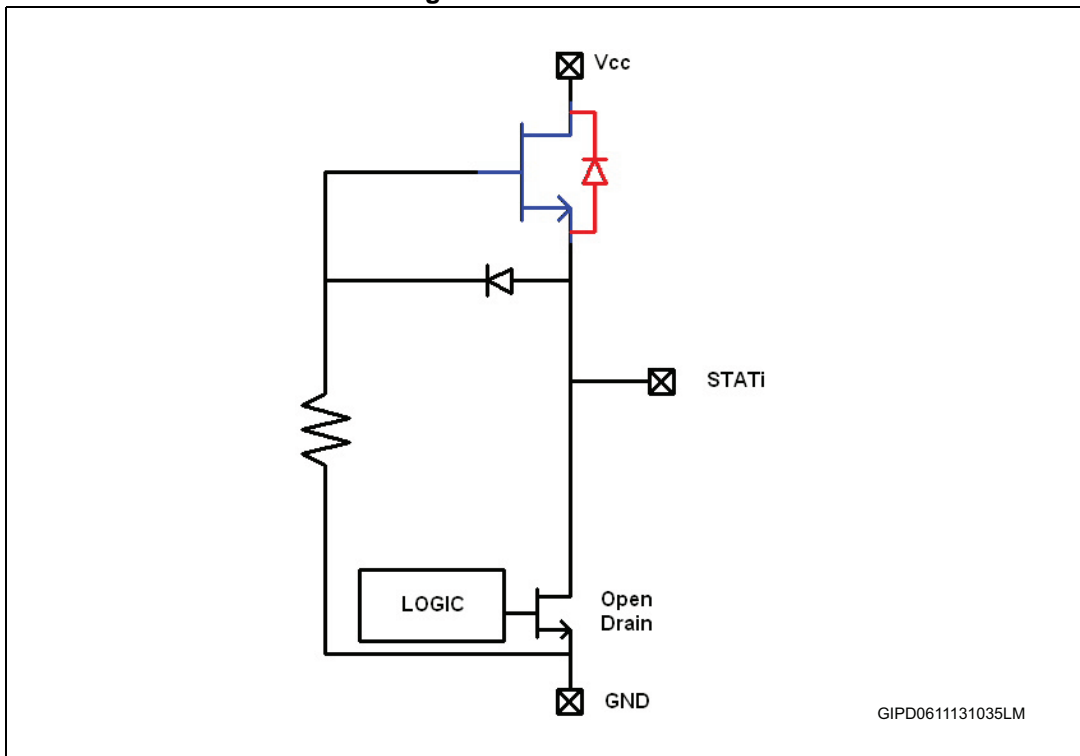
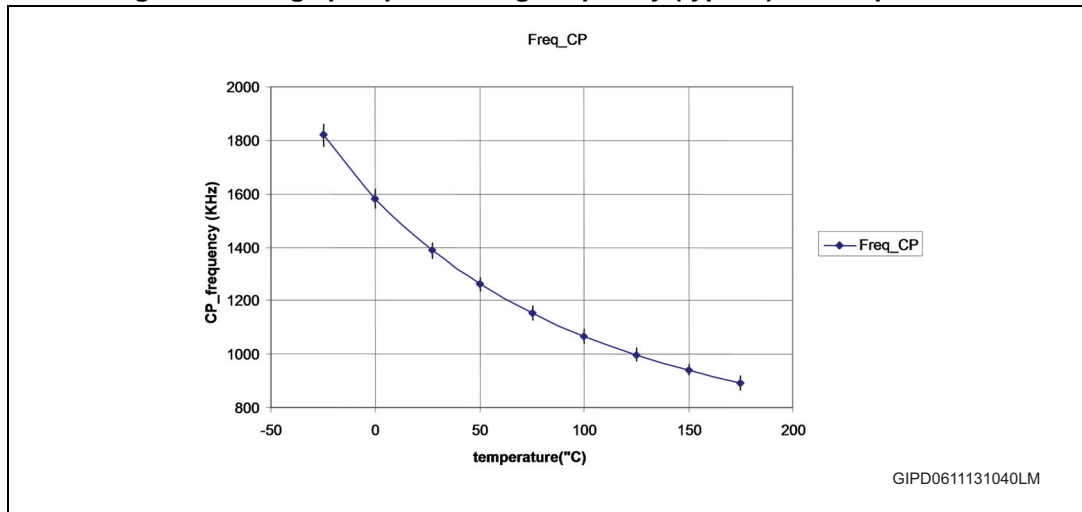


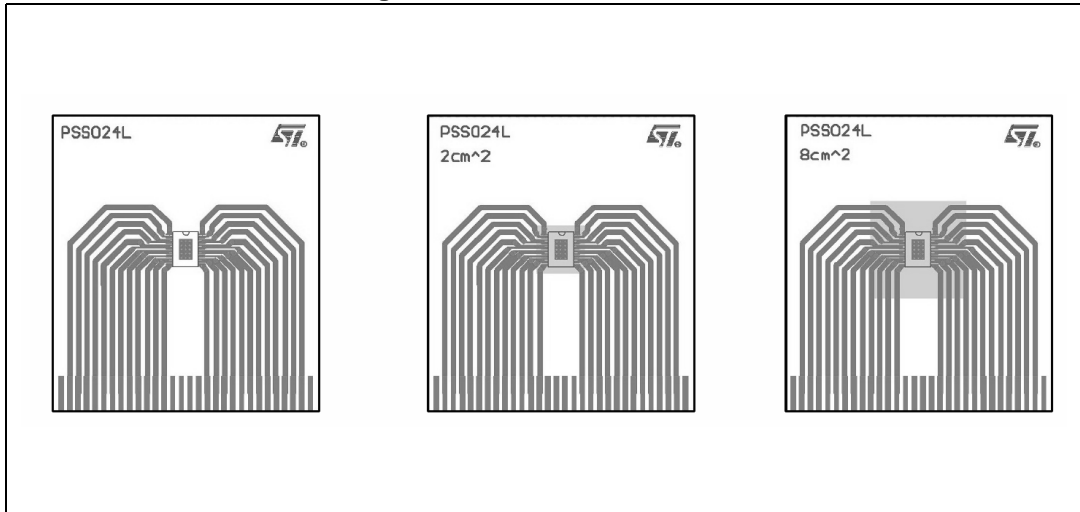
Figure 9. Charge pump switching frequency (typical) vs. temperature



## 8 Package and PC board thermal data

### 8.1 VNI4140K thermal data

Figure 10. VNI4140K PC board



Note: *Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 mm (front and back side), copper areas: from minimum pad layout to 8 cm<sup>2</sup>).*

Figure 11.  $R_{th(JA)}$  vs. PCB copper area in open box free air condition (one channel ON)

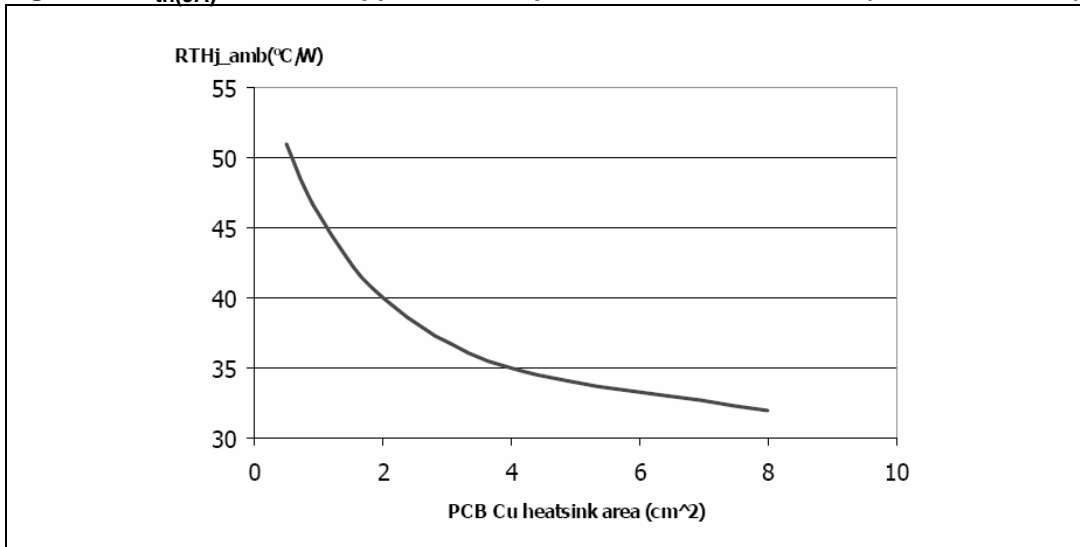
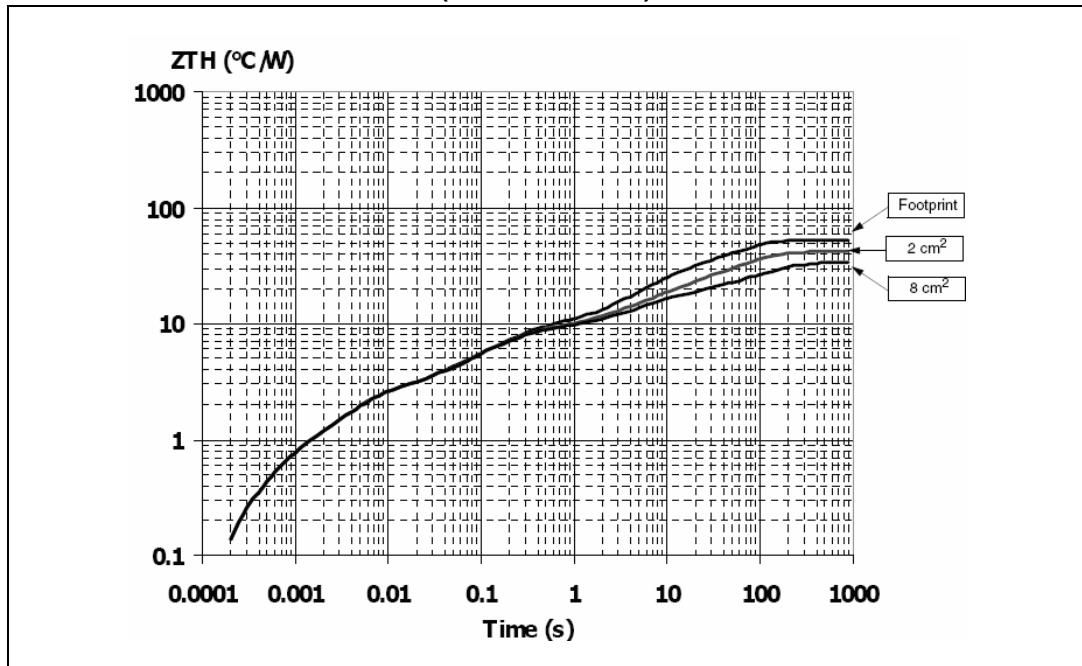


Figure 12. VNI4140K thermal impedance junction ambient single pulse (one channel on)



## 9 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:

1. Placing a resistor ( $R_{GND}$ ) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

### Equation 1

$$R_{GND} \geq V_{CC}/I_{GND}$$

where  $I_{GND}$  is the DC reverse ground pin current and can be found in [Section 2: Maximum ratings](#) of this datasheet.

Power dissipated by  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse polarity situations) is:

### Equation 2

$$PD = (V_{CC})^2/R_{GND}$$

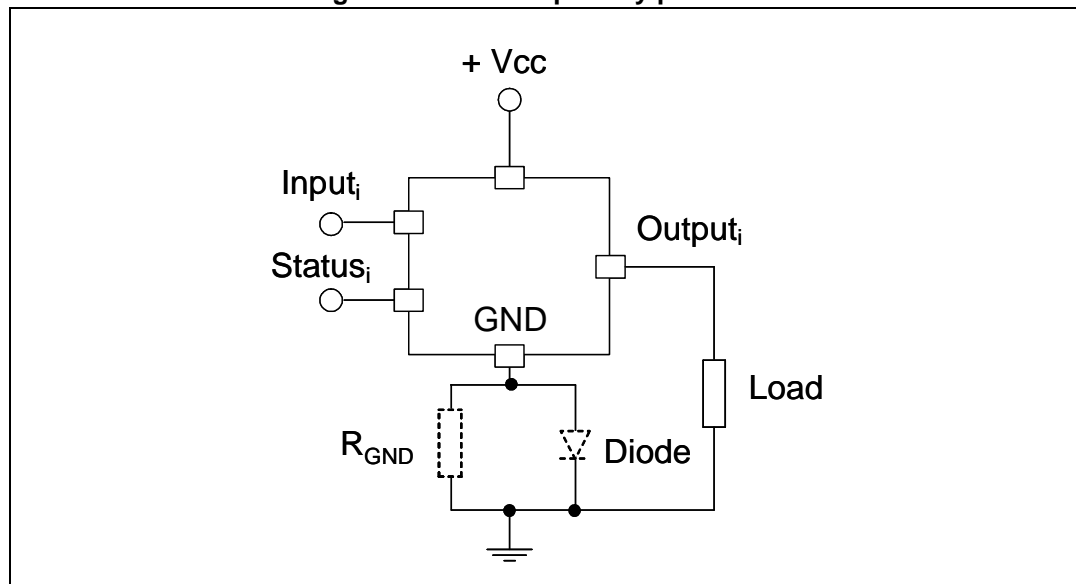
If option 2 is selected, the diode has to be chosen by taking into account  $VRRM > |V_{CC}|$  and its power dissipation capability:

### Equation 3

$$P_D \geq I_S * V_f$$

*Note:* In normal conditions (no reverse polarity) due to the diode, there is a voltage drop between GND of the device and GND of the system.

Figure 13. Reverse polarity protection

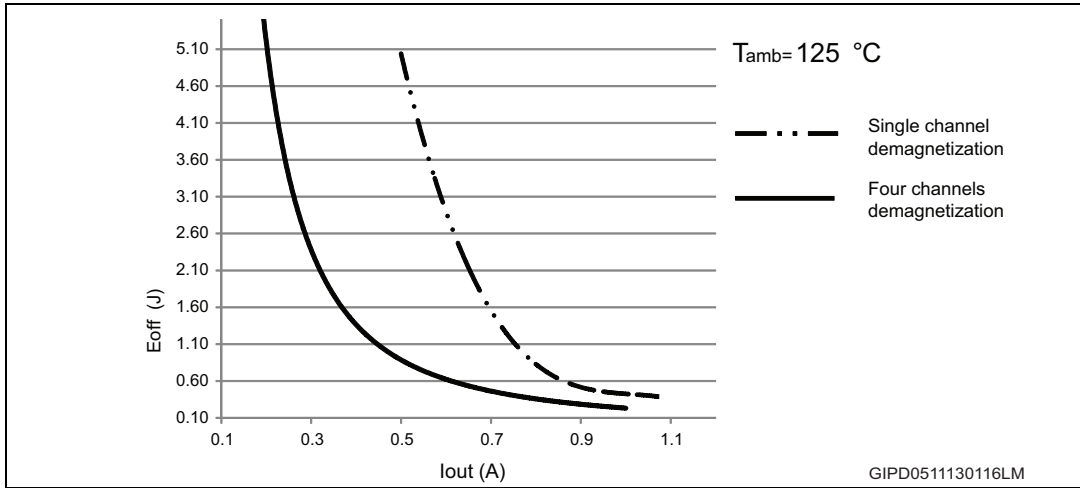


This schematic can be used with any type of load.



# 10 Demagnetization energy

Figure 14. Maximum demagnetization energy vs. load current, typical values



## 11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 9. PowerSSO-24 mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

Figure 15. PowerSSO-24 package dimensions

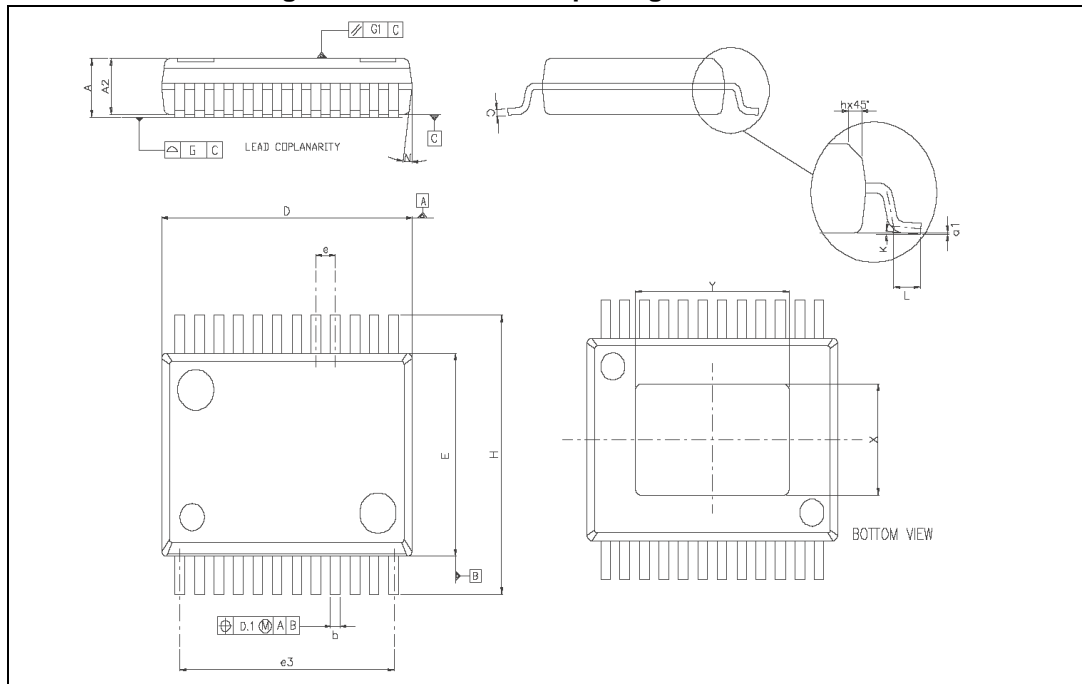


Figure 16. PowerSSO-24 tube shipment (no suffix)

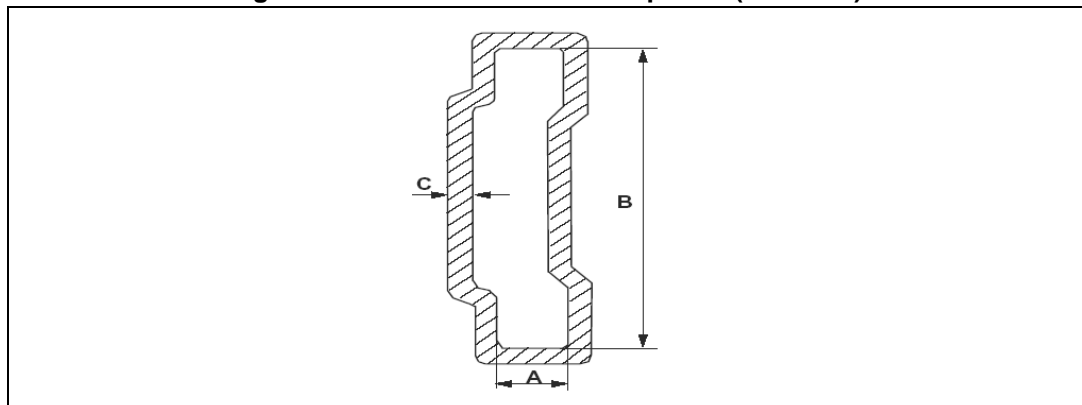


Table 10. PowerSSO-24 tube shipment

Base quantity	49
Bulk quantity	1225
Tube length ( $\pm 0.5$ )	532
A	3.5
B	13.8
C ( $\pm 0.1$ )	0.6

Note: All dimensions are in mm.

Figure 17. PowerSSO-24 reel shipment (suffix "TR")

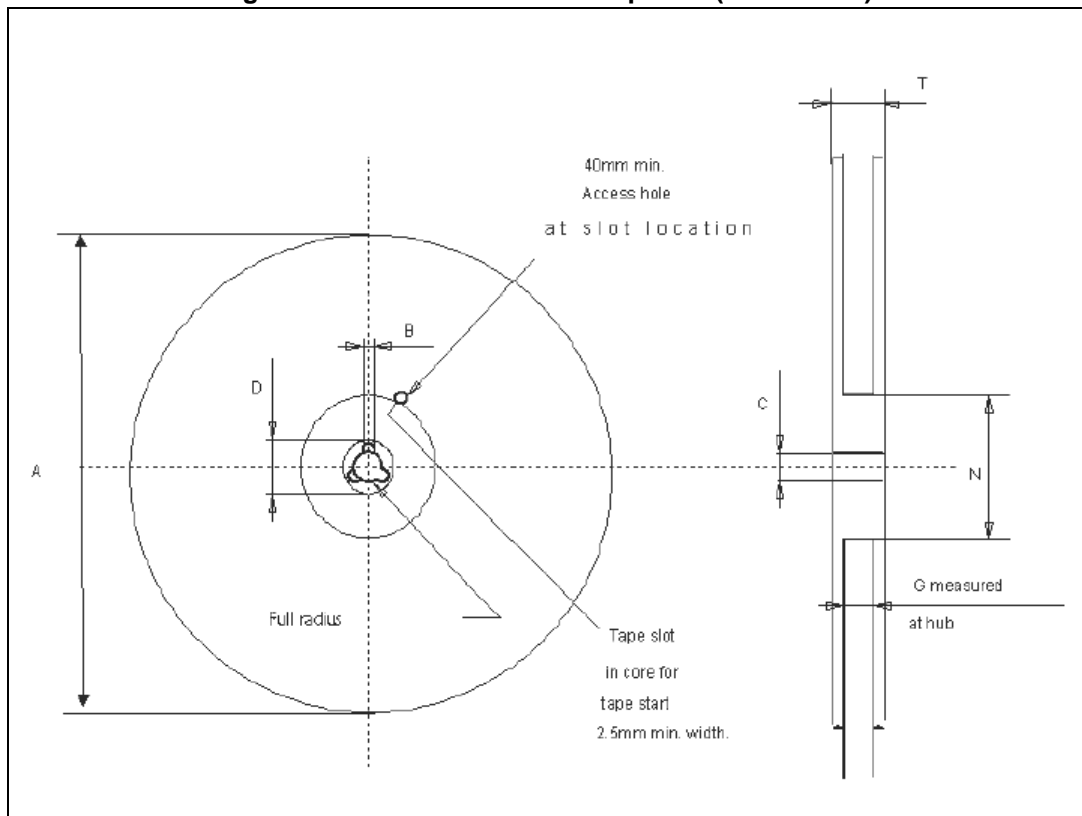


Table 11. PowerSSO-24 reel dimensions

Base quantity	1000
Bulk quantity	1000
A (max.)	330
B (min.)	1.5
C ( $\pm 0.2$ )	13
F	20.2
G ( $2 \pm 0$ )	24.4
N (min.)	100
T (max.)	30.4

Figure 18. PowerSSO-24™ tape dimensions

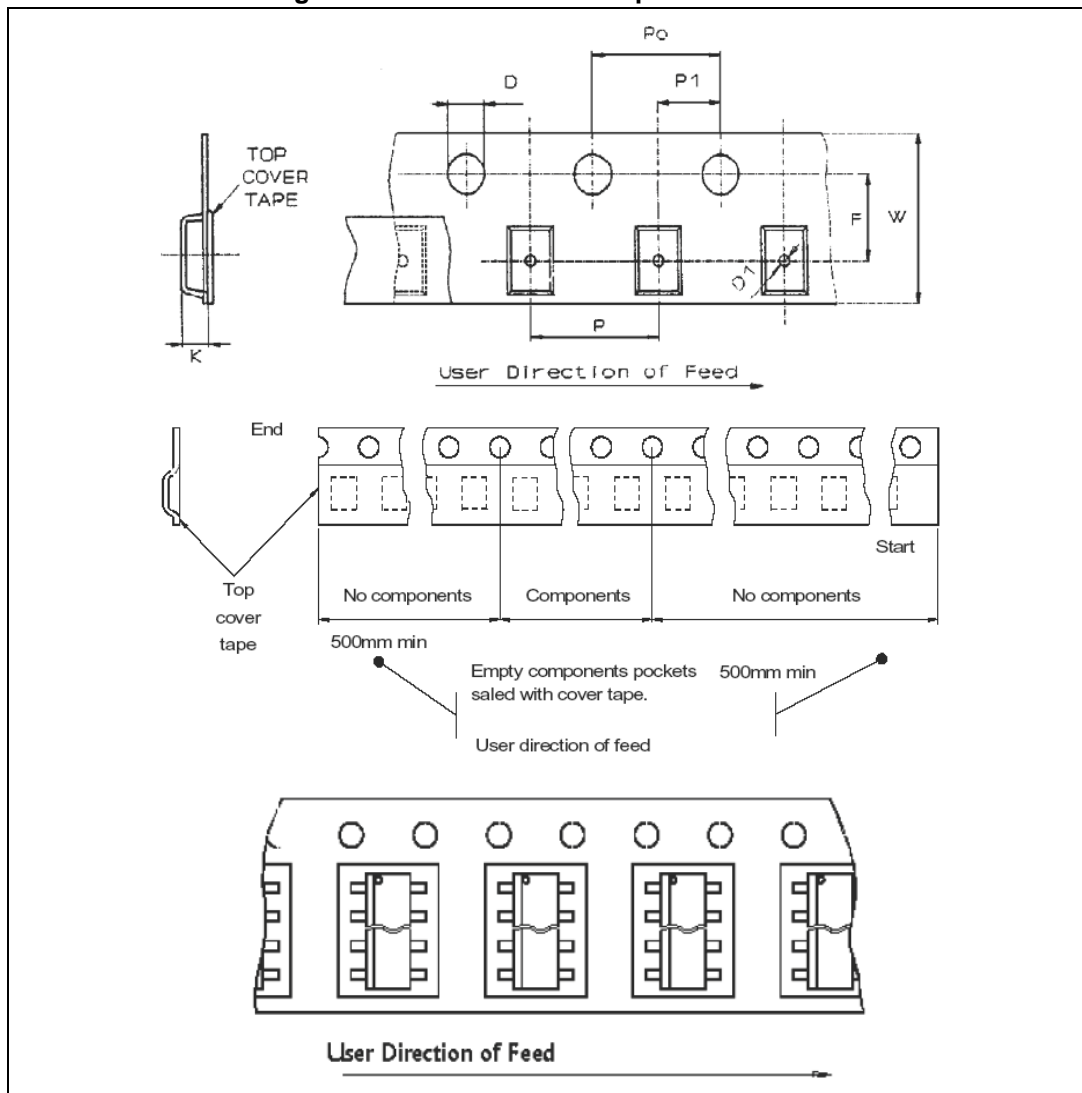
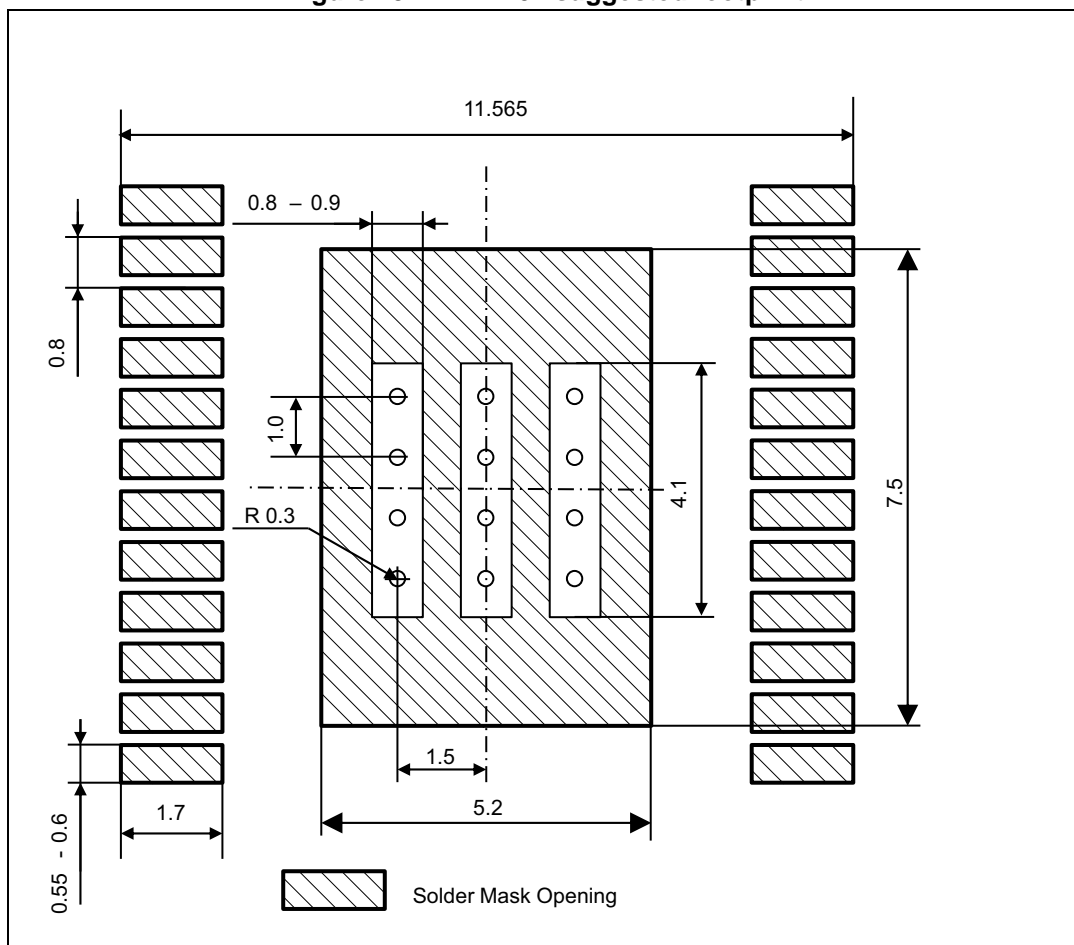


Table 12. PowerSSO-24™ tape dimensions

Tape width	W	24
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	12
Hole diameter	D (± 0.05)	1.55
Hole diameter	D1 (min.)	1.5
Hole position	F (± 0.1)	11.5
Compartment depth	K (max.)	2.85
Hole spacing	P1 (± 0.1)	2

Note: According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Figure 19. VN14140k suggested footprint



Note: STMicroelectronics is not responsible for any PCB related issues. The footprint shown in the above figure is a suggestion which might not be in line to the customer PCB supplier design rules.

All dimensions are in mm.

## 12 Ordering information

**Table 13. Order code**

<b>Order code</b>	<b>Package</b>	<b>Packaging</b>
VNI4140K	PowerSSO-24	Tube
VNI4140KTR	PowerSSO-24	Tape and reel

## 13 Revision history

**Table 14. Document revision history**

Date	Revision	Changes
16-Nov-2007	1	Initial release.
26-Nov-2007	2	Updated electrical parameters values.
08-Jul-2008	3	Inserted: <i>Figure 4 on page 9</i> and <i>Section 9: Reverse polarity protection on page 16</i> .
08-Apr-2008	4	Added $I_{LGND}$ parameter in <i>Table 4 on page 6</i> .
27-Aug-2009	5	Updated <i>Section 9: Reverse polarity protection</i> .
09-Dec-2009	6	Added <i>Section 10: Conformity to IEC 61000-4-2 ESD immunity test</i> .
15-Apr-2010	7	Updated <i>Table 5 on page 6</i> .
06-Feb-2012	8	Inserted feature: conformity to IEC 61000-4-2 ESD immunity test in cover page. Removed chapter: conformity to IEC 61000-4-2 ESD immunity test.
05-Mar-2012	9	Suggested footprint inserted. In <i>Table 4</i> parameter $I_{LGND}$ has been added.
19-Mar-2012	10	Minor text changes.
20-Dec-2012	11	Operating temperature range extended.
06-Nov-2013	12	Updated $E_{AS}$ value in <i>Table 2: Absolute maximum ratings</i> . Added <i>Figure 14</i> .
11-Dec-2013	13	Updated <i>Section 9</i> .



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