STRUCTURE Silicon monolithic integrated circuit

PRODUCT SERIES Motor driver for ink jet printer

(H-bridge driver 2ch, switching regulator 1ch, reset output)

TYPE **BD64560EUV**

FUNCTION
- External reset input terminal function
- Built-in thermal shut down circuit
- Built-in UVLO circuit

○Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Supply voltage	V_M	-0.4～40.0	V
Logic input voltage	V_L	-0.4～5.5	V
RNF voltage (DC)	V_{RNF}(DC)	0.5	V
Power dissipation	Pd	1.70※1	W
		4.32※2	
Operating temperature range	T_{opt}	-25～+85	℃
Storage temperature range	T_{stg}	-55～+150	℃
Junction temperature	T_{jmax}	150	℃
Motor driver maximum output current (peak500ns)	I_{out}(peak)	8.0	A
Motor driver maximum output current (DC)	I_{out}(DC)	2.5※3	A
Switching Reg maximum output current (DC)	I_{out}	1.5	A

※1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 13.6mW/℃ for operating above Ta=25℃.
※2 4-layer recommended board. Derating in done at 34.6mW/℃ for operating above Ta=25℃.
※3 Do not, however exceed Pd, ASO and Tjmax=150℃.

○Recommended operating conditions (Ta= -25～+85℃)

Parameter	Symbol	Limit	Unit
Supply voltage	V_M	7～36	V
CLK input frequency	f_{CLK}	1～25	MHz
Switching Reg output voltage range	V_{OUT}	1～V_M×0.5	V

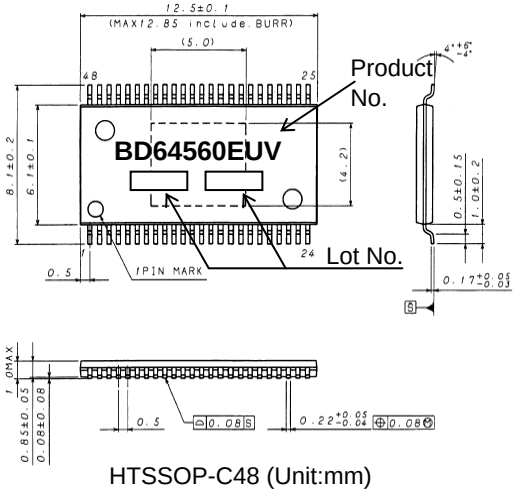
This product isn't designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

○Electrical characteristics (Unless otherwise specified, Ta=25℃, V_M=32V)

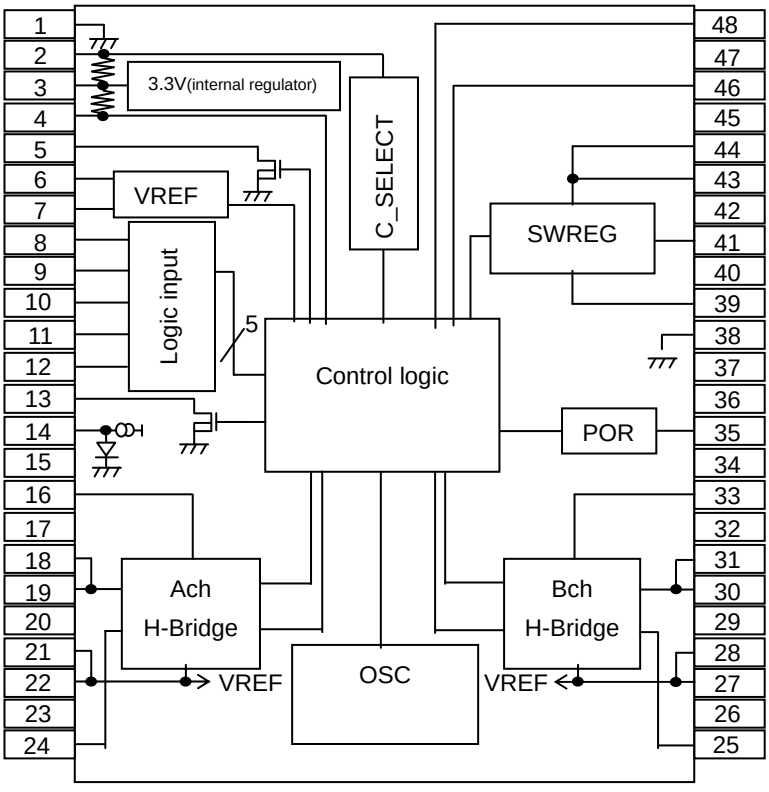
Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
VM current 1	I_{M1}	-	-	2	mA	SLEEP=L SWREG=OFF
VM current 2	I_{M2}	-	-	15	mA	SLEEP=H SWREG=Max Duty
Control logic (C_SELECT, IRT, SLEEP, STROBE/ENABLE_A, CLK/PHASE_A, DATA/PHASE_B, ENABLE_B)						
High input voltage	V_{LINH}	2.0	-	5.5	V	
Low input voltage	V_{LINL}	0	-	0.8	V	
Input current	I_{LIN}	15	33	50	uA	Input voltage=3.3V
C_SELECT Low input voltage	V_{CSELL}	0	-	0.8	V	
C_SELECT Middle input voltage	V_{CSELM}	1.20	1.65	2.10	V	
C_SELECT High input voltage	V_{CSELH}	2.5	3.3	-	V	
C_SELECT input current	I_{CSEL}	-45	-33	-21	uA	C_SELECT=0V
IRT High input voltage	V_{IRTH}	2.0	-	5.5	V	
IRT Low input voltage	V_{IRTL}	0	-	0.8	V	
IRT input current	I_{IRT}	-50	-33	-15	uA	IRT=0V
H bridge						
Output on resistance (High side)	R_{ONH}	-	0.70	0.84	Ω	I_{OUT}=1A
Output on resistance (Low side)	R_{ONL}	-	0.50	0.60	Ω	I_{OUT}=1A
Output leak current (High side)	I_{LEAKH}	-1	-	1	uA	V_M=40V、OUTxx=0V
Output leak current (Low side)	I_{LEAKL}	-1	-	1	uA	V_M=OUTxx=40V
RNF pin outflow current	I_{RNF}	10	20	30	uA	
VREF-RNF offset voltage	V_{OFST}	-5	0	5	%	VREF=2V GAIN=1/10 or 1/20
	※V_{OFST}={(VREF×GAIN−RNF threshold voltage) / (VREF×GAIN)}×100%					
VREF voltage range	V_{VREF}	0.8	-	3.0	V	
VREF pin outflow current	I_{VREF}	-1	0	1	uA	VREF=2V
High motor UVLO voltage	V_{UVLOH}	13.5	15.0	16.5	V	
Low motor UVLO voltage	V_{UVLOL}	12.5	14.0	15.5	V	
Switching regulator						
FB threshold voltage	V_{FB}	0.873	0.900	0.927	V	
FB pin outflow current	I_{FB}	-1	0	1	uA	
Output on resistance	R_{ONSW}	-	0.70	0.84	Ω	I_{OUT}=0.5A
Leak current	I_{LEAKSW}	-1	0	1	uA	V_M=40V、SWOUT=0V
FB over voltage protection	V_{FBOVP}	1.10	1.20	1.30	V	Disabled at turn on
FB under voltage protection	V_{FBUVP}	0.55	0.60	0.65	V	Disabled at turn on
ORT pin						
Output voltage	V_{ORT}	-	-	0.4	V	I_{DRAIN}=5mA
Leak current	$I_{LEAKORT}$	-1	0	1	uA	
VM threshold voltage	V_{POR}	5.9	6.3	6.7	V	No hysteresis
L_OUT pin						
Output voltage	V_{LOUT}	-	-	0.5	V	I_{DRAIN}=5mA
Leak current	$I_{LEAKLOUT}$	-1	0	1	uA	

○Package outline



HTSSOP-C48 (Unit:mm)

○Block diagram



○Pin No. / Pin name

Pin No.	Pin name	Pin No.	Pin name
1	LGND	48	TEST2
2	C_SELECT	47	NC
3	CC	46	TEST1
4	IRT	45	NC
5	ORT	44	VMSW
6	VREFA	43	VMSW
7	VREFB	42	NC
8	SLEEP	41	SWOUT
9	STROBE /ENABLE_A	40	NC
10	CLK /PHASE_A	39	FB
11	DATA /PHASE_B	38	AGND
12	ENABLE_B	37	NC
13	L_OUT	36	NC
14	TJMON	35	VM
15	NC	34	NC
16	OUTAM	33	OUTBM
17	NC	32	NC
18	VMA	31	VMB
19	VMA	30	VMB
20	NC	29	NC
21	RNFA	28	RNFB
22	RNFA	27	RNFB
23	NC	26	NC
24	OUTAP	25	OUTBP

NC：Non Connection

○Operation Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Power supply lines

As return of current regenerated by back EMF of motor happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) GND potential

The potential of GND pin must be minimum potential in all operating conditions.

(4) Metal on the backside (Define the side where product markings are printed as front)

The metal on the backside is shorted with the backside of IC chip therefore it should be connected to GND. Be aware that there is a possibility of malfunction or destruction if it is shorted with any potential other than GND.

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency . Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

(6) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(7) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(8) Thermal shutdown circuit

The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes Tjmax=150℃, and higher, coil output to the motor and regulator output will be OFF, and reset output will be L. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

(9) Ground Wiring Pattern

When using both large current and small signal GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

(10) TEST pin

Be sure to leave TEST1 pin open and connect TEST2 pin to GND.

Notes

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