

NCP391

Positive Overvoltage Protection Controller with Internal Low R_{ON} NMOS FET

The NCP391 is able to disconnect the systems from its output pin when wrong input operating conditions are detected. The system is positive overvoltage protected up to +28 V.

This device uses an internal NMOS and therefore, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP391 is able to instantaneously disconnect the output from the input, due to integrated Low R_{ON} Power NMOS, if the input voltage exceeds the overvoltage threshold (OVLO) or falls below the undervoltage threshold (UVLO).

At powerup (\overline{EN} pin = low level), the V_{out} turns on t_{on} time after the V_{in} exceeds the undervoltage threshold.

The NCP391 provides a negative going flag (\overline{FLAG}) output, which alerts the system that a fault has occurred.

In addition, the device has ESD-protected input (15 kV Air) when bypassed with a 1.0 μ F or larger capacitor.

Features

- Overvoltage Protection up to 28 V
- On-Chip Low $R_{DS(on)}$ NMOS Transistor
- Internal Charge Pump
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Soft-Start
- Alert \overline{FLAG} Output
- Shutdown \overline{EN} Input
- Compliance to IEC61000-4-2 (Level 4)
8.0 kV (Contact)
15 kV (Air)
- ESD Ratings: Machine Model = B
Human Body Model = 2
- WLCSP6 1.31x1.04 mm Package
- This is a Pb-Free Device

Applications

- Cell Phones
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications
- MP3 Players



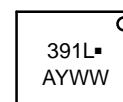
ON Semiconductor®

<http://onsemi.com>

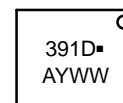


WLCSP6
FCAL SUFFIX
CASE 499BP

MARKING DIAGRAM

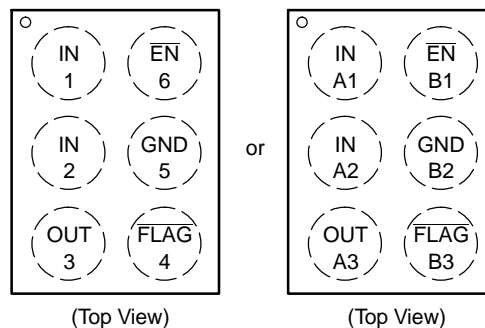


WLCSP6
FCCAD SUFFIX
CASE 567JW



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 12 of this data sheet.

NCP391

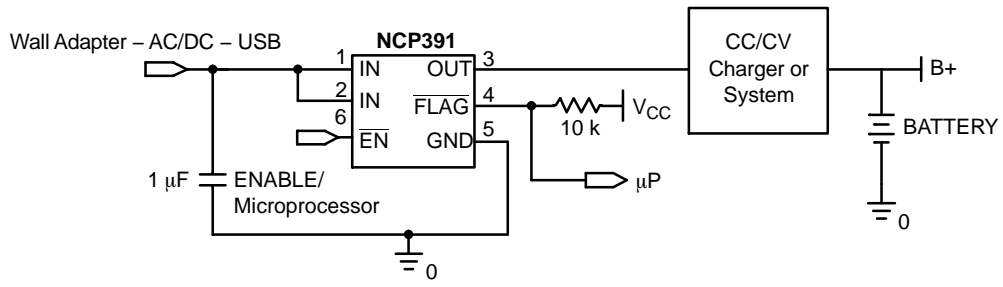


Figure 1. Typical Application Circuit

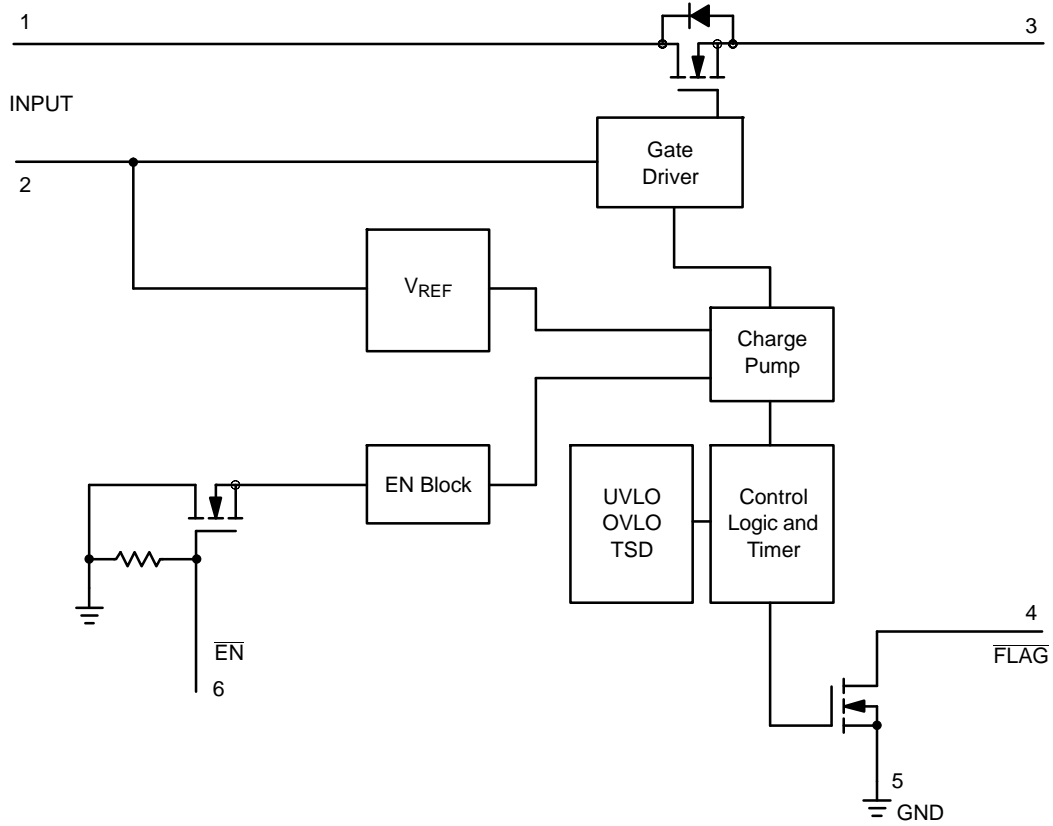


Figure 2. Functional Block Diagram

NCP391

PIN FUNCTION DESCRIPTION

| Pin No. | Symbol | Function | Description |
|----------------|------------------------|----------|--|
| 1, 2 or A1, A2 | IN | INPUT | Input Voltage Pins. These pins are connected to the Wall Adapter (AC-DC, Vbus ..). A 1 μ F low ESR ceramic capacitor, or larger, must be connected between these pins and GND, as close as possible to the DUT. The two IN pins must be connected together to power supply. (See PCB recommendation for the pin7). |
| 3 or A3 | OUT | OUTPUT | Output Voltage Pins. This pin follows IN pins when “no fault” is detected. |
| 4 or B3 | FLAG | OUTPUT | Fault Indication Pin. This pin allows an external system to detect a fault on the IN pins. The FLAG pin goes low when input voltage exceeds OVLO threshold or drops below UVLO threshold or when TSD is exceeded. Since the FLAG pin is open drain functionality, an external pull-up resistor to V _{CC} must be added. (Minimum 10 k Ω). |
| 5 or B2 | GND | POWER | Ground |
| 6 or B1 | $\overline{\text{EN}}$ | INPUT | Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{\text{EN}}$ pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|------------------------------------|------------------------------------|--------------|
| Minimum Voltage (IN to GND) | V _{min_{in}} | -0.3 | V |
| Minimum Voltage (All others to GND) | V _{min} | -0.3 | V |
| Maximum Voltage (IN to GND) | V _{max_{in}} | 30 | V |
| Maximum Voltage (All others to GND) | V _{max} | 7.0 | V |
| Maximum Current (UVLO < V _{IN} < OVLO) | I _{max} | 2.0 | A |
| Maximum Peak Current (t \leq 1 ms, T _A = 85°C) | I _{max_{peak}} | 4.0 | A |
| Thermal Resistance, Junction-to-Air (Note 1) | R _{θJA} | 130 | °C/W |
| Operating Ambient Temperature Range | T _A | -40 to +85 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |
| Junction Operating Temperature | T _J | 150 | °C |
| ESD Withstand Voltage (IEC 61000-4-2) (input only) when bypassed with 1.0 μ F capacitor Human Body Model (HBM), Model = 2 (Note 2) Machine Model (MM) Model = B (Note 3) | V _{esd} | 15 Air, 8.0 Contact 2000 200 | kV V V |
| Moisture Sensitivity | MSL | Level 1 | - |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The R _{θ JA} is highly dependent on the PCB heat sink area (connected to pin 7).
2. Human Body Model, 100 pF discharged through a 1.5 k Ω resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

NCP391

ELECTRICAL CHARACTERISTICS – NCP391FCALT2G (Min/Max limits values ($-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$) and $V_{in} = +5.0\text{ V}$. Typical values are $T_A = +25^{\circ}\text{C}$, unless otherwise noted.)

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|--------------------------|---|------|------|------|--------------------|
| Input Voltage Range | V_{in} | – | 1.2 | – | 28 | V |
| Undervoltage Lockout Threshold (Note 4) NCP391FCAL | UVLO | V_{in} falls below UVLO threshold from 5 V to 2.7 V | 2.8 | 2.95 | 3.1 | V |
| Undervoltage Lockout Hysteresis | UVLO _{hyst} | V_{in} rises above UVLO + UVLO _{hyst} | 30 | 60 | 90 | mV |
| Overvoltage Lockout Threshold (Note 4) NCP391FCAL | OVLO | V_{in} rises above OVLO threshold | 7.16 | 7.4 | 7.65 | V |
| Overvoltage Lockout Hysteresis NCP391FCAL | OVLO _{hyst} | V_{in} falls below OVLO + OVLO _{hyst} | 50 | 100 | 150 | mV |
| V_{in} versus V_{out} Resistance | $R_{DS(on)}$ | $V_{in} = 5.0\text{ V}$, $\overline{EN} = \text{GND}$, Load connected to V_{out} | – | 120 | 200 | m Ω |
| Supply Quiescent Current | I_{dd} | No load. $\overline{EN} = 5.0\text{ V}$ | – | 70 | 150 | μA |
| | | No load. $\overline{EN} = \text{Gnd}$ | – | 90 | 170 | μA |
| UVLO Supply Current | $I_{dd_{uvlo}}$ | $V_{IN} = 2.7\text{ V}$ | – | 60 | – | μA |
| MOSFET Leakage | I_{vdss} | $V_{IN} = 28\text{ V}$ | – | 10 | 500 | nA |
| \overline{FLAG} Output Low Voltage | $V_{ol_{flag}}$ | 1.2 V < V_{IN} < UVLO Sink 50 μA on \overline{FLAG} pin | – | 20 | 400 | mV |
| | | $V_{IN} > \text{OVLO}$ Sink 1.0 mA on \overline{FLAG} pin | – | – | 400 | mV |
| \overline{FLAG} Leakage Current | \overline{FLAG}_{leak} | \overline{FLAG} level = 5.0 V | – | 1.0 | – | nA |
| \overline{EN} Voltage High | V_{ih} | – | 1.2 | – | – | V |
| \overline{EN} Voltage Low | V_{ol} | – | – | – | 0.4 | V |
| \overline{EN} Leakage Current | \overline{EN}_{leak} | $\overline{EN} = 5.0\text{ V}$ or GND | – | 1.0 | – | nA |
| Thermal Shutdown Temperature | t_{SD} | – | – | 150 | – | $^{\circ}\text{C}$ |
| Thermal Shutdown Hysteresis | t_{SDhyst} | – | – | 15 | – | $^{\circ}\text{C}$ |

TIMINGS

| | | | | | | |
|----------------------------------|-------------|--|-----|-----|-----|---------------|
| Startup Delay | t_{on} | From $V_{in} > \text{UVLO}$ to $V_{out} = 0.3\text{ V}$ (See Figures 3 & 7) | 6.0 | 10 | 14 | ms |
| \overline{FLAG} Going Up Delay | t_{start} | From $V_{out} = 0.3\text{ V}$ to $\overline{FLAG} = 1.2\text{ V}$ (See Figures 3 & 9) | 6.0 | 10 | 14 | ms |
| Output Turn Off Time | t_{off} | From $V_{in} > \text{OVLO}$ to $V_{out} \leq 0.3\text{ V}$ (See Figures 4 & 8) V_{in} increasing from 5.0 V to 8.0 V at 3.0 V/ μs Rload connected on V_{out} | – | 1.5 | 5.0 | μs |
| Alert Delay | t_{stop} | From $V_{in} > \text{OVLO}$ to $\overline{FLAG} \leq 0.4\text{ V}$ (See Figures 4 & 10) V_{in} increasing from 5.0 V to 8.0 V at 3.0 V/ μs Rload connected on V_{out} | – | 1.0 | – | μs |
| Disable Time | t_{dis} | From $\overline{EN} > 1.2\text{ V}$ to $V_{out} < 0.3\text{ V}$ Rload = 5.0 Ω (See Figures 5 & 12) | – | 1.0 | 5.0 | μs |

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

4. Additional UVLO and OVLO thresholds ranging from UVLO and from OVLO can be manufactured. Contact your ON Semiconductor representative for availability.

NCP391

ELECTRICAL CHARACTERISTICS – NCP391FCCADT2G (Min/Max limits values ($-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$) and $V_{in} = +4.2\text{ V}$. Typical values are $T_A = +25^{\circ}\text{C}$, unless otherwise noted.)

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|--------------------------|--|-----|------|------|--------------------|
| Input Voltage Range | V_{in} | – | 1.2 | – | 28 | V |
| Undervoltage Lockout Threshold (Note 5) | UVLO | V_{in} falls below UVLO threshold from 4.2 V to 2.7 V | 2.8 | 2.95 | 3.1 | V |
| Undervoltage Lockout Hysteresis | UVLO _{hyst} | V_{in} rises above UVLO + UVLO _{hyst} | 30 | 60 | 90 | mV |
| Overshoot Lockout Threshold (Note 5) | OVLO | V_{in} rises above OVLO threshold | 4.8 | 4.95 | 5.1 | V |
| Overshoot Lockout Hysteresis | OVLO _{hyst} | V_{in} falls below OVLO + OVLO _{hyst} | 50 | 100 | 150 | mV |
| V_{in} versus V_{out} Resistance | $R_{DS(on)}$ | $V_{in} = 4.2\text{ V}$, $\overline{EN} = \text{GND}$, Load connected to V_{out} | – | 120 | 200 | m Ω |
| Supply Quiescent Current | I_{dd} | No load. $\overline{EN} = 4.2\text{ V}$ | – | 70 | 150 | μA |
| | | No load. $\overline{EN} = \text{Gnd}$ | – | 90 | 170 | μA |
| UVLO Supply Current | $I_{dd_{uvlo}}$ | $V_{IN} = 2.7\text{ V}$ | – | 60 | – | μA |
| MOSFET Leakage | I_{vdss} | $V_{IN} = 28\text{ V}$ | – | 10 | 500 | nA |
| \overline{FLAG} Output Low Voltage | $V_{ol_{flag}}$ | 1.2 V < V_{IN} < UVLO Sink 50 μA on \overline{FLAG} pin | – | 20 | 400 | mV |
| | | $V_{IN} > \text{OVLO}$ Sink 1.0 mA on \overline{FLAG} pin | – | – | 400 | mV |
| \overline{FLAG} Leakage Current | \overline{FLAG}_{leak} | \overline{FLAG} level = 4.2 V | – | 1.0 | – | nA |
| \overline{EN} Voltage High | V_{ih} | – | 1.2 | – | 4.95 | V |
| \overline{EN} Voltage Low | V_{ol} | – | – | – | 0.4 | V |
| \overline{EN} Leakage Current | \overline{EN}_{leak} | $\overline{EN} = 4.2\text{ V}$ or GND | – | 1.0 | – | nA |
| Thermal Shutdown Temperature | t_{SD} | – | – | 150 | – | $^{\circ}\text{C}$ |
| Thermal Shutdown Hysteresis | $t_{SD_{hyst}}$ | – | – | 15 | – | $^{\circ}\text{C}$ |

TIMINGS

| | | | | | | |
|----------------------------------|-------------|--|-----|-----|-----|---------------|
| Startup Delay | t_{on} | From $V_{in} > \text{UVLO}$ to $V_{out} = 0.3\text{ V}$ (See Figures 3 & 7) | 6.0 | 10 | 14 | ms |
| \overline{FLAG} Going Up Delay | t_{start} | From $V_{out} = 0.3\text{ V}$ to $\overline{FLAG} = 1.2\text{ V}$ (See Figures 3 & 9) | 6.0 | 10 | 14 | ms |
| Output Turn Off Time | t_{off} | From $V_{in} > \text{OVLO}$ to $V_{out} \leq 0.3\text{ V}$ (See Figures 4 & 8) V_{in} increasing from 4.2 V to 8.0 V at 3.0 V/ μs Rload connected on V_{out} | – | 1.5 | 5.0 | μs |
| Alert Delay | t_{stop} | From $V_{in} > \text{OVLO}$ to $\overline{FLAG} \leq 0.4\text{ V}$ (See Figures 4 & 10) V_{in} increasing from 4.2 V to 8.0 V at 3.0 V/ μs Rload connected on V_{out} | – | 1.0 | – | μs |
| Disable Time | t_{dis} | From $\overline{EN} > 1.2\text{ V}$ to $V_{out} < 0.3\text{ V}$ Rload = 5.0 Ω (See Figures 5 & 12) | – | 1.0 | 5.0 | μs |

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

5. Additional UVLO and OVLO thresholds ranging from UVLO and from OVLO can be manufactured. Contact your ON Semiconductor representative for availability.

NCP391

TIMING DIAGRAMS

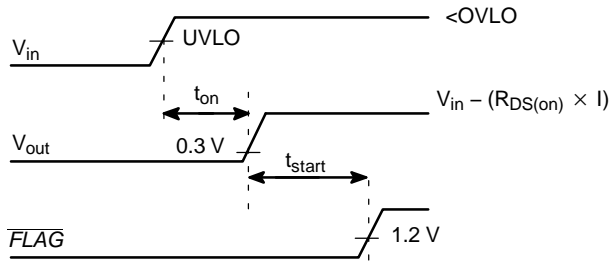


Figure 3. Startup

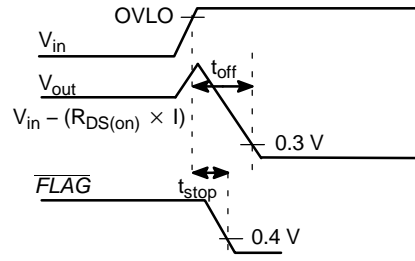


Figure 4. Shutdown on Overvoltage Detection

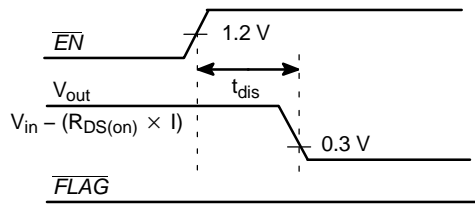


Figure 5. Disable on $\overline{EN} = 1$

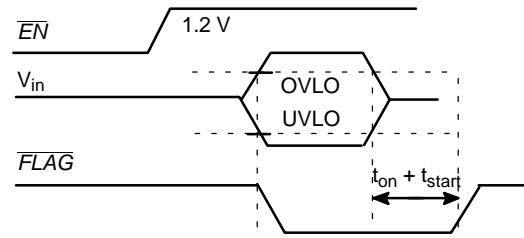


Figure 6. \overline{FLAG} Response with $\overline{EN} = 1$

NCP391

TYPICAL OPERATING CHARACTERISTICS

50 ms t_{on} and t_{start} version

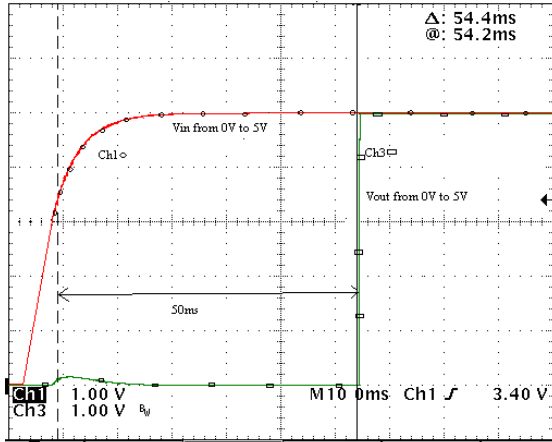


Figure 7. Startup
 $V_{in} = \text{Ch1}, V_{out} = \text{Ch3}$

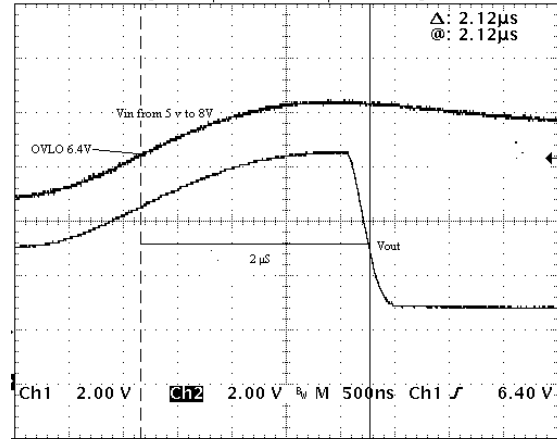


Figure 8. Output Turn Off Time
 $V_{in} = \text{Ch1}, V_{out} = \text{Ch2}$

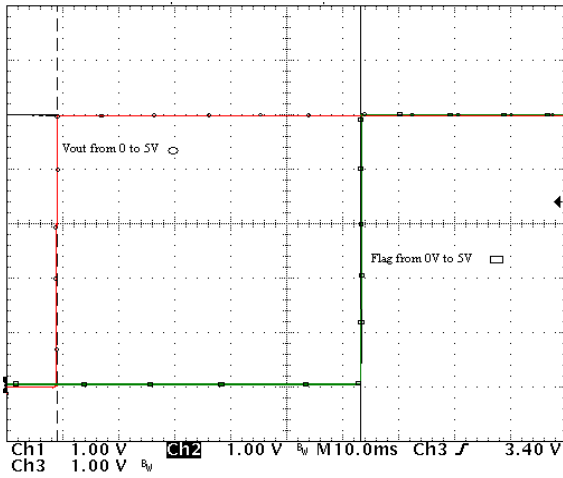


Figure 9. FLAG Going Up Delay
 $V_{out} = \text{Ch3}, \text{FLAG} = \text{Ch2}$

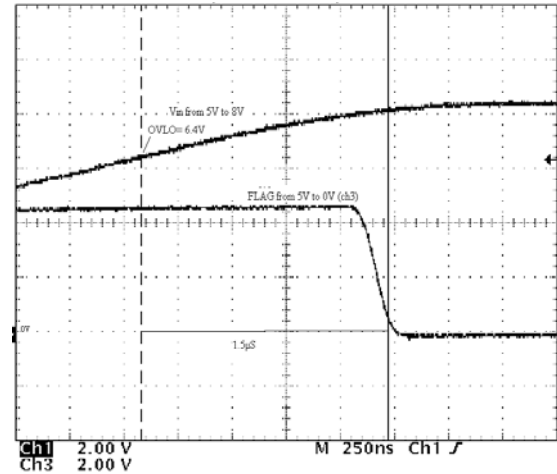


Figure 10. Alert Delay
 $V_{out} = \text{Ch1}, \text{FLAG} = \text{Ch3}$

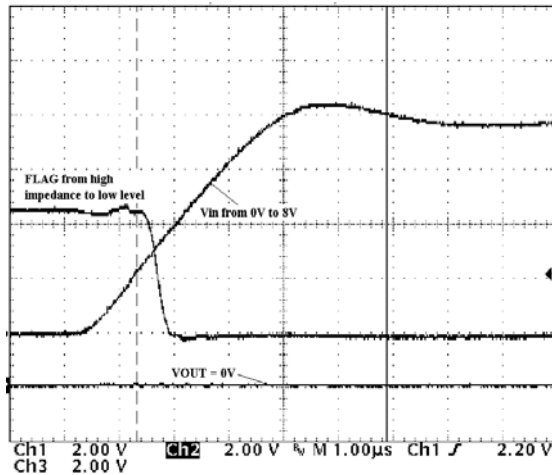


Figure 11. Initial Overvoltage Delay
 $V_{in} = \text{Ch1}, V_{out} = \text{Ch2}, \text{FLAG} = \text{Ch3}$

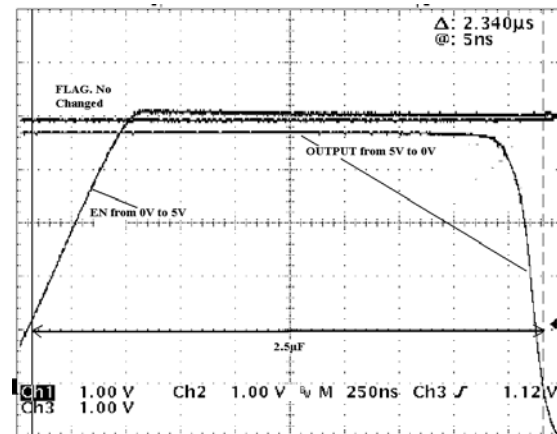


Figure 12. Disable Time
 $EN = \text{Ch1}, V_{out} = \text{Ch2}, \text{FLAG} = \text{Ch3}$

TYPICAL OPERATING CHARACTERISTICS

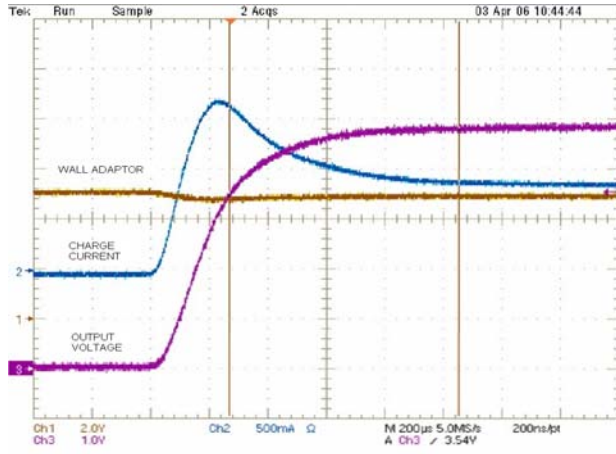


Figure 13. Inrush Current with $C_{out} = 100 \mu F$, $I_{charge} = 1 A$, Output Wall Adaptor Inductance $1 \mu H$

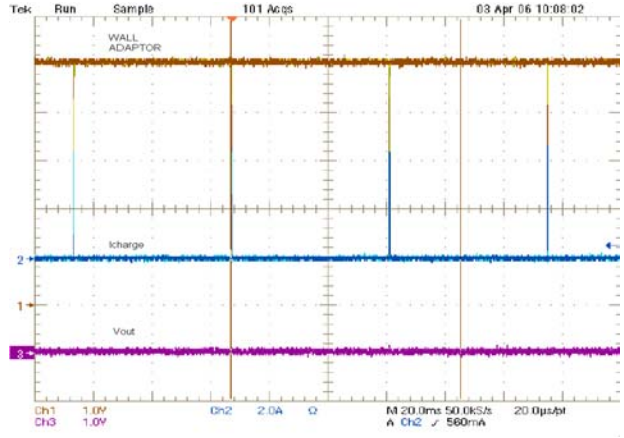


Figure 14. Output Short Circuit

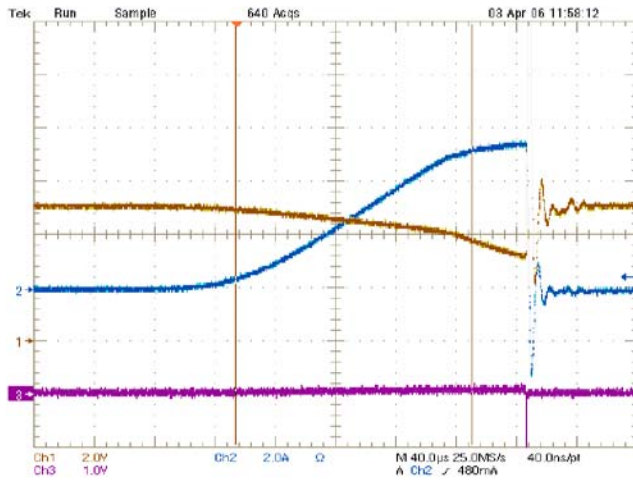


Figure 15. Output Short Circuit (Zoom Fig. 14)

NCP391

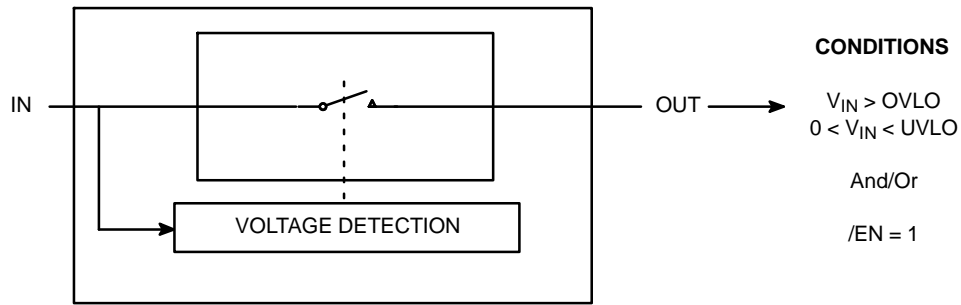


Figure 16. Simplified Diagram

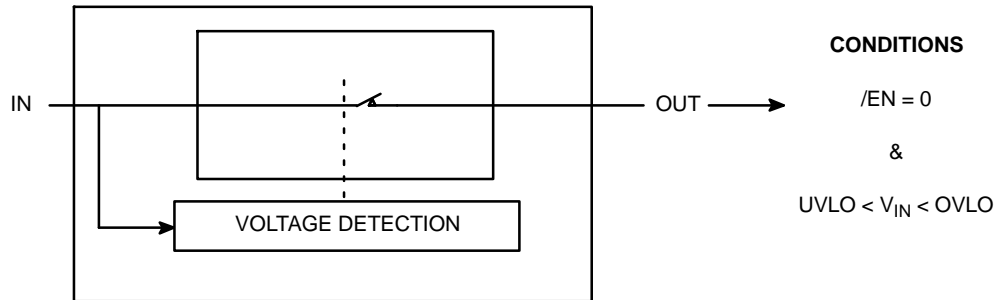


Figure 17. Simplified Diagram

Operation

The NCP391 provides overvoltage protection for positive voltage, up to 28 V. A low $R_{DS(on)}$ NMOSFET protects the systems (i.e.: charger) connected on the V_{out} pin, against positive overvoltage. At powerup, with \overline{EN} pin = low, the output is rising up t_{on} soft-start after the input

overtaking undervoltage UVLO (Figure 3). The NCP391 provides a \overline{FLAG} output, which alerts the system that a fault has occurred. A t_{start} additional delay, regarding available output (Figure 3) is added between output signal rising up and to \overline{FLAG} signal rising up. \overline{FLAG} pin is an open drain output.

NCP391

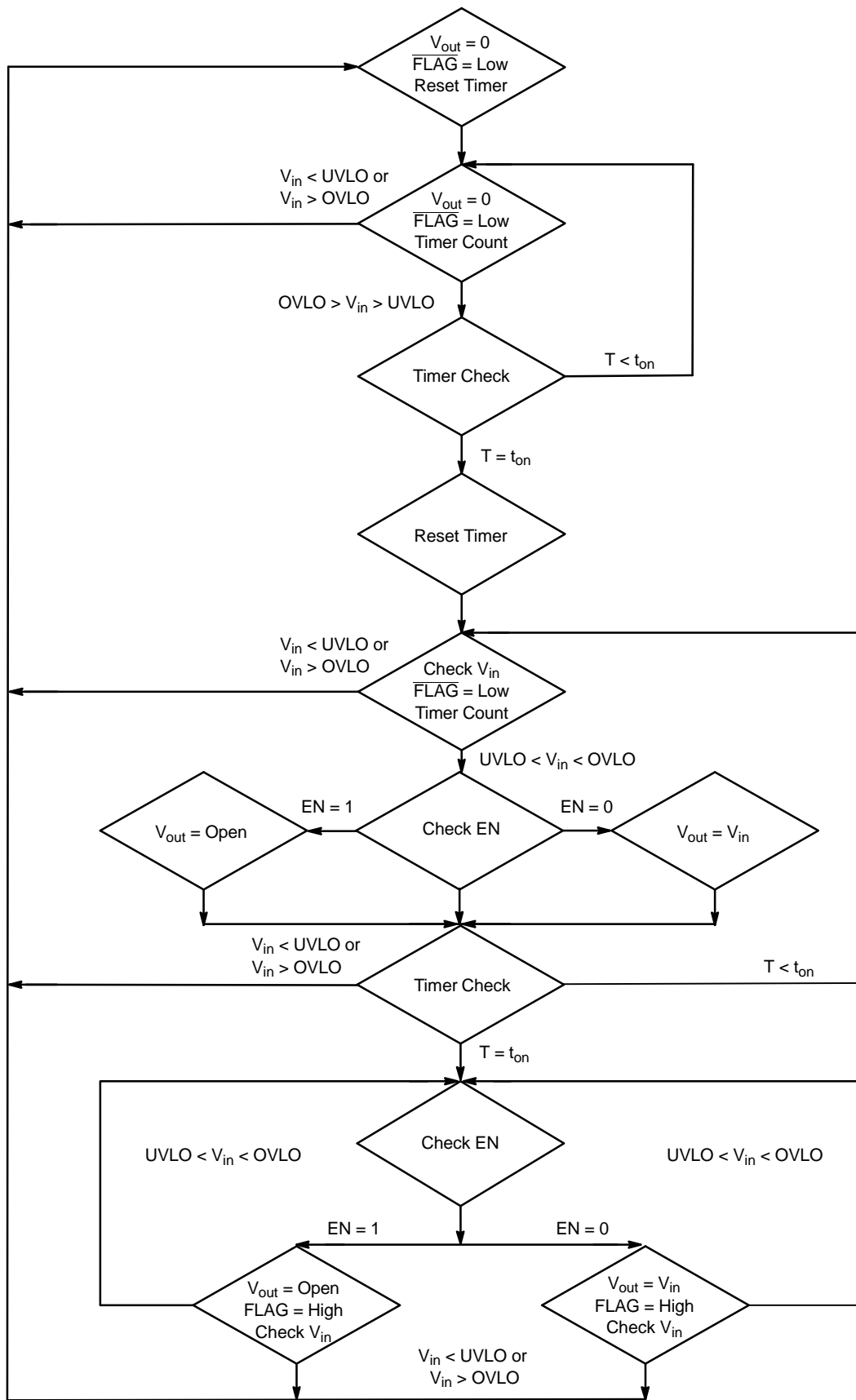


Figure 18. State Machine

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built-in undervoltage lockout (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is below UVLO, plus hysteresis, nominal. The \overline{FLAG} output is tied to low as long as V_{in} does not reach UVLO threshold. This circuit has a built-in hysteresis to provide noise immunity to transient condition. Additional UVLO thresholds ranging from UVLO can be manufactured. Contact your ON Semiconductor representative for availability.

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built-in overvoltage lockout (OVLO) circuit. During overvoltage condition, the output remains disabled as long as the input voltage exceeds typical OVLO. Additional OVLO thresholds ranging from OVLO can be manufactured. Contact your ON Semiconductor representative for availability.

\overline{FLAG} output is tied to low until V_{in} is higher than OVLO. This circuit has a built-in hysteresis to provide noise immunity to transient conditions.

\overline{FLAG} Output

The NCP391 provides a \overline{FLAG} output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon the OVLO threshold is exceeded or when the V_{in} level is below the UVLO threshold. When V_{in} level recovers normal condition, \overline{FLAG} is held high, keeping in mind that an additional t_{start} delay has been added between available output and \overline{FLAG} = high. The pin is an open drain output, thus a pull up resistor (typically 1 M Ω , minimum 10 k Ω) must be added to V_{bat} . Minimum V_{bat} supply must be 2.5 V. The \overline{FLAG} level will always reflects V_{in} status, even if the device is turned off ($\overline{EN} = 1$).

\overline{EN} Input

To enable normal operation, the \overline{EN} pin shall be forced to low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin. \overline{EN} does not overdrive an OVLO or UVLO fault.

Internal NMOSFET

The NCP391 includes an internal Low $R_{DS(on)}$ NMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the $R_{DS(on)}$, during normal operation, will create low losses on V_{out} pin.

As example: $R_{load} = 8.0 \Omega$, $V_{in} = 5.0 V$
 Typical $R_{DS(on)} = 120 m\Omega$, $I_{out} = 615 mA$
 $V_{out} = 8 \times 0.615 = 4.926 V$

$$NMOS \text{ losses} = R_{DS(on)} \times I_{out}^2 = 0.12 \times 0.615^2 = 45 \text{ mW}$$

ESD Tests

The NCP391 input pin fully supports the IEC61000-4-2. 1.0 μF (minimum) must be connected between V_{in} and GND, close to the device.

That means, in Air condition, V_{in} has a $\pm 15 \text{ kV}$ ESD protected input. In Contact condition, V_{in} has $\pm 8.0 \text{ kV}$ ESD protected input.

Please refer to Figure 19 to see the IEC 61000-4-2 electrostatic discharge waveform.

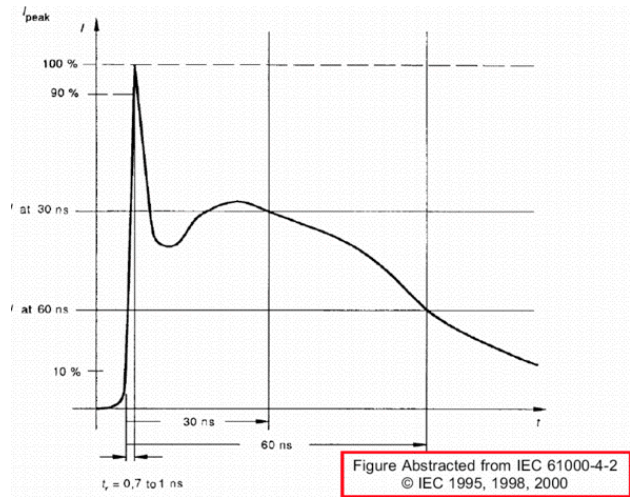


Figure 19. Electrostatic Discharge Waveform

PCB Recommendations

The NCP391 integrates a 2 A rated NMOSFET, and the PCB rules must be respected to properly evacuate the heat out of the silicon.

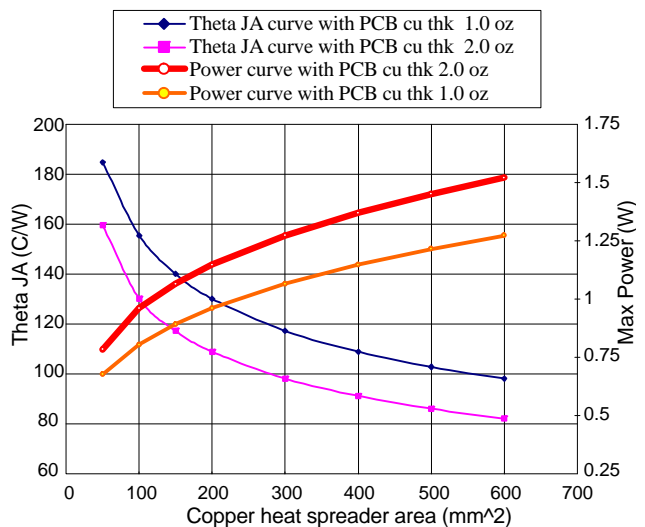


Figure 20.

NCP391

ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|----------------|---------|---------------------|--------------------|
| NCP391FCALT2G | 391L | WLCSP6 (Pb-Free) | 3000 / Tape & Reel |
| NCP391FCCADT2G | 391D | WLCSP6 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SELECTION GUIDE

The NCP391 can be available in several undervoltage and overvoltage thresholds versions. Part number is designated as follows:

NCP391FCxxT1G

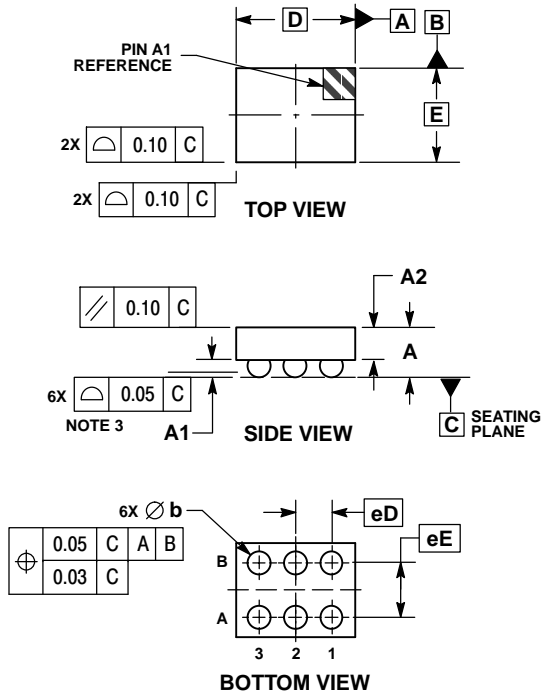
↑↑
a b

| Code | Contents |
|------|---|
| a | UVLO Typical Threshold a: A = 2.95 V |
| b | OVLO Typical Threshold b: D = 4.95 V b: L = 7.4 V |

NCP391

PACKAGE DIMENSIONS

WLCSP6, 1.31x1.04
CASE 499BP
ISSUE A

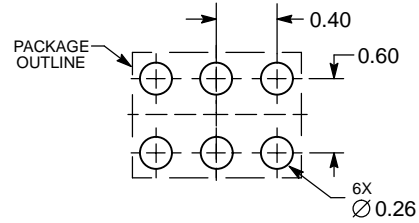


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.50 | 0.56 |
| A1 | 0.17 | 0.23 |
| A2 | 0.33 | 0.39 |
| b | 0.24 | 0.29 |
| D | 1.31 | BSC |
| E | 1.04 | BSC |
| eD | 0.40 | BSC |
| eE | 0.60 | BSC |

RECOMMENDED SOLDERING FOOTPRINT*



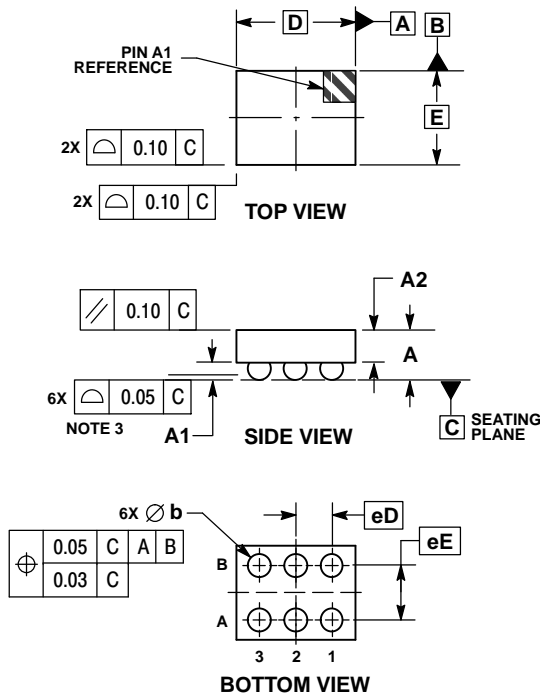
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP391

PACKAGE DIMENSIONS

WLCSP6, 1.31x1.04
CASE 567JW
ISSUE O

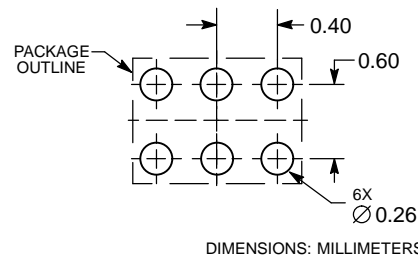


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.


| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.50 | 0.62 |
| A1 | 0.17 | 0.23 |
| A2 | 0.33 | 0.39 |
| b | 0.24 | 0.29 |
| D | 1.31 BSC | |
| E | 1.04 BSC | |
| eD | 0.40 BSC | |
| eE | 0.60 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative