Konnex Association

elmos

KNX/ EIB TRANSCEIVER **E981.03**

PRODUCTION DATA - JAN 15, 2015

RoHS compliant

Key Features

- Certified with **KNX**® TP1-256 application
- Autonomous MAC and individual physical address
- Included protocol handling
- Included power supply for bus powered applications with selectable bus current limitation

KNX® Interface

- Extended frames with up to 254 byte payload
- Analog Mode (direct RX / TX interface)
- Autonomous Telegram trigger
- Alarm Telegram
- Autonomous poll data transfer

UART host interface

- Supports 9.6 k, 19.2 k, 115.2 k
- 9 bit mode for easy data stream interpretation
- Optional CRC (at 19.2kBd and 115.2 kBd)

SPI™ host interface

- if not used 4 GPIOs are available

Included power supplies:

- 20V supply, up to 20mA
- 3.3V (70mA) / 5V (70mA) DC/DC converter

General Description

The E981.03 combines the TP1-256 physical layer, the communication controller and two DC supply outputs for bus powered applications. The internal power management assures **KNX** conformance under all load conditions.

The connection between the E981.03 and the host processor can be established by either UART or SPI compatible interfaces, or in direct Analog Mode.

Applications

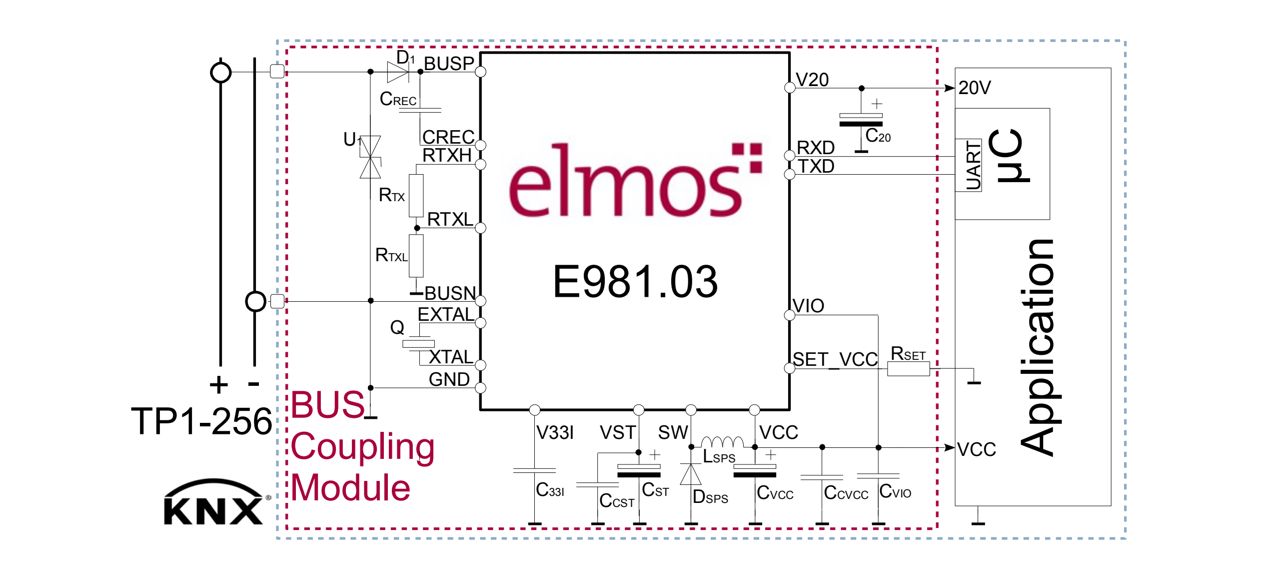
- Sensors, actuators, routers, gateways, Bus-powered or externally supplied
- Security applications

Ordering Information

Ordering-No.:	Temp Range	Package
E98103A38B	-25°C to +85°C	QFN32L7

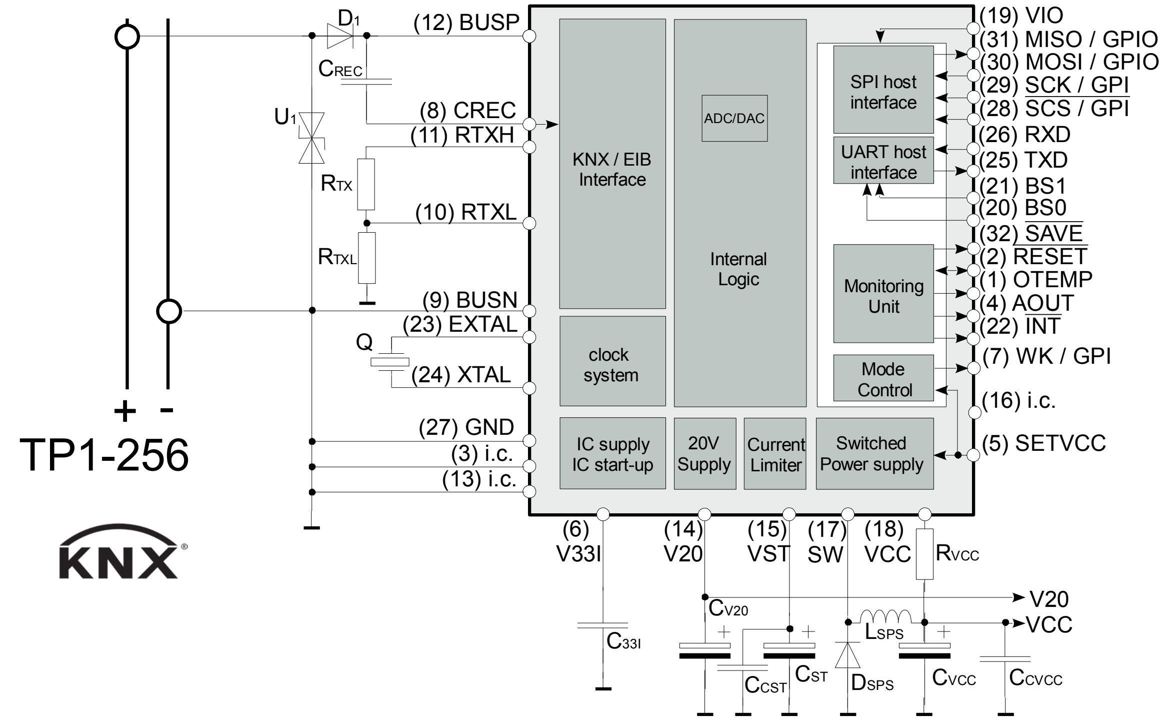
*KNX is a **Konnex Association** registered trademark.*
SPI™ is a Motorola Inc. trademark.

Typical Application Circuit

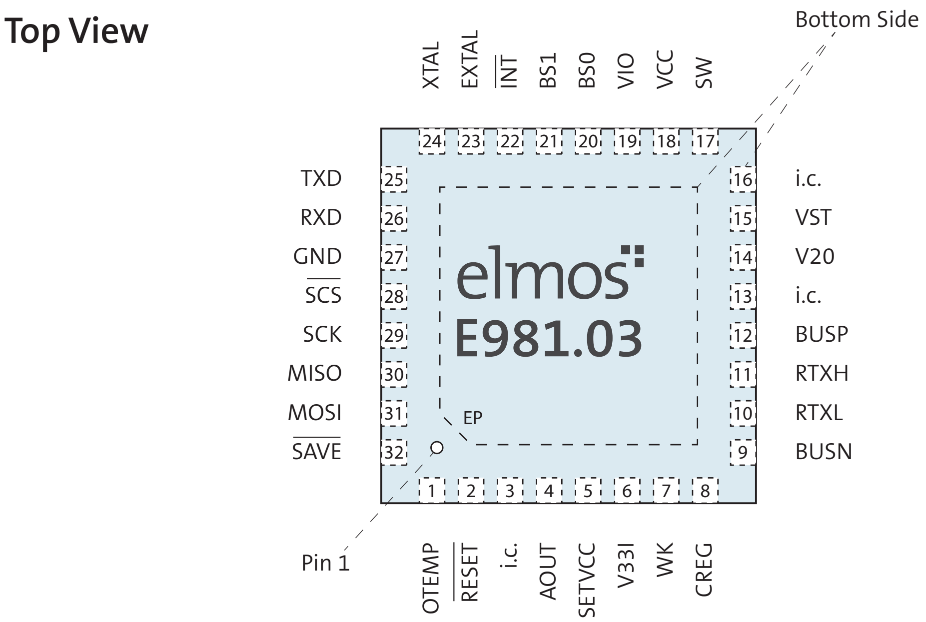


Elmos Semiconductor AG reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

Functional Diagram



Pin Configuration



Note: *Not to scale, EP Exposed die pad*

Pin Description

Pin	Name	Type 1)	Pull	Description
1	OTEMP	D_O	-	Over-temperature warning
2	$\overline{\text{RESET}}$	D_IO	Up	Bidirectional reset pin (low active)
3	i.c.	-	-	Reserved for factory use, connect to GND during operation.
4	AOUT	A_O	-	Analog multiplexer output
5	SETVCC	D_I	2)	Combination of - selection of the VCC output voltage and - alarm function activation
6	V33I	S	-	3.3V internal supply: Connect to external capacitor
7	WK	HV_D_IO	-	Output with tri-state capability; used for **KNX** telegram trigger Output [default]: VIO related output levels Input: VST tolerant. Thresholds V_{V33i} related
8	CREC	HV_A_I	-	Receive pin for **KNX** bus communication
9	BUSN	S	-	Connection to the negative bus line
10	RTXL	HV_A_IO	-	Ground connection of external resistor RTX
11	RTXH	HV_A_IO	-	**KNX** send output pin - upper connection of external resistor RTX
12	BUSP	HV_S	-	Connection to positive **KNX** bus via external diode for reverse polarity protection
13	i.c.	-	-	Reserved for factory use, connect to GND during operation.
14	V20	HV_S	-	20V DC supply output
15	VST	HV_S	-	Connection to external storage capacitor CST
16	i.c.	-	-	Do not connect externally
17	SW	HV_A_IO	-	Switched output of DC/ DC converter
18	VCC	A_I	-	DC/ DC converter output voltage control input
19	VIO	S	-	Supply for digital IO pins (connect to VCC if no external supply is used)
20	BS0	D_I	Down	Baud rate select pin 0
21	BS1	D_I	Down	Baud rate select pin 1
22	$\overline{\text{INT}}$	D_O	-	Used for **KNX** collision trigger (low active)
23	EXTAL	D_O	-	External crystal terminal 2
24	XTAL	D_I	-	External crystal terminal 1 or clock input if no crystal is connected
25	TXD	D_O	-	UART transmit signal: from E981.03 to host processor (push/pull)
26	RXD	D_I	Down	UART receive signal: from host processor to E981.03
27	GND	S	-	GND pin
28	$\overline{\text{SCS}}$	D_I	Up	SPI chip select (low active) or **G**eneral **P**urpose **I**nput if SPI is disabled
29	SCK	D_I	Down	SPI clock or GPI if SPI is disabled
30	MISO	D_IO	-	SPI master in slave out data line or GPIO if SPI is disabled
31	MOSI	D_IO	-	SPI master out slave in data line or GPIO if SPI is disabled
32	$\overline{\text{SAVE}}$	D_O	Up	VST under voltage pre alarm signal (low active)
33	EP			Exposed Die Pad

1) D = digital, A = analog, S = supply, I = input, O = output, HV = high voltage

2) Internally weak pulled to V33I/2. A open pin is the alarm condition. To select a VCC voltage push it to VIO or pull it to GND.

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Description	Symbol	Min	Max	Unit
BUSP voltage	V_{BUSP}	-0.3	55	V
BUSP voltage during surge pulse (t < 150µs)	V_{BUSP_surge}	-0.3	65	V
Junction temperature	T_J	-45	150	°C
Storage temperature	T_S	-45	150	°C
ESD immunity (human body model, this test can be applied between any two pins of the IC)	$V_{ESD,hbm}$	-2	2	kV
Voltage at digital and analog VIO pins: RESET, SAVE, XTAL, INT, SETVCC, OTEMP, $\overline{\text{SCS}}$, SCK, MOSI, MISO, RXD, TXD, BS0, BS1, AOUT	V	-0.3 V	V_{IO} + 0.3 V	
Voltage at WK pin	V_{WK}	-0.3	40	V
Voltage at VST pin	V_{VST}	-0.3	40	V
Voltage at SW pin	V_{SW}	-5 V	V_{ST} + 0.3 V	
Voltage at VCC pin	V_{VCC}	-0.3	8	V
Voltage at VIO pin	V_{VIO}	-0.3	7	V
Overall current through digital and analog VIO pins (latch up immunity): RESET, SAVE, XTAL, INT, SETVCC, OTEMP, $\overline{\text{SCS}}$, SCK, MOSI, MISO, RXD, TXD, BS0, BS1, WK, AOUT	I	-100	100	mA
Current through digital and analog VIO pins (latch up immunity): RESET, SAVE, XTAL, INT, SETVCC, OTEMP, $\overline{\text{SCS}}$, SCK, MOSI, MISO, RXD, TXD, BS0, BS1, WK	I	-70	70	mA
Voltage at pin EXTAL	V_{EXTAL}	-0.3	+3.6	V
Input voltage at CREC pin	V_{CREC}	-15 V	V_{BUSP}	
Voltage at pins RTXH, RTXL	V_{RTX}	-0.3 V	V_{BUSP}	
Current through RTXL pin	I_{RTXL}	0	800	mA
Current through AOUT pin	I_{AOUT}	-10	10	mA
Voltage at pin V33I pin	V_{V33I}	-0.3	+3.6	V
Voltage at pin V20	V_{V20}	-0.3 V	V_{ST} + 0.3 V	

2 Recommended Operation Conditions

Description	Condition	Symbol	Min	Typ	Max	Unit
Ambient temperature		T_{amb}	-25	25	85	°C
External storage capacitance [4)]		C_{ST}	270	330	1000	µF
C_{ST} equivalent series resistance		$R_{ESR,CST}$	0.1		1	Ω
C_{ST} voltage capability		V_{CST}	35			V
Parallel ceramic capacitance VST to GND		$C_{CER,ST}$	80	100	120	nF
Average bus idle voltage		V_{BUSP}	20	30	33	V
20V supply external capacitance [7)]		C_{20}	10	22		µF
C20 equivalent series resistance		$R_{ESR,C20}$	0.1		1	Ω

Description	Condition	Symbol	Min	Typ	Max	Unit
20V load current, this current is positive from the supply to the output		I_{V20} 8)	0		20	mA
V_{CC} output capacitance	L_{SPS}=330µH	$C_{VCC,L330\mu}$	10	47	$0.6 \cdot C_{ST}$	µF
V_{CC} output capacitance	L_{SPS}=1000µH	$C_{VCC,L1000\mu}$	68	100	$0.6 \cdot C_{ST}$	µF
C_{VCC} equivalent series resistance	L_{SPS}=330µH 2)	$R_{ESR,CVCC,L330\mu}$	0.2	0.5	0.8	Ω
C_{VCC} equivalent series resistance	L_{SPS}=1000µH 2)	$R_{ESR,CVCC, L1000\mu}$	1	1.25	1.5	Ω
Ceramic capacitance V_{CC} to ground		C_{CVCC}	80	100	120	nF
DC / DC converter inductance		L_{SPS}	270	330	1200	µH
L_{SPS} series resistance		$R_{L,SPS}$	1	3	10	Ω
Saturation current of L_{SPS}	3)	$I_{sat,SPS}$	160			mA
Maximum forward voltage of the external diode	I=150mA	$V_{f,DSPS}$		0.6	1	V
Reverse recovery time of the external diode		$t_{rr,DSPS}$			50	ns
V_{CC} load current in 3.3 V mode, this current is positive from the supply to the output	L_{SPS}=330µH	$I_{VCC3.3,L330\mu}$ 8)	0		50	mA
V_{CC} load current in 3.3 V mode, this current is positive from the supply to the output	L_{SPS}=1000µH	$I_{VCC3.3,L1000\mu}$ 8)	0		70	mA
V_{CC} load current in 5V mode, this current is positive from the supply to the output	L_{SPS}=330µH	$I_{VCC5,L330\mu}$ 8)	0		30	mA
V_{CC} load current in 5V mode, this current is positive from the supply to the output	L_{SPS}=1000µH	$I_{VCC5,L1000\mu}$ 8)	0		70	mA
Digital IO interface voltage 6)	$V_{IO,norm}$=5V	$V_{IO,5}$	4.75		5.25	V
Digital IO interface voltage 6)	$V_{IO,norm}$=3.3V	$V_{IO,33}$	3.15		3.45	V
Crystal frequency (+- 50 ppm)		f_O		7.3728		MHz
Synchronization clock frequency applied at pin XTAL	no crystal installed	$f_{XTAL,sync}$	126.537	126.562	126.588	Hz
Receiver decoupling capacitance		C_{CREC}	50	56	62	nF
External send resistance		R_{TX}	44.5	47	49.4	Ω
External send resistor power dissipation 1)		P_{RTX}	1			W
System level ESD protection resistance 5)		$R_{SET;}$ R_{VCC}		1		kΩ
System level ESD protection zener-diode 5)		V_{zDiode}			6.2	V
Analog monitor (AOUT - pin) current		I_{AOUT}	-50		50	µA
External send pull-down		R_{TXL}	9	10	11	kΩ

1) *For telegram rates > 50% P_{RTX} = 2 W is recommended.*
2) *The lower limit is necessary for DC/ DC control.*
*The upper limit is a result of ripple considerations: voltage ripple is ESR * current ripple of LSPS.*
To guarantee this over lifetime it is useful to use a low ESR capacitor and realize the lower limit with a series resistor.
3) *$I_{sat,SPS}$ is the DC current that causes an inductance drop of 20 %.*
4) *Smaller C_{ST} down to 47 µF can be used, however the load step capability has to be proved experimentally.*
5) *Only necessary in case of the E981.03 being connected to a separate application module.*
These components only ensuring to meet the absolute maximum rating in case of connecting and disconnecting the application module. If the connector guarantees to connect GND potential first, the ESD protection is not needed.
6) *For better elaboration of the ADC results a stable VIO is highly recommended.*
7) *High capacitance may affect the Reset / Power up Sequence time, as it is loaded with current limitation $I_{V20(max)}$.*
8) *To use the maximum current capability on VCC and V20 it is needed to change MAX_BUS_CURR settings before switching on high current consumption. Additionally a continuous under voltage condition on BUSP could reduce available current. To prevent unexpected under voltage conditions it is strongly recommended to observe VVST and implement a power management system. The voltage VVST could be observed ADC converted trough UART or SPI.*
For details read chapter 6.3 and 10.2.

3 Electrical Characteristics

(V_{BUSP} = 19V ... 33V, T_{AMB} = -25°C ... +85°C, unless otherwise noted. Positive currents are flowing into the device pins. Typical values are at T_{AMB} = +25°C, unless otherwise noted.)

Description	Condition	Symbol	Min	Typ	Max	Unit
E981.03 Modes, Sequences and Functions - DC Characteristics						
Voltage level at V33I pin for activating hard reset mode		$V_{V33I,reset,act}$	2.6			
Voltage level at V33I pin for leaving hard reset mode		$V_{V33I,reset,deact}$			3.0	
First voltage level at VST pin for switching VCC supply on		$V_{ST,VCC,on,abs}$		16		V
Second voltage level at VST pin for switching VCC supply on		$V_{VST,VCC,on,rel}$	-	$V_{BUSP,mean}$ - 6 V	-	V
Voltage level for switching **KNX** IC current from BUSP to VST		$V_{VST,V33ana}$	-	12	-	V
Voltage level for switching VST load current in soft start mode to maximum level		$V_{VST,V33dig}$		15		V
Current at BUSP during soft start		$I_{BUSP,SS}$		9	10	mA
Voltage level at VST pin for switching VCC supply off		$V_{VST,VCC,off}$		9		V
Voltage level at VCC pin for $\overline{RESET}$ deactivation (3.3 V)	V_{VCC} = 3.3 V	$V_{\overline{RESET},LH,3}$	2.8		3.05	V
Voltage level at VCC pin for $\overline{RESET}$ deactivation (5V)	V_{VCC} = 5 V	$V_{\overline{RESET},LH,5}$	4.20		4.5	V
Voltage hysteresis at VCC pin for $\overline{RESET}$ generation		$V_{\overline{RESET},VCC,hyst}$	0.095			V
Voltage level at VST pin for activation of $\overline{SAVE}$ pin		$V_{VST,\overline{SAVE},HL}$	13		15	V
Absolute V_{VST} level for deactivation of $\overline{SAVE}$ pin		$V_{VST,\overline{SAVE},LH,abs}$	14		16	V
Relative V_{VST} level for deactivation of $\overline{SAVE}$ pin		$V_{VST,\overline{SAVE},LH,rel}$		$V_{BUSP,mean}$ - 6 V		V
V_{BUSP} level for deactivation of $\overline{SAVE}$ pin		$V_{BUSP,\overline{SAVE},LH}$		18.5		V
Hysteresis of $\overline{SAVE}$ pin activation / deactivation levels		$V_{ST,\overline{SAVE},hyst}$	1			V
$\overline{SAVE}$ output voltage at logic-level low	$I_{\overline{SAVE}}$ = 5 mA V_{IO} = 5 V	$V_{\overline{SAVE},low,5}$			0.7	V
	$I_{\overline{SAVE}}$ = 2 mA	$V_{\overline{SAVE},low,2}$			0.4	V
Pull up current at pin $\overline{SAVE}$	$V_{\overline{SAVE}}$ = 0 V V_{IO} = 5 V	$I_{\overline{SAVE},pu}$		-500		µA
Absolute V_{20} supply activation threshold		$V_{V20,on,abs}$		$V_{VST,SAVE,LH}$ +1 V		
Relative V_{20} supply activation threshold		$V_{V20,on,rel}$		$V_{BUSP,mean}$ - 5 V		
Absolute V_{20} supply deactivation threshold		$V_{V20,off,abs}$		$V_{VST,SAVE,HL}$ +1 V		

Electrical Characteristics (continued)

(V_{BUSP} = 19V ... 33V, T_{AMB} = -25°C ... +85°C, unless otherwise noted. Positive currents are flowing into the device pins. Typical values are at T_{AMB} = +25°C, unless otherwise noted.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Relative V20 supply deactivation threshold		$V_{V20,off,rel}$		$V_{BUSP,mean}$ - 6 V		
High threshold at pin WK. 1)		$V_{WK,high}$	2.0		2.5	V
Low threshold at pin WK. 1)		$V_{WK,low}$	1.1		1.6	V
Pull down current at pin WK (active in input mode) 1)	$V_{WK} = V_{VIO}/2$, V_{VIO} = 5V	$I_{WK,pd}$		60		µA
High level at pin WK	I_{WK} = -2mA	$V_{WK,OUT,high2}$	V_{VIO} -1V			V
High level at pin WK	I_{WK} = -0.5mA	$V_{WK,OUT,high5}$	V_{VIO} -0.5V			V
Low level at pin WK	I_{WK} = 5mA	$V_{WK,OUT,low}$			0.7	V
E981.03 mode parameters - AC Characteristics						
Maximum duration of hard reset mode	V_{BUSP} > 20 V, C_{33I} = 100 nF	$t_{33I,on}$			20	ms
Wait time between **KNX** bus communication free and sending Reset indication to the host processor		$t_{w,ri}$	40			bit times
Duration of an active driven wake-up pulse to MCU causes by a valid trigger telegram		$t_{TRIGGER,pw}$	80	100	120	ms
Debounce time of alarm condition at pin SETVCC		$t_{ALARM,deb}$		100	120	ms
Reset Concept - DC Characteristics						
Actively driven low level on pin RESET	$I_{\overline{RESET}}$ < 5 mA, V_{VIO} > 3 V	$V_{\overline{RESET},low,out}$			0.4	V
Pull up current at pin $\overline{RESET}$ 2)	$V_{\overline{RESET}}$ = 0 V, V_{VIO} = 5 V	$I_{\overline{RESET},pu}$		-500		µA
Low level at pin $\overline{RESET}$ input path		$V_{\overline{RESET},low,in}$			0.2	V_{IO}
High level at pin $\overline{RESET}$ input path		$V_{\overline{RESET},high,in}$	0.8			V_{IO}
Minimum voltage at pin VIO for interpreting the input path of RESET 3)		$V_{IO,min,\overline{RESET}}$	2.0			V
Reset Concept - AC Characteristics						
Debounce time of input pin $\overline{RESET}$ for activation soft reset mode		$t_{RESET,deb}$	10			µs
Minimum active time of $\overline{RESET}$ 4)		$t_{RESET,min}$	10		20	ms
Power Supply – DC Characteristics						
Voltage drop between BSUP and VST PIN		V_{ST_drop}	2	2.4	3	V
Maximum DC BUSP current	MAX_BUS_CURR (0x20F) = 0xBF	$I_{BUSP(max)}$	11.4	12	12.6	mA

1) The WK pin is configurable as input or as output which sent a trigger pulse on received trigger telegram. To configure this change bit EN_OUT to "0" in Register TRIGGER (0x214). Default configuration is output.

2) The $\overline{RESET}$ pin is an open drain input/output with pull current source to V_{IO}

3) The input at pin $\overline{RESET}$ is not active in reset and startup modes and in case of low V_{IO}

4) In case of $\overline{RESET}$ activation by E981.03.

Electrical Characteristics (continued)

(V_{BUSP} = 19V ... 33V, T_{AMB} = -25°C ... +85°C, unless otherwise noted. Positive currents are flowing into the device pins. Typical values are at T_{AMB} = +25°C, unless otherwise noted.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Maximum DC BUSP current	MAX_BUS_CURR (0x20F) = 0xFF	$I_{BUSP(max)}$	17.1	18	18.9	mA
Maximum DC BUSP current	MAX_BUS_CURR (0x20F) = 0x3F	$I_{BUSP(max)}$	22.8	24	25.2	mA
Maximum DC BUSP current	MAX_BUS_CURR (0x20F) = 0x7F	$I_{BUSP(max)}$	28.5	30	31.5	mA
Maximum bus current slope in 0.25 mA/ms mode	CURRENT_SLOPE (0x210) = 0x00	slope, lim025_di/dt	0.17	0.2	0.23	mA / ms
Maximum bus current slope in 0.5 mA/ms mode (default)	(0x210) = 0x01	slope, lim05_di/dt	0.35 [1)]	0.4 [1)]	0.45 [1)]	mA / ms
Maximum bus current slope in 1.25 mA/ms mode	(0x210) = 0x02	slope, lim125_di/dt	0.87 [1)]	1 [1)]	1.13 [1)]	mA / ms
Maximum bus current slope in 2.5 mA/ms mode	(0x210) = 0x03	slope, lim25_di/dt	1.75	2	2.25	mA / ms
Output voltage at pin V20	V_{VST} > 20V, I_{V20} = 0 ... $I_{V20(max)}$ (positive output current)	V_{V20}	18.5	20	21.5	V
Voltage drop linear voltage regulator at under-voltage	V_{VST}<20V, I_{V20}=0...20mA (positive output current)	$V_{V20,DROP}$		0.5	0.8	V
Short circuit current	(positive output current)	$I_{V20(SC)}$	25		50	mA
Output voltage in 3.3V mode	$I_{LOAD,VCC}$ <= 50 mA (positive output current) SETVCC = GND	$V_{VCC3.3}$	3.15	3.3	3.45	V
Output voltage in 5V mode	$I_{LOAD,VCC}$ <= 30 mA (positive output current) SETVCC = VIO	V_{VCC5}	4.75	5	5.25	V
Voltage ripple in 3.3V mode. This ripple is already included in output voltage tolerance.	CVCC = 47µF ESR = 0.5Ω LSPS = 330µH RLSPS = 3 Ω SETVCC = GND	$V_{VCC,PP3.3}$		70		mV
Voltage ripple in 5V mode. This ripple is already included in output voltage tolerance.	CVCC = 47µF ESR = 0.5Ω LSPS = 330µH RLSPS = 3 Ω SETVCC = VIO	$V_{VVC,PP5}$		70		mV
Voltage at pin SETVCC for selection of VCC = 3.3 V and no active alarm condition		$V_{SETVCC,low}$			0.6	V
Voltage at pin SETVCC for an active alarm condition		$V_{SETVCC,alarm}$	0.4		0.6	V_{V33I}

1) guaranteed by design

Electrical Characteristics (continued)

(V_{BUSP} = 19V ... 33V, T_{AMB} = -25°C ... +85°C, unless otherwise noted. Positive currents are flowing into the device pins. Typical values are at T_{AMB} = +25°C, unless otherwise noted.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Voltage at pin SETVCC for selection of VCC = 5 V and no active alarm condition		$V_{SETVCC,high}$	0.8			V_{V33I}
Pull resistance at pin SETVCC to V33I		$R_{p33,SETVCC}$		200		kΩ
Pull resistance at pin SETVCC to GND		$R_{p0,SETVCC}$		200		kΩ
Voltage at pin V33I		V_{V33I}	3.22	3.3	3.38	V
Clock System - AC Characteristics						
Crystal frequency (±50ppm)	CLK_FAC L/H (0x20A / 0x20B) = 0xE330 (reset value)	f_Q		7.3728		MHz
Synchronization clock frequency applied at pin XTAL	no crystal installed EXTAL is n.c.	$f_{XTAL,sync}$	126.537	126.562	126.588	Hz
Host UART Interface - DC Characteristics						
Input low voltage at pin RXD		$V_{RXD,low}$			0.2	V_{IO}
Input high voltage at pin RXD		$V_{RXD,high}$	0.8			V_{IO}
Pull down current at pin RXD	V_{RXD} = 5 V, V_{IO} = 5 V	$I_{RXD,pd}$		100		µA
Low level on TXD pin	I_{TXD} = 5 mA, V_{IO} = 5	$V_{TXD,low,5}$			0.7	V
	I_{TXD} = 2 mA	$V_{TXD,low,2}$			0.4	V
High level on TXD pin	I_{TXD} = -5 mA, V_{IO} = 5	$V_{TXD,high,5}$	V_{IO}-0.7 V			
	I_{TXD} = -2 mA	$V_{TXD,high,2}$	V_{IO}-0.4 V			
Low level on pin BS0		$V_{BS0,low}$			0.2	V_{IO}
High level on pin BS0		$V_{BS0,high}$	0.8			V_{IO}
Pull down current on pin BS0	V_{IO}=5 V, V_{BS0}=5 V	$I_{PD,BS0}$		30		µA
Low level on pin BS1		$V_{BS1,low}$			0.2	V_{IO}
High level on pin BS1		$V_{BS1,high}$	0.8			V_{IO}
Pull down current on pin BS1	V_{IO}=5 V, V_{BS0}=5 V	$I_{PD,BS1}$		30		µA
Host UART Interface - AC Characteristics						
UART receiver timeout between subsequent byte of a service		$t_{UART,IBG,RX}$	2.5			ms
Baud rate deviation		Δf_{UART}	-3%		3%	
Host SP Interface - DC Characteristics						
Input high voltage at pin $\overline{SCS}$, SCK, MOSI, MISO		$V_{SPI,high}$	0.8			V_{IO}
Input low voltage at pin $\overline{SCS}$, SCK, MOSI, MISO		$V_{SPI,low}$			0.2	V_{IO}
Pull down current on pin $\overline{SCS}$	$V_{\overline{SCS}}$=5 V, V_{IO}=5 V	$I_{PU,\overline{SCS}}$		-30		µA
Pull down current on pin SCK	V_{SCK}=5 V, V_{IO}=5 V	$I_{PU,SCK}$		-30		µA
High output level on MISO, MOSI pin	I_{MISO} = -5mA, V_{IO}= 5V	$V_{MISO,high,5}$	V_{IO} -0.7V			
	I_{MISO} = -2 mA	$V_{MISO,high,2}$	V_{IO}-0.4 V			
Low output level on MISO, MOSI pin	I_{MISO} = 5mA, V_{IO}= 5V	$V_{MISO,low,5}$			0.7	V
	I_{MISO} = 2 mA	$V_{MISO,low,2}$			0.4	V

Electrical Characteristics (continued)

(V_{BUSP} = 19V ... 33V, T_{AMB} = -25°C ... +85°C, unless otherwise noted. Positive currents are flowing into the device pins. Typical values are at T_{AMB} = +25°C, unless otherwise noted.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Host SP Interface - AC Characteristics						
Time between falling $\overline{SCS}$ edge and first rising SCK edge		t_{LS1}	30			ns
Time between last falling SCK edge and rising $\overline{SCS}$ edge		t_{LS2}	30			ns
Inter byte gap - time between last falling SCK edge of a byte transmission and first rising SCK edge of subsequent byte within a SPI transfer relevant especially for read accesses between address and data bytes		t_{IBG}	1			µs
Period of SPI clock		t_{P_SCK}	250			ns
MOSI data setup time (time between MOSI data valid and falling edge of SCK		t_{setup}	30			ns
Input low voltage at pin MOSI data hold time (time between falling edge of SCK and MOSI data invalidation)		t_{hold}	20			ns
MISO data valid time (time between rising edge of SCK and MISO data valid)	C_{MISO} < 20 pF	t_{valid}			35	ns
Time between rising edge of $\overline{SCS}$ and high impedance at MISO		t_{MISO_Z}		100		ns
Monitoring Functions						
ADC scaling factor for low voltage V_{BUSP} signal used for measurement (V_{ADC} / V_{BUSP})		$Scale_{VBUSP,ADC}$	1/16.1	1/15	1/13.9	
ADC scaling factor for low voltage V_{20} signal used for measurement (V_{ADC} / V_{20})		$Scale_{V20,ADC}$	1/8.4	1/8	1/7.6	
ADC scaling factor for low voltage V_{CC} signal used for measurement (V_{ADC} / V_{CC})		$Scale_{VCC,ADC}$	1/2.14	1/2	1/1.86	
ADC scaling factor for low voltage V_{CC} signal used for measurement (V_{ADC} / V_{ST})		$Scale_{VST,ADC}$	1/10.7	1/10.05	1/9.4	
ADC scaling factor for low voltage V_{IO} signal used for ADC measurement (V_{ADC} / V_{IO})		$Scale_{VIO,ADC}$	1/2.36	1/2.2	1/2.04	
Averaging time for mean value of V_{BUSP}		$t_{VBUSP(AV)}$		5		ms
Temperature limit for activating temperature warning		$T_{warn,on}$	110	120	140	°C
Temperature limit for deactivating temperature warning		$T_{warn,off}$		$T_{warn,on}$ -10°C		°C
Temperature limit for reducing power consumption		$T_{shutoff,on}$		$T_{warn,on}$ +30°C		°C

Electrical Characteristics (continued)

(V_{BUSP} = 19V ... 33V, T_{AMB} = -25°C ... +85°C, unless otherwise noted. Positive currents are flowing into the device pins. Typical values are at T_{AMB} = +25°C, unless otherwise noted.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Temperature limit for switching on power consuming functions		$T_{shutoff,off}$		$T_{warn,on}$ +20°C		°C
High level at pin OTEMP	I_{OTEMP} = -5 mA, V_{VIO}=5V	$V_{OTEMP,high,5}$	V_{IO}-0.7V			
	I_{OTEMP} = -2 mA	$V_{OTEMP,high,2}$	V_{IO}-0.4V			
Low level at pin OTEMP	I_{OTEMP} = 5 mA, V_{VIO}=5V	$V_{OTEMP,low,5}$			0.7	V
	I_{OTEMP} = 2 mA	$V_{OTEMP,low,2}$			0.4	V
Temperature step per LSB		ΔT_{LSB}		2.5		K
Aout scaling factor for low voltage VBUSP signal used for measurement (V_{AOUT} / V_{BUSP})		$Scale_{VBUSP,AOUT,3V3}$	1/12.2	1/12	1/11.8	
Aout scaling factor for low voltage VBUSP signal used for measurement (V_{AOUT} / V_{BUSP})		$Scale_{VBUSP,AOUT,5V}$	1/8.1	1/8	1/7.9	

4 Hardware Configuration

Pins of SPI and UART interfaces, $\overline{SAVE}$, $\overline{RESET}$, WK, $\overline{INT}$ and OTEMP are prepared for galvanic insulation with optical coupler. MISO, TXD, $\overline{SAVE}$, $\overline{RESET}$, WK, $\overline{INT}$ and OTEMP can provide a current of 5 mA for driving a diode of an optical coupler in case of VIO = 5 V.
For lower power consumption set VIO_SW bit in PS_CTRL register.

4.1 PCB Design Rules

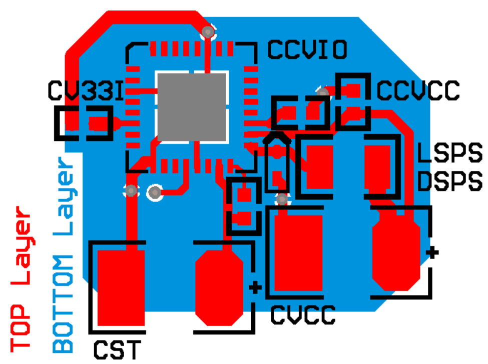


Figure 1. PCB Layout

Remark! The layout example is incomplete! The layout only gives an example about the placement of the DC/DC converter components, the external capacitors and GND routing.

4.2 Minimal Function of E981.03

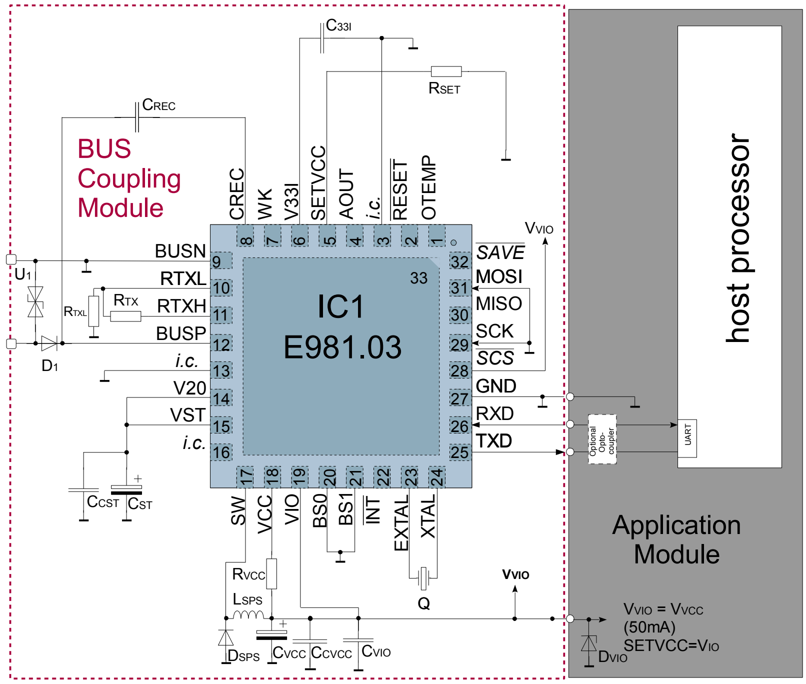


Figure 2. Schematic Example (minimal application)

DC/ DC converter active (3.3 V):	I_{max}=50 mA	OTEMP not used:	open
SETVCC = GND:	VCC = 3.3 V	WK not used:	open
BS1 = BS0 = GND:	UART 19.2 k baud	SAVE not used:	open
V20 not used:	V20 = VST	RESET not used:	open
UART optional with optical coupler		AOUT not used:	open
SPI not used	MOSI = GND		
	MISO = open		
	SCK = GND		
	SCS = VIO		

4.3 Full Normal Mode Application

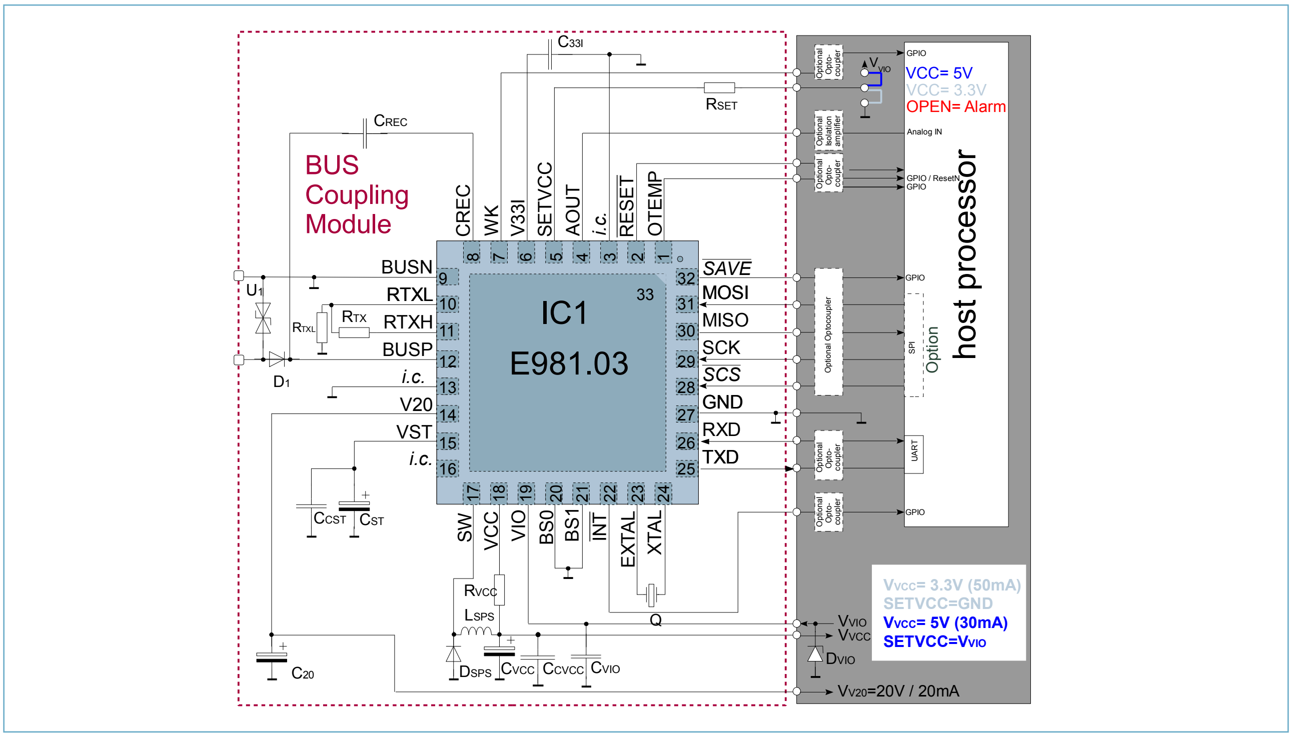


Figure 3. Schematic Example (full application)

DC/DC converter active (3.3 V/5 V):	I_{max} = 50/ 30 mA	OTEMP used	optional with optocoupler
SETVCC = GND:	VCC = 3 V	WK used	optional with optocoupler
SETVCC = VIO:	VCC = 5 V	$\overline{\text{SAVE}}$ used	optional with optocoupler
BS1 = BS0 = GND:	UART 19.2 k baud	$\overline{\text{RESET}}$ used	optional with optocoupler
V20 used:	additional C_{V20}, I_{max} = 20 mA	AOUT used	optional with insulation amplifier for analog Signal

UART optional with optical coupler
SPI optional with optical coupler

In Normal Mode alarm functionality is usable. Alarm is detected in case of an open SETVCC pin.

For other schematics read application notes.

Table 1. Recommended Components

Component	Recommended value	Remarks
U1	model: SMAJ43CA, SMBJ43CA	
D1	model: BYG21	
C_{ST}	330 µF / 35 V	ESR < 1 Ω
C_{CST}	ceramic 100 nF / 35 V	±20%
C_{20}	22 µF / 35 V	ESR < 1 Ohm
L_{SPS}	330 µH, R_{LSPS},typ = 3 Ω,$R_{LSPS,max}$ = 10 Ω, $I_{sat,SPS}$ = 160 mA, T_{amb} < 85 °C	±20%
C_{VCC}	47 µF / 6 V	0.2 Ω < ESR < 0.8 Ω
C_{CVCC}	ceramic 100 nF / 8V	±20%
C_{CVIO}	ceramic 100 nF / 8V	±20%
D_{SPS}	40 V, 200 mA, t_{rr} < 15 ns	e.g. BAT64
C_{33I}	ceramic 100 nF	±20%
R_{TX}	47 Ω	±5 % / 1 W
C_{REC}	Ceramic 56 nF	±10 %
Q	f = 7.3728 MHz, tolerance 50 ppm	Do not use external capacitors or crystals with internal capacitors.
R_{SET} 1)	1 kΩ	
R_{VCC} 1)	1 kΩ	
D_{VIO} 1)	6.2 V, 500 mW	
R_{TXL}	10 kΩ	±1%

1) Only necessary in case of the E981.03 being connected to a separate application module. These components only ensuring to meet the absolute maximum rating in case of connecting and disconnecting the application module. If the connector guarantees to connect GND potential first, the ESD protection is not needed.

5 Interfaces Description

5.1 KNX/ EIB – Interface

The **KNX**/ EIB - Interface is a full compatible **KNX** TP1 transceiver with autonomous Medium Access Control and individual physical Address. The telegram on **KNX** bus is analyzed and dependent on its contents and communication mode, the data will be processed.
In Analog Mode, the signals SEND and REC are directly bypassed to the host UART interface pins RXD and TXD.

5.2 UART – Interface

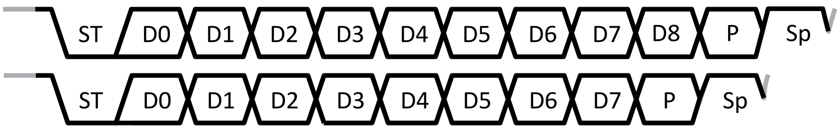
The E981.03 has a full duplex UART interface to transmit and receive bytes asynchronously. The protocol between E981.03 and host controller is a two-wire protocol with software handshake.

The UART host interface consists of the following three parts
- UART physical layer realizes media access and bit decoding / encoding or output driver for **KNX** bypass in Analog Mode
- UART logical layer provides byte framing capabilities
- UART service layer defines control and data access sequences

To secure UART communication, a CRC calculation for receive and transmit path can be activated separately.

Table 2. Baud rate configuration

BS1	BS0	Description	CRC check useable	Remark
GND	VIO	9.6 k baud	No	8 bit, even parity, 1 stop-bit
GND	GND	19.2 k baud	Yes	8 bit, even parity, 1 stop-bit
VIO	GND	115.2 k baud	Yes	9 bit, even parity, 1 stop-bit
VIO	VIO	Analog Mode	No	



$104\mu s \bullet 11Bit = 1{,}042ms$ 9.600 Baud
$52\mu s \bullet 11Bit = 0{,}521ms$ 19.200 Baud
$8{,}7\mu s \bullet 12Bit = 0{,}104ms$ 115.200 Baud

ST	Start Bit	Low
D0..D8	Data Bits	LSB first
P	Parity Bit	even
Sp	Stop Bit	High

Figure 4. UART Bit

The bit D8 in 9-bit UART has the following meaning:
0: data byte
1: service byte

5.3 SPI compatible – Interface

E981.03 has a slave SPI compatible - interface to transmit and receive data. The interface can be used alternatively for E981.03 configuration and **KNX** communication. In analog mode the interface is the only possibility to configure parameters like bus current.
To secure SPI compatible communication, a CRC calculation can also be activated.

The user could switch off the SPI compatible - Interface by setting ON0 and ON1 to zero (Register SPI_CTRL). In this case 4 GPIOS could be used trough the UART – Interface. The GPIOs have VIO related I/O levels.
The pins MOSI and MISO are useable as general purpose inputs or outputs. The pins SCS and SCK can be used as input pins. For read and write

5.4 Telegram Transmission

After successful upload of the frame E981.03 sends the frame on **KNX** bus after the **KNX** specified bus idle time detected.
The repeat flag of the frame transmitted is handled by the E981.03.

- In first transmission the repeat flag is set to 1.
- In repeated frames the repeat bit is cleared to 0.

The acknowledge frame sent by the receivers of the frame is checked and

- In case of BUSY acknowledged frames E981.03 waits for at least 150 bit times after the BUSY acknowledge before starting a new transmission attempt. These 150 bit times refer to the end of the BUSY acknowledged frame independent from other communication on the EIB bus. In case of bus communication between the two (BUSY) repetitions the time between the interposed frame and the BUSY repetition is 50 bit times.
- In case of NACK acknowledged frames E981.03 starts a new transmission attempt.
- No acknowledge and corrupted acknowledge will be handled as NACK.
- BUSY and NACK acknowledge will be handled as BUSY.

If the repeat flag in the uploaded frame is not set, E981.03 will send the frame only once even in case of not ACK acknowledgment.
The maximum number of repetitions is defined in the register MAX_RST_CNT and can be modified e.g. by a host UART service or SPI.

Table 3. **KNX** frame timing

Description	Condition	Symbol	Min	Typ	Max	Unit
Time between end of telegram upload from host processor to E981.03 and start of telegram transmission on EIB bus (in case of idle EIB bus)	bit TXDEL of register UART_CTRL = 0 L_Data or L_PollData frame	$t_{tr,delay,var}$			104	µs
Time between end of telegram upload from host processor to E981.03 and start of telegram transmission on EIB bus (in case of idle EIB bus)	bit TXDEL of register UART_CTRL = 0 L_ExtData frame				250	µs
Wait time after BUSY acknowledge		$t_{BUSY,rep}$		104		µs

5.5 AOUT

The pin AOUT is used to monitor several voltages. The source can be selected by a register value. The analog monitor signal is not filtered by the E981.03. Especially the scaled analog bus voltage is not the mean value of the bus voltage but follows the BUSP line immediately.

Between AOUT buffer and AOUT pin a series resistor of approximately 10 k is implemented in E981.03. It can be used to realize a first order RC filter by connecting AOUT to an external capacitor C_{ext}. Measurement of AOUT voltage needs to take the intern resistor value into account (high impedance measurement input use).
Measurement values are:

- Temperature voltage
- Band gap voltage [1)]
- Bus voltage

VIO = 3.3 V	VBUS / 12
VIO = 5 V	VBUS / 8

other multiplexer configuration are invalid
1) The band gap voltage can be used to increase the precision of the ADC.

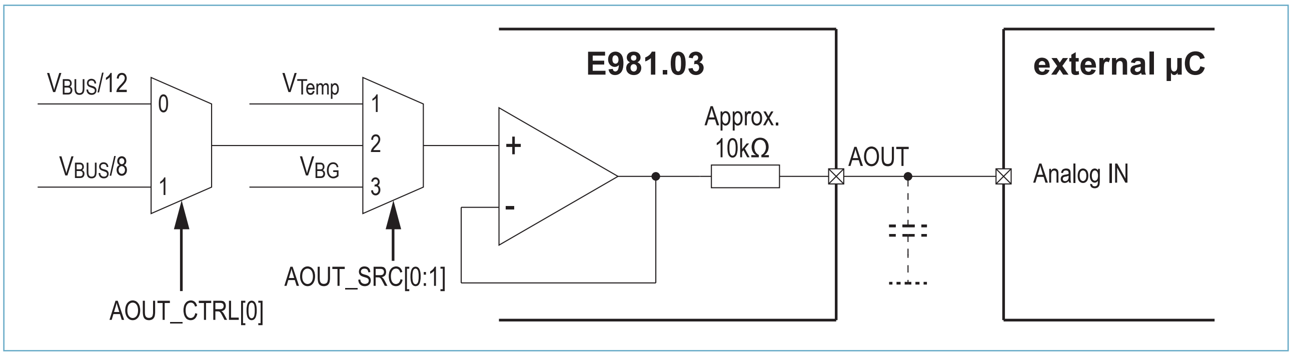


Figure 5. Analog Monitoring

AOUT is controlled by Register AOUT_CTRL and Register AOUT_SRC.

5.6 WK

The WK pin is configurable as output for remote wake-up with trigger telegram or as general purpose input. To configure as a input change bit EN_OUT to “0” in Register TRIGGER (0x214). Default configuration is output. To read input state read bit WK in the Register PINS.

5.7 E981.03 System Functions

5.8 Power Supply

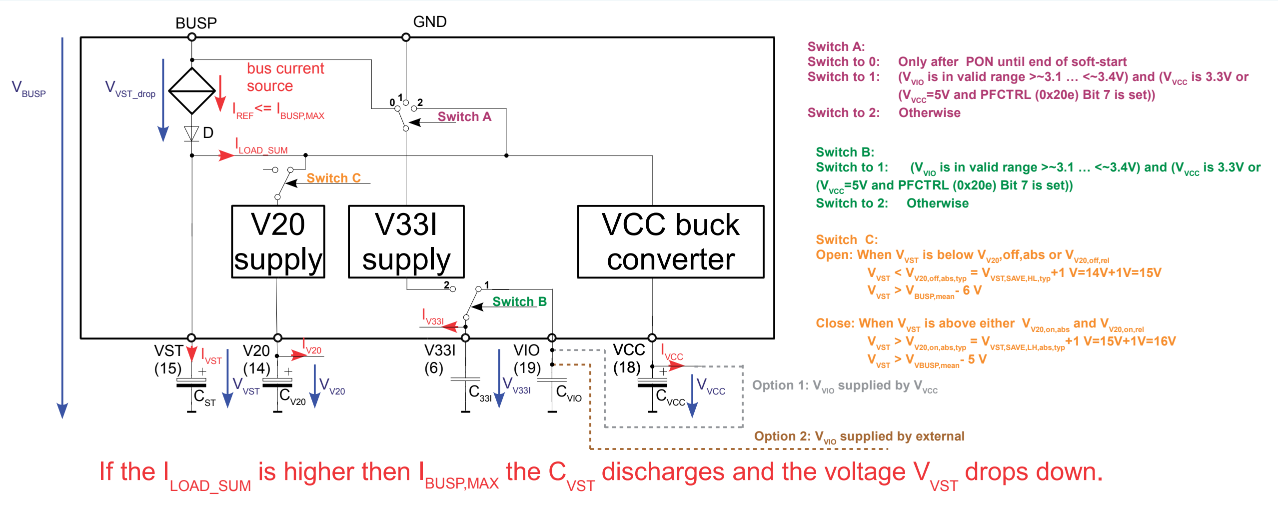


Figure 6. Configurable Power Management

The supply blocks generates a 20V application voltage V_{V20}, a variable storage voltage VST, a configurable 5V/3.3V output voltage V_{VCC} and a 3.3V voltage V_{V33I} used by internal components of the E981.03. The voltages V_{V20} and V_{VCC} can be used to supply external components. The voltages V_{V33I} is externally blocked but the strictly recommendation is not use this pin for other supplies!
The voltage V_{VST} is externally blocked. Usage of this voltage for external supplies is not recommended because it disturb the autonomous power management of the IC!

To prevent a overload and a fast load slope on the bus the power management of the IC generates a variable storage voltage V_{VST}. This voltage has a limited input current I_{REF} and a limited slope of I_{REF}. The maximum current I_{REF} and the maximum slope are configurable through SPI or UART – Service. The value of V_{VST} in normal operation without an overload condition is $V_{BUSP} - V_{VST\_DROP}$. The power which is continuously useable is $(V_{BUSP} - V_{VST\_DROP}) * I_{REF}$. If more power is used the C_{ST} is discharging, V_{VST} drops below $V_{BUSP} - V_{VST\_DROP}$.
To prevent a unpredictable crash the supplies have the following prioritization:

3rd : V20
Is generated by a linear voltage regulator out of the V_{ST}. It is the supply for additional circuits and has the lowest priority. V20 is the first one drops down, to prevent a dropping down of VCC with the consequence of a microcontroller reset. If a continuous overload is applied a pulsing V20 is possible.

2nd : VCC
Is generated by a step down DC/DC converter and could supply a microcontroller with its peripheral. The output voltage is selectable 5V or 3.3V. The supply could deliver up to 30mA at 5V and 50mA at 3.3V. Before it drops down V20 is switched of. If a continues overload condition is active V_{VST} drops below $V_{VST,SAVE,HL}$ and the SAFE signal flags a overload condition before VCC drops down.

1st : V33I
Supplies the IC and is the last one which drops down.

Please refer the Application Note for more details.

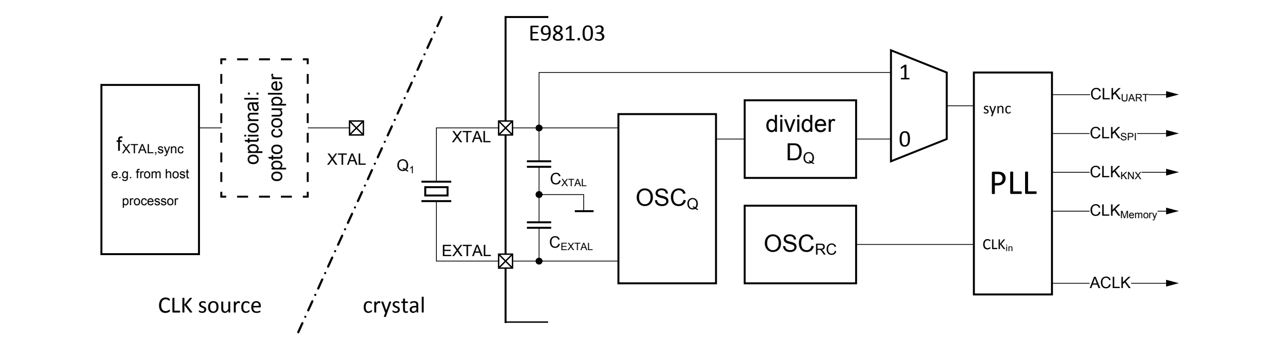


Figure 7. Clock Generation

5.9 Clock System

The main clock is generated by an internal RC oscillator. An external clock reference / crystal can be used to achieve a system clock accuracy of approx 0.05%.

Two different synchronization clocks are useable:

1) Crystal at f_Q = 7.3728 MHz
- default configuration
- foot point capacitors are incl

2) Clock reference at $f_{XTAL,sync}$ = 126.562 Hz
- the crystal oscillator should be switched off
  - EXT_Q to 1 in CLK_CTRL Register

The sync - signal source could be a crystal oscillator (OSCQ) or an external VIO related digital clock on XTAL(remark: absolute maximum rating “V”). The IC automatically detects the used mode and selects the correct internal signal path.

In Analog Mode no crystal and no external clock are required. To increase the robustness to EMI the input XTAL shall be connected to GND if not used.

6 Mode Depending Device Functions

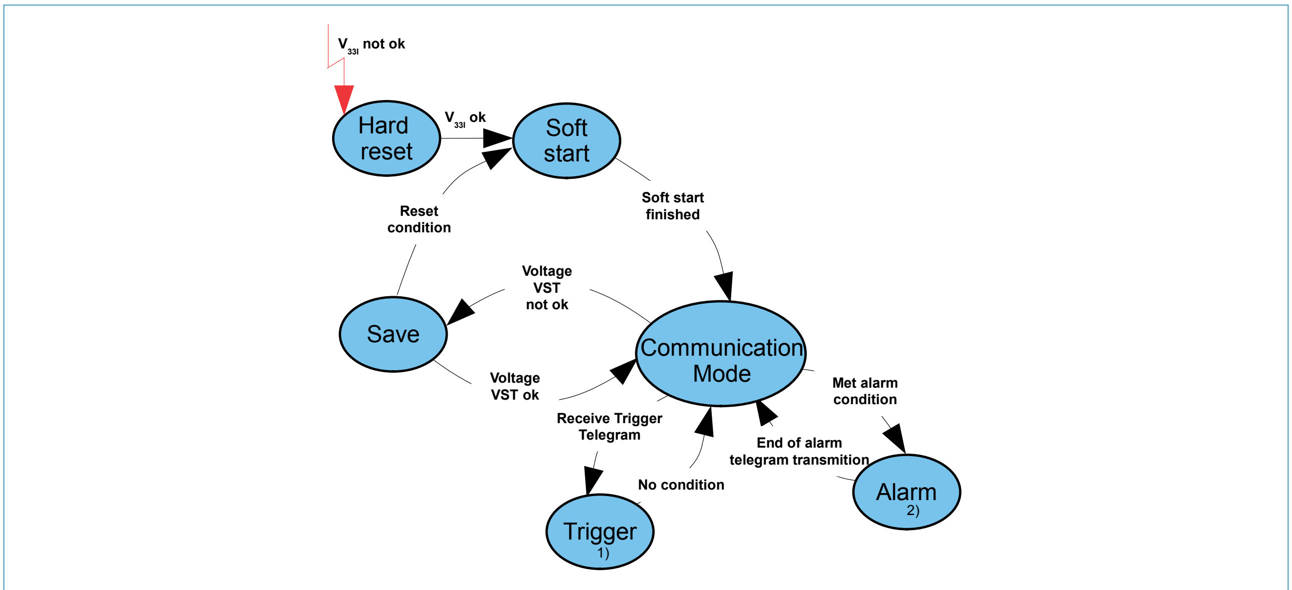


Figure 8. Device Modes

1) Trigger mode only available from Normal Mode

2) Alarm mode not available in Analog Mode see chapter 6.5 Analog Mode

6.1 Reset / Power Up-&Down Sequence

6.2 Overall

To ensure a stable function under all conditions the E981.03 supports several power up and power down scenarios. The status of the configurable supply management/ monitoring can be queried via UART and digital SAVE pin at any time.

Properties

Power Up Sequence

- Hard Reset Mode — V33I not ok
- Start Up Mode — external supply voltage switch on dependent on capacitance the Power Up Sequence stays longer in this mode
- Soft Reset — E981.03 will be set to soft reset value.

Power Down Sequence

- Save Mode — $\overline{SAVE}$ pin is active (low)
- Internal Reset — Hard Reset Mode

6.3 Undervoltage Condition

With falling bus voltage (data point 1) VST falls, too.

When V_{VST} is below either $V_{V20,off,abs}$ or $V_{V20,off,rel}$ (whichever is higher) V20 is switched off (data point 2). V_{VST} will rise in typical case of high V20 load resulting in pulsed activation of V20.

When V_{VST} falls below $V_{VST,save,HL}$ the $\overline{SAVE}$ signal is activated to initiate the save routines of host processor (data point 3). The DC/DC converter continues its normal operation until V_{VST} falls below the minimum converter input voltage V_{VCC} switch off and the V_{V33I} input (or output compare Figure 6 Configurable Power Management) make a switchover to V_{VST} without a fail time (data point 4). To avoid bus overload soft start phase with bus current reduction is activated in case of active $\overline{SAVE}$.
The $\overline{RESET}$ signal is activated when V_{VCC} falls below the threshold $V_{\overline{RESET},HL}$ (short after data point 4). If the BUSP recovers now (data point 5) the IC come back without internal reset. $\overline{SAVE}$ will be deactivated, when V_{VST} achieves the value $V_{VST,save,LH}$ (data point 6). V_{VCC} will be activated, when V_{VST} achieves the value $V_{VST,VCCon}$ (data point 7). The IC is back on regular condition after V_{VST} achieves V_{BUSP} - V_{VST_drop} (data point 8). With the returning V_{VCC} the V_{33I} output (compare Figure 6 Configurable Power Management) make a switchover to V_{VCC} if V_{VCC} is in a valid range for 3.3V otherwise the Input of the internal V_{33I} regulator switch to V_{VST} and the output of V_{33I} regulator switch to V_{V33I} output. And finally V20 recovers.
The 2nd case with data point 10 to 14 is like the case before, but now the V_{VST} drop deeper and finally E981.03 will be reset when V_{33I} is lower than V_{33I}, reset, act (data point 14).

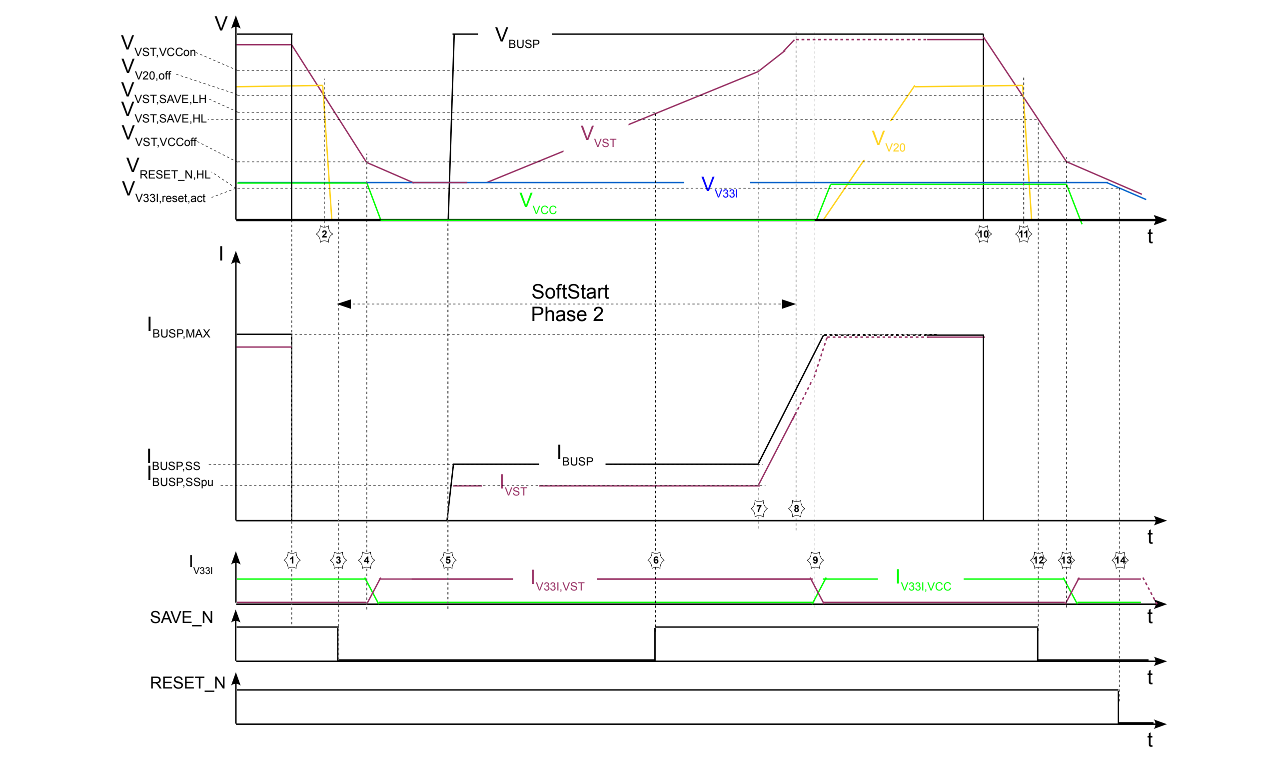


Figure 9. Undervoltage Condition

6.4 Communication Mode

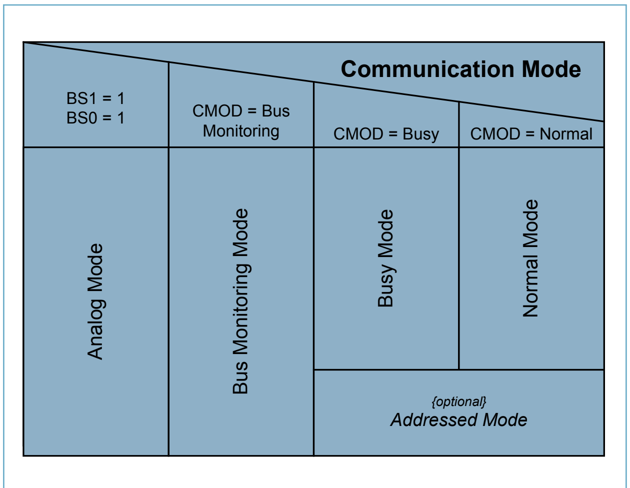


Figure 10. E981.03 Communication Mode

In figure 10 the four communication sub modes are shown. The mode controlling registers can be modified through UART or SPI commands.
For mode controlling registers see registers "DEVMODE" und "CMODE".

Mode	Prioritization
Hard reset	1
Start-up	2
Soft reset	3
Analog	4
Normal	5
Bus monitor	5
Busy	4

The Prioritization is higher with a lower value.

6.5 Analog Mode

Activation

Analog Mode is activated if

- no higher prioritize mode is active (e.g. reset, starup) and the baud rate select pins BS0 and BS1 have both high level

Deactivation

Analog Mode will be left for

- a higher prior mode (e.g. reset) if the activation condition for that modes holds or
- Normal Mode if any of the baud rate select pins has low level

Properties

- IC is fully functional (all supplies active)
- host UART interface is switched off.
  No UART service is available
- bypass from **KNX** transceiver to UART transceiver is active
- host SPI interface is active (may be switched off by host processor)

comparable to 'Medium Attachment Unit (MAU)'
***KNX** standard: Volume 3 System Specifications: Physical Layer General*

6.6 Monitoring Mode

Activation

Monitor mode can be activated if

- no higher prioritize mode is active (e.g. reset, startup, busy) and
- the CMODE register has the Bus monitor mode value

The CMODE register can be modified by

- sending a U_ActivateBusmon service request via UART or
- writing to the CMODE register via SPI or UART

Deactivation

Bus monitor mode can be left for any higher prioritize mode (e.g. reset) if the activation condition for that modes holds.
Switching to Busy Mode is not possible in Bus monitor mode.

Properties

- The data link layer of the UART is in bus monitor mode. Only the local L_Busmon service is available for the host processor. All L_Data host to E981.03 services including L_Poll_Data service are not available and will be ignored.
- Each byte received on the **KNX** / EIB is sent to the host as well as illegal control bytes and all acknowledge frames.
- E981.03 is quiet (not sending) on the **KNX** bus.
- Writing to the telegram buffers in Bus Monitoring Mode is possible.
- The transmit frame buffer content will not be transmitted to the **KNX** bus in Bus Monitoring Mode.
- U_Reset.request clears the transmit buffer ready flag (Flag READY in Register KNX_TR_BUF_STAT). Leaving Bus Monitoring Mode without clearing this flag results in transmission of the transmit buffer content on **KNX** bus.
- Alarm telegrams can be transmitted even in Bus Monitor Mode.

All received telegrams are sent byte-wise from E981.03 to the host.

Switching to Busy Mode is not allowed in Bus Monitoring Mode. Bus Monitoring Mode will be deactivated on activation of Busy Mode.

It is recommended to activate and deactivate Bus Monitoring Mode using UART service requests. Activation using direct register access will be described in an application note.

6.7 Busy Mode

If the host controller is temporarily not able to receive telegrams from the bus (e.g. due to no code execution during flash erase), the Busy Mode can be estimated to reject frames from the bus with BUSY acknowledges independently from host acknowledge information in **KNX** Busy Mode.

Activation
Busy Mode can be activated if

- no higher prior mode is active (e.g. reset, startup) and
- the CMODE register has the Busy Mode value

Busy Mode activation during active Busy Mode is ignored. The Busy Mode duration is not prolongated.

Busy Mode activation in active Bus monitor mode is not supported.

The CMODE register can be modified by

- sending a U_ActivateBusyMode service request via UART or
- writing to the CMODE register via SPI or UART

Deactivation
Busy Mode can be left for

- any higher prior mode (e.g. reset) if the activation condition for that modes holds or
- another CMODE controlled mode in case of CMODE value change
- the CMODE register can be modified by
  - sending an U_Ackinfo or an U_ResetBusyMode service request via UART or
  - writing to the CMODE register via SPI or UART or
  - internal logic when reaching timeout defined by register BUSY_REG
  - after timeout of defined in Register BUSY_REG.

Properties

- the IC is in full function (all supplies may be switched on)
- **KNX**/ EIB, UART and SPI interfaces are active (dependent on their control register contents)

but E981.03 rejects following telegrams from the bus with BUSY acknowledges

1) individually addressed telegrams with their destination address matching the individual address stored in the registers (Addressed Mode only)

2) all group telegrams including broadcast

All other frames will not be acknowledged with BUSY. All received telegrams are sent byte-wise from E981.03 to the host.

Remark
Busy Mode activation in active Bus Monitoring Mode is not supported. The IC would switch from Bus Monitoring Mode to Busy Mode but BUSY acknowledging will be delayed.

6.8 Normal Mode

Activation
The Normal Mode is active if

- no higher prioritized mode is active (e.g. reset, start-up) and
- the CMOD register has the Normal Mode value

Deactivation
The Normal Mode will be left for

- any higher prior mode (e.g. reset) if the activation condition for that modes holds or
- another CMOD controlled mode in case of CMOD value change

Properties

- the IC is in full function (all supplies may be switched on)
- **KNX**/ EIB, UART and SPI compatible interfaces are active (dependent on their control register contents)
- UART is in normal (full) mode as long as UART is not switched off by SPI access
- all UART services are available

All received telegrams are sent byte-wise from E981.03 to the host.

6.9 Addressed Mode

Each **KNX** / EIB device has it's own unique individual address in a network. The E981.03 can be configured with an individual node (physical) address. In this mode, the processor load will be reduced by the autonomous **KNX** protocol handling.

Activation

- after a complete address upload
- activated VALID bit in KNX_ADR_STAT register

Deactivation

- Reset / Power up Sequence
- deactivated VALID bit in KNX_ADR_STAT register

Properties

- incoming Frames will be analyzed
- frames with a physical address will be answered with an acknowledge automatically, if the stored address matched
- all frames with a group address will be answered automatically with an acknowledge.
- the host can suppress an automatic acknowledge generation

6.10 Trigger Functionality

Activation

- after upload of a trigger frame to E981.03 and upload of a trigger telegram mask to E981.03
- entering busy or Normal Mode.

Deactivation

- deactivated BUF bit in TRIGGER register.

Properties

WK pin is a tristate pin (tristate push pull) the E981.03 forces in Reset / Power up sequence WK to ground level.

E981.03 applies high level at pin WK after either

- a trigger telegram was received correctly or
- a broadcast telegram was received or
- an individually addressed telegram was received with address equals node address (optional if configured)
- the generated trigger pulse has a length of $t_{TRIGGER,pw.}$

The received telegram can be read from telegram receive buffer until the next telegram arrives on the **KNX**/ EIB bus. Thus the host processor can get information about trigger telegram contents after restarting the node.

Attention: To be able to get the trigger message in all conditions use the communication interface UART with 115.2KBd or SPI.
Trigger Function is not available in Bus Monitoring Mode and Analog Mode.

6.11 Alarm Functionality

During any Communication Mode (but not in Analog Mode) an alarm sequence can be used to signal improper node state to the system via **KNX** / EIB bus by sending an alarm telegram.

Activation

- after a complete alarm telegram upload and alarm condition (SETVCC pin open or forced to $V_{V33I}/2 = V_{VSETVCC,ALARM}$) is pending

Deactivation

- deactivated BUF bit in ALARM_STAT register

Properties

- an alarm telegram is send on **KNX** bus
- active $\overline{\text{RESET}}$ will be delay transmission, both alarm telegram buffer and alarm state register are not changed

The **KNX**/ EIB to UART receive path remains active during alarm sequence.

6.12 Save Mode

To enlarge the V_{VCC} operation time during low bus voltage supply the E981.03 switches some power devices off.

Properties

- **KNX**/ EIB transmitter is switched off
- The SAVE pin is active low
- **KNX**/ EIB receiver, UART host and SPI host interfaces remain active
- V20 is switched off to allow longer VCC active times

7 Data Communication

The general communication between E981.03 and host is realized by using UART services. Furthermore the IC can be configured via SPI interface.

7.1 UART-Service Host -> UART

Any service sent from host to E981.03 consists of one or more bytes. The first byte is the UART control field which identifies the type of the requested service. The E981.03 can handle the following service requests:

Table 4. UART Service - Host to E981.03

Service Name	UART control field		Remarks / Description	followed by n bytes
	Hex	Bin		7 | 6 | 5 | 4 | 3 | 2 | 1 | 0
U_Reset.request	0x01	0000 0001	After receiving a U_Reset. request the IC transits to its soft reset state.	
U_State.request	0x02	0000 0010	The IC answers an U_State. request service by sending its communication state using State.response service.	
U_ActivateBusmon	0x05	0000 0101		
U_AckInformation	0x10 ... 0x17	0001 0nba	n: NACK b: BUSY a: ADDRESSED 0: inactive 1: active	
U_ProductID.request	0x20	0010 0000		
U_ActivateBusyMode	0x21	0010 0001	The service activates the **KNX** Busy Mode in the E981.03	
U_ResetBusyMode	0x22	0010 0010	The host shall synchronize its receiver before sending the U_ResetBusyMode.	
U_MxRstCnt	0x24	0010 0100	number of busy and nack counts (in one byte) - 0..7 times	B2 | B1 | B0 | 0 | 0 | N2 | N1 | N0 Busy | 0 | 0 | Nack **KNX** control field
U_ActivateCRC	0x25	0010 0101	Only with baud rates 19.200 or 115.200	

Service Name	UART control field Hex	UART control field Bin	Remarks / Description	followed by n bytes (7 6 5 4 3 2 1 0)
U_SetAddress	0x28	0010 1000	Set **KNX** physical address - individual **KNX** address (high byte) - individual **KNX** address (low byte)	A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
U_SetAlarmTelegramm	0x29	0010 1001	**KNX** control field which is sent in alarm condition	F1 F0 R 1 P1 P2 0 0 (F1 F0: frame format; R: Re-peat flag; P1 P2: priority) **KNX** control field
U_SetTriggerTelegram	0x2A	0010 1010	**KNX** control field which is reason for a event detec-tion	F1 F0 R 1 P1 P2 0 0 **KNX** control field
U_SetTriggerTelegramMask	0x2B	0010 1011	**KNX** control field mask make it possible to detect a event with several combi-nations	M7 M6 M5 M4 M3 M2 M1 M0
U_ReadReg.request	0x2E	0010 1110	read access to the E981.03 internal memories - address (high byte) - address (low byte)	0 0 0 0 0 0 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
U_WriteReg	0x2F	0010 1111	write access to the E981.03 internal memories - address (high byte) - address (low byte) - data byte	0 0 0 0 0 0 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D7 D6 D5 D4 D3 D2 D1 D0
U_L_DataStart	0x80	1000 0000	Begin data telegram up-load with **KNX** control field	F1 F0 R 1 P1 P0 0 0 **KNX** control field
U_L_DataContinue	0x81 ... 0xBE	10xx xxxx	Upload data byte with in-dex x x: index (1 ... 62)	D7 D6 D5 D4 D3 D2 D1 D0
U_L_DataEnd	0x47 ... 0x7F	01xx xxxx	Upload check sum with last index x+1 x: last index+1 (7 ... 63)	C7 C6 C5 C4 C3 C2 C1 C0 It is calculated as logical NOT XOR function over the individual bits of the preceding bytes of the frame.
U_PollingState	0xE0 ... 0xEF	1110 xxxx	Upload polling state in to the expecting slot x x: slot number (0 ... 14) - PollAddrHigh - PollAddrLow - State	A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 S7 S6 S5 S4 S3 S2 S1 S0
U_L_LongDataContinue	0xC0 0xC1	1100 000x	Upload data byte with in-dex x(bit 8 .. 0) (1 ... 263) x: MSB (bit 8) of index - index x(bit 7 ... 0) - data byte	I7 I6 I5 I4 I3 I2 I1 I0 D7 D6 D5 D4 D3 D2 D1 D0
U_L_LongDataEnd	0xD0 0xD1	1101 000x	Upload check sum with last index x+1 (bit 8 .. 0) (1 ... 264) x: MSB (bit 8) of index - index x(bit 7 ... 0) - data byte	I7 I6 I5 I4 I3 I2 I1 I0 D7 D6 D5 D4 D3 D2 D1 D0 It is calculated as logical NOT XOR function over the individual bits of the preceding bytes of the frame.

An U_State.indication as a result of faulty UART control field is sent to the host as soon as possible in the follow-ing cases:

- protocol error flag set: undefined UART control field
- receiver error flag set: time between subsequent bytes of a service longer than the defined timeout

7.2 UART Service UART -> Host

Any service sent from E981.03 to host consists of one or more bytes. The first byte is the control field which identifies UART service. The E981.03 can handle the following three different UART services:

- **KNX** data link layer services are complete
- immediate acknowledge service include information about sending state
- UART control services are used to send requested information to the host controller or, in case of failures, a state indication

Table 5. UART Service - E981.03 to Host

Service Name	UART control field		Remarks / Description	followed by
	Hex	Bin		7 6 5 4 3 2 1 0
acknowledge (BUSY and NACK)	0x00	0000 0000	the preceding data telegram is negative and busy acknowledged by a combination of receiving nodes. 1)	
Reset.indication	0x03	0000 0011	indicate a Reset of the E981.03	
L_Data.confirm (negative)	0x0B	0000 1011	L_Data telegram negative confirm: the preceding data telegram was either negative acknowledged (either NACK or BUSY) by receiving node(s) or not acknowledged at all.	
acknowledge (NACK)	0x0C	0000 1100	the preceding data telegram is negative acknowledged by any of the receiving nodes. 1)	
L_Data telegram (L_ExtData frame)	0x10 0x14 0x18 0x1C 0x30 0x34 0x38 0x3C	0001 0000 0001 0100 0001 1000 0001 1100 0011 0000 0011 0100 0011 1000 0011 1100	First Byte (Control field of an frame which is received on **KNX** bus. 3)	an extended data frame (L_ExtData) Each complete received byte of the frame will be transmitted. (End of Frame indication will be a time gap above $t_{UART,IBG,RX}$ = 2.5ms.) The frame length is between 2 and 264 byte.
L_Data.confirm (positive)	0x8B	1000 1011	L_Data telegram positive confirm: the preceding data telegram was positive acknowledged (ACK) by the receiving node	
L_Data telegram (L_Data frame)	0x90 0x94 0x98 0x9C 0xB0 0xB4 0xB8 0xBC	1001 0000 1001 0100 1001 1000 1001 1100 1011 0000 1011 0100 1011 1000 1011 1100	First Byte (Control field) of an frame which is received on **KNX** bus. 3)	a data frame (L_Data) Each complete received byte of the frame will be transmitted. (End of Frame indication will be a time gap above $t_{UART,IBG,RX}$ = 2.5ms.) The frame length is between 2 and 64 byte.
acknowledge (BUSY)	0xC0	1100 0000	the preceding data telegram is busy acknowledged by any of the receiving nodes. 1)	
acknowledge (ACK)	0xCC	1100 1100	the preceding data telegram is positive acknowledged by all of the receiving nodes. 1)	

Service Name	UART control field		Remarks / Description	followed by
	Hex	Bin		7 | 6 | 5 | 4 | 3 | 2 | 1 | 0
L_PollData.request	0xF0	1111 0000	E981.03 is Poll_Master: uploaded L_PollData.request telegram	a data frame (L_PollData. request) Each complete received byte of the frame will be transmitted. (End of Frame indication will be a time gap above $t_{UART,IBG,RX}$ = 2.5ms.) The frame length is 7 byte.
			E981.03 is Poll_Slave: a Poll_Master can also be a Poll_Slave	write host to UART service U_PollingState with the corresponding data
U_ReadReg.response	0xF1	1111 0001	answer of U_ReadReg.request	D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0
U_ProductID.response	0xFE	1111 1110	answer of U_ProductID.request	I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0
State.response State.indication	0x_7 and 0x_F	abcd e111 a: [SC] b: [RE] c: [TE] d: [PE] e: [TW]	answer of - U_State.request - Indication of any state chance: [1] activation [0] deactivation see table below	

1) note: all acknowledge frames are transmitted to the host in Bus Monitor Mode only

2) each L_Data telegram is transmitted completely to the host controller.

3) Each correctly received byte is immediately transferred to the host processor.

Table 6. E981.03 State Indication

Name	Bit is set in case of
SC: slave collision	- an other polling slave uses same slot (and has higher "priority")
RE: receiver error	- check-sum error in uploaded telegram - parity error on UART - frame error on UART (stop bit wrong) - timeout violation between received service bytes
TE: transmitter error	- **KNX** transmitter sends "0", **KNX** receiver receives "1"
PE: protocol error	- illegal control byte in a service of telegram upload - transmit telegram buffer overrun (upload during telegram transmission on **KNX** bus) - U_L_DataContinue service with index 0 or greater than 263
TW: temperature warning	- temperature monitor signals too high temperature

7.3 SPI Logical Layer

Several bytes transferred subsequently during active chip select form a SPI access. The first byte of a SPI access is the command byte. It contains the following information:

1. distinction between read and write
2. decision whether to transmit a xor check-sum or
3. read accesses information about short or long access
4. upper part of address

If the XOR bit in the command byte is set a check-sum is calculated over the bytes of the access and transferred as last byte in master --> slave and slave --> master directions. Thus both master and slave have information about potentially incorrect transfer of command, address and data bytes.
In short form of read access the inter byte gap has to be regarded between byte 2 (address) and byte 3 (data). Otherwise the transmitted byte may not be correct.

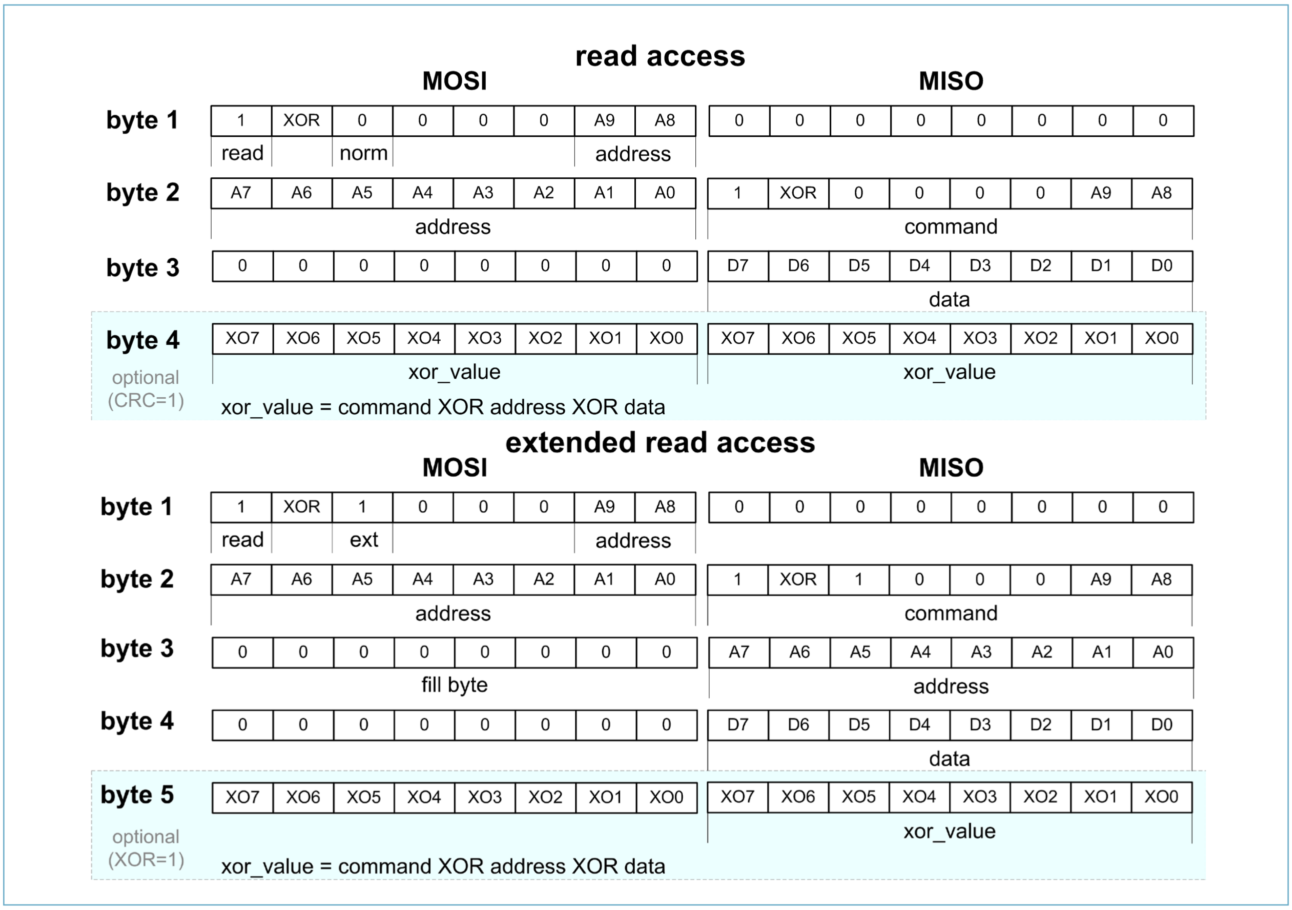


Figure 11. SPI read accesses

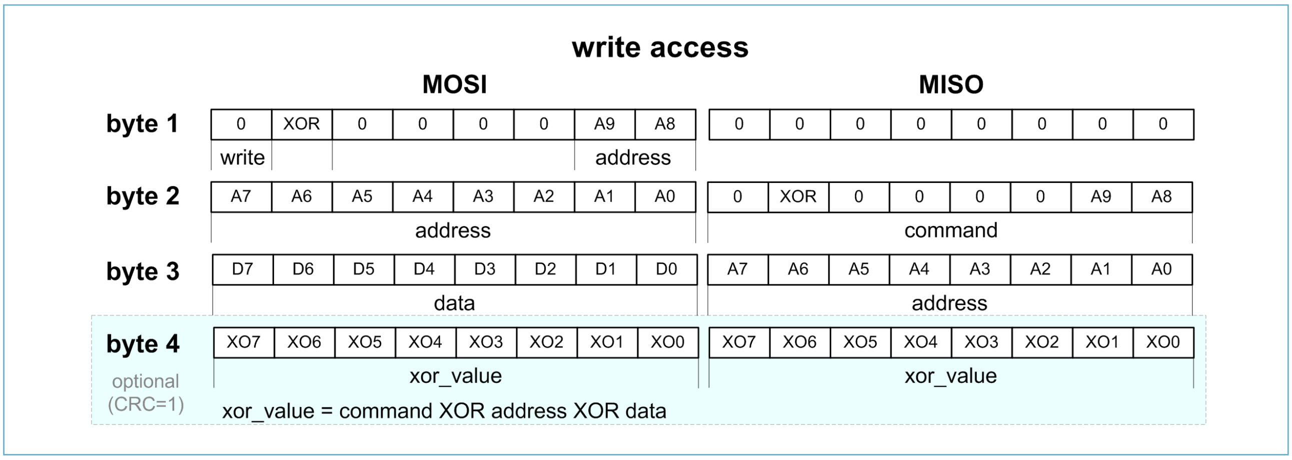


Figure 12. SPI write accesses

Via SPI the host is able to read all addresses in the ranges 0x000 ... 0x27F and 0x300-3FF.
Write access is allowed in the address range 0x000 ... 0x17F and 0x200 to 0x27F, except:

- UART_STAT (0x2A0)
- UART_RX (0x2A3)
- UART_TX (0x2A4)

7.4 SPI Timing

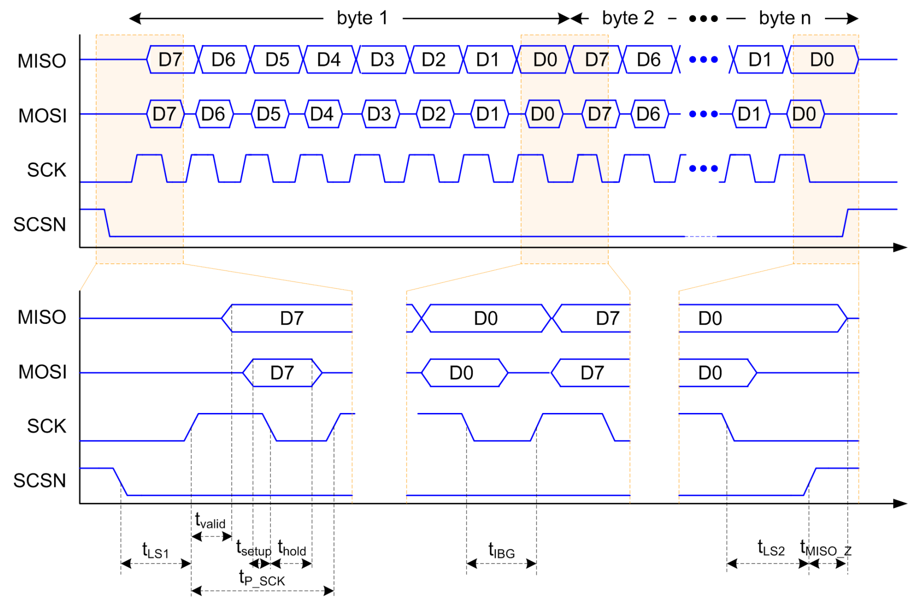


Figure 13. SPI timing

8 Monitoring Functions

For measurement reasons the voltages are scaled to low voltage domain V33I. For scaling factors please read Table Electrical Characteristics section Monitoring Functions.
For error calculations refer following tolerances: Divider, ADC, V33I Supply (tolerance depend on configuration and Mode).

8.1 Analog Monitoring Functions

As described in section 5.5 AOUT the AOUT is an analog monitoring pin with a high impedance. Possible sources are:

- Temperature voltage
- Band gap voltage
- Bus voltage

8.2 Digital Monitoring Functions

ADC unit converts a configurable count of analog signals to 8 bit resolution digital numbers. The signal conversion time of a selected channel is typical 5 µs at a clock frequency of 4 MHz. The input channels are converted in a continuously running conversion cycle. The ADC embedded system consists of:
8 bit SAR ADC Core

- high and low level reference generator
- conversion channel mux with input buffer
- channel sequence control unit
- result registers

In E981.03 ADC converts

- bus voltage VBUSP
- VST
- V20
- VCC
- VIO
- temperature (for details read chapter 8.3 Temperature Supervision)

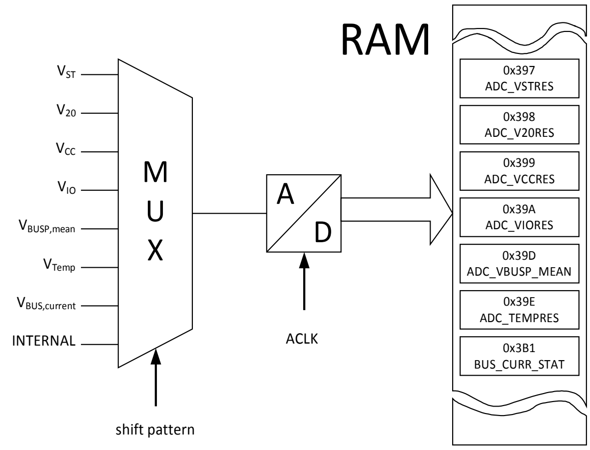


Figure 14. Digital Monitoring Functions

For measurement reasons the voltages are scaled to low voltage domain V33I. The scaled voltages are converted by the on chip ADC. For scaling factor look at chapter Electrical Functions section Monitoring Functions. The conversion results can be read by access to the result registers. The VBUSP is an average value ($t_{VBUSP(AV)}$ = 5 ms). ADC control cycle consists of two conversion cycles. The bus voltage is converted in the first conversion cycle of every control cycle. All other analog channels are converted in the second slot of the control cycle. The resulting conversion rate is approximately

- 70 k samples for bus voltage
- 10 .. 20 k samples for all other sources

Note: From VST supervision an active SAVE_N signal is generated in case of falling supply voltages. This allows the host processor to stop the application program and to save its data before the reset pin RESET_N becomes active.

8.3 Temperature Supervision

The temperature supervision is necessary for protection in case of high power dissipation in failure cases, for example short circuit of supply outputs.

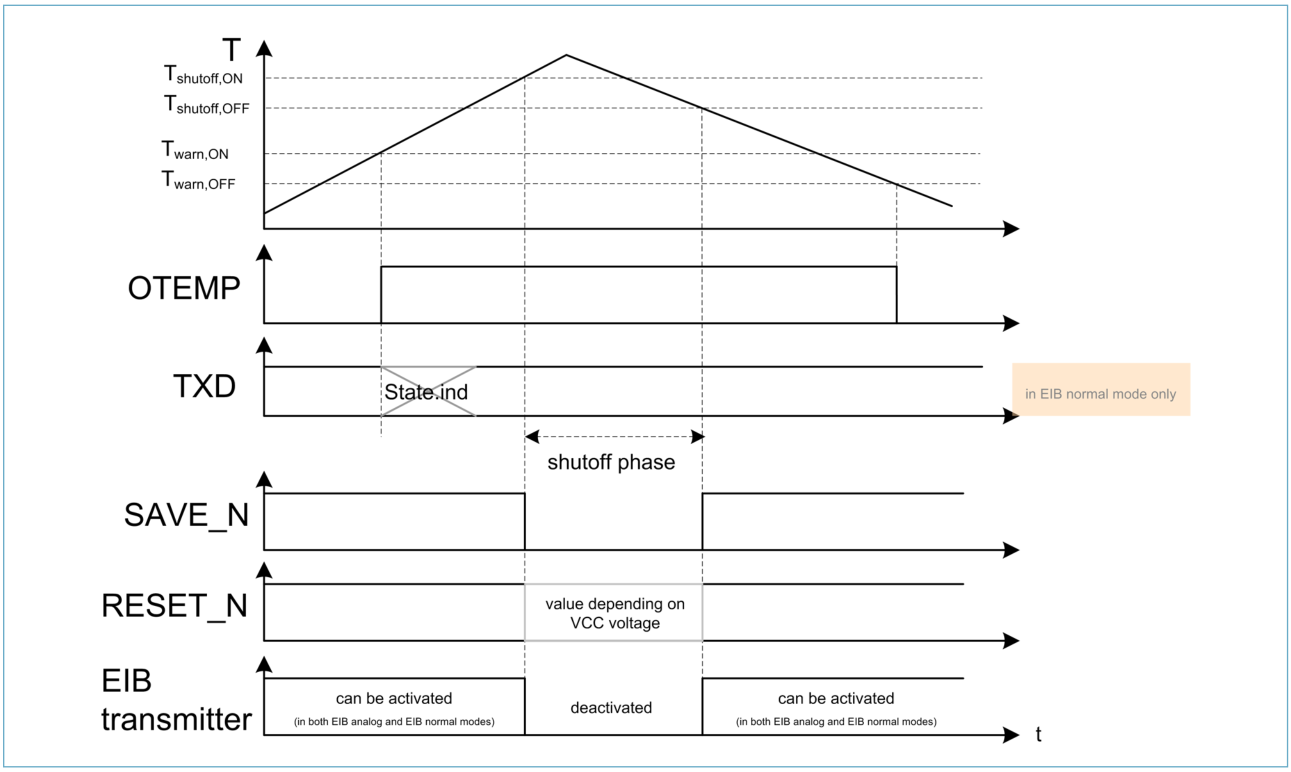


Figure 15. Over-temperature scenario

In case of over temperature

- the warning signal OTEMP for the host controller is generated
- in Normal Mode a State.indication service is sent to the host controller once at the beginning of over temperature situation

In case of further temperature rising power consuming blocks are switched off (shutoff phase):

- no further transmission at **KNX** (**KNX** transmitter is disabled) in both Analog and Normal Modes
- V20 and VCC supplies are switched off
- $\overline{\text{SAVE}}$ is activated
- $\overline{\text{RESET}}$ is activated when VCC is lower than the reset limit – not depending on temperature.

When E981.03 temperature is lower than the limit:

- VCC and V20 supplies are switched on again
- SAVE_N is deactivated
- **KNX** transmitter is enabled

9 E981.03 security functions

The E981.03 has two security functions featuring an external digital interface.

$\overline{\text{SAVE}}$	In case of an invalid VST voltage, the E981.03 activates the Save Mode to expand an active VCC time. The SAVE pin gives this status of the Save Mode to an external device (host processor).
OTEMP	The temperature supervision is necessary for protection in case of higher power dissipation in failure cases, for example short circuit of supply outputs. The OTEMP pin gives an over-temperature warning

10 RAM and register table

10.1 RAM table

Table 7. RAM address ranges

Address	Bytes	Content	App. note
0x000 ... 0x107	264	transmit frame buffer	
0x108 ... 0x109	2	individual **KNX** address of the **KNX**/EIB node	
0x10A ... 0x10B	2	polling address 1)	
0x10C	1	polling slot 1)	
0x10D	1	polling data 1)	
0x10E ... 0x10F	2	reserved for E981.03 internal use 2)	
0x110 ... 0x128	25	alarm telegram buffer	
0x129 ... 0x12F	7	reserved for E981.03 internal use 2)	
0x130 ... 0x148	25	trigger telegram buffer	
0x149 ... 0x14F	7	reserved for E981.03 internal use 2)	
0x150 ... 0x168	25	trigger mask buffer	
0x169 ... 0x16A	2	length of alarm telegram	
0x16B ... 0x16C	2	length of trigger telegram	
0x16D ... 0x1BF	82	reserved for E981.03 internal use 2)	
0x1C0 ... 0x1FF	64	received frame buffer 2)	
0x200 ... 0x2FF	256	registers table 3)	
0x300 ... 0x3FF	256	registers table 2) 3)	

1) May be written by the host during a L_PollData.request frame.
2) Writing to these addresses is not allowed
3) Only allowed access to the named registers, see table below (register table).

10.2 Register table

Table 8. Register Table

Register Name	Address	Description	App. note
CMODE	0x200	communication mode	
RESET_CTRL	0x201	Reset control register	
BUSY_REG	0x202	Busy Mode register	
SPI_CTRL	0x205	SPI control register	
SPI_PINS	0x206	SPI pin access	
UART_CTRL	0x208	UART control register	
CLK_CTRL	0x209	host clock control register	
CLK_FAC0	0x20A	lower 8 bit of the clock divider register	
CLK_FAC1	0x20B	upper 8 bit of the clock divider register	
PS_CTRL	0x20E	power supply control register	

Register Name	Address	Description	App. note
MAX_BUS_CURR	0x20F	set the maximum DC bus current	
CURRENT_SLOPE	0x210	set up the maximum bus current slope	
AOUT_CTRL	0x211	AOUT control register	
AOUT_SRC	0x212	AOUT source select register	
ALARM_STAT	0x213	alarm status register	
TRIGGER	0x214	trigger register	
KNX_TR_BUF_STAT	0x215	status of the transmit telegram buffer	
KNX_ADR_STAT	0x216	status of the address	
MAX_RST_CNT	0x217	number of retries in case of not acknowledge and busy	
KNX_TX_LEN1	0x218	length of the frame in the transmit buffer (bits 8)	
KNX_TX_LEN0	0x219	length of the frame in the transmit buffer (bits 7 ... 0)	
ACK_HOST	0x21A	acknowledge information from host	
POLL_CONF	0x21B	status of a polling slave	
UART_STAT	0x2A0	UART status register	
UART_RX	0x2A3	previous received byte	
UART_TX	0x2A4	UART transmitter data register	
DEVMODE	0x300	active device mode	
RES_SOURCE	0x302	binary coded reset source	
PINS	0x306	mode control and baud rate select pin values	
SPI_STAT	0x310	SPI status register	
PROD_ID	0x371	Product ID (read only)	
ADC_VSTRES	0x397	ADC result for the (scaled) voltage on VST	
ADC_V20RES	0x398	ADC result for the (scaled) voltage on V20	
ADC_VCCRES	0x399	ADC result for the (scaled) voltage on pin VCC	
ADC_VIORES	0x39A	ADC result for the (scaled) voltage on VIO	
ADC_VBUSP_MEAN	0x39D	mean value for VBUSP voltage	
ADC_TEMPRES	0x39E	ADC result temperature scan	
BUS_CURR_STAT	0x3B0	actual value of DC bus current	
PS_STAT	0x3BF	power supply status register	
ACK_KNXIC	0x3E9	acknowledge information from E981.03	

Table 9. Reset register

Register Name	Address	Description
RES_SOURCE	0x302	binary coded reset source

Table 10. Binary coded reset source

back to Table 8 Register Table

RES_SOURCE	MSB							LSB
content	-	-	-	-	-	SRC2	SRC1	SRC0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	value of reset source							
access	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)
bit description	**SRC** : binary coded reset source (see following table for valid values, reset value is “startup reset” value)							

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 11. Reset source

RES_SOURCE value	reset source
0x00	start-up reset (this is the only reset source that corresponds to register hard reset values)
0x01	the previous reset was initiated by an externally driven active $\overline{\text{RESET}}$
0x02	the previous reset was initiated by a Reset.request service
0x03	the previous reset was initiated by a write access to the RESET_CTRL register
0x04	E981.03 intern watchdog
0x05	the previous reset was initiated by a low VCC
0x07	E981.03 internal error

Table 12. Busy timeout register

Register Name	Address	Description
BUSY_REG	0x202	Busy Mode register

Table 13. BUSY_REG back to Table 8 Register Table

BUSY_REG	MSB						LSB
content	T7	T6	T5	T4	T3	T2	T1	T0
hard reset value	0	0	0	1	1	0	1	0
soft reset value	0	0	0	1	1	0	1	0
access	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 14. Timeout examples

BUSY_REG value	timeout value
255	1.02 s
175	0.7 s
26 (default)	0.1 s
0	0 s

Timebase is 4 ms per digit.

Table 15. Device mode registers

Register Name	Address	Description
DEVMODE	0x300	active device mode
CMODE	0x200	communication mode
PROD_ID	0x371	IC product ID (read only)
PINS	0x306	mode control and baud rate select pin values

Register CMODE is used for IC control and is intended to be written by host controller. Register DEVMODE reflects the state of the IC.

Table 16. Active device mode back to Table 8 Register Table

DEVMODE	MSB							LSB
content	M7	M6	M5	M4	M3	M2	M1	M0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	0	0	0	0	0	0	1	0
access	R [1]	R [1]	R [1]	R [1]	R [1]	R [1]	R [1]	R [1]
bit description	This register holds the value of the currently active mode. This mode may differ from the communication mode selected by the CMODE register for several reasons. Especially during mode changes the DEVMODE register reflects the currently active mode.							

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 17. Communication mode back to Table 8 Register Table

CMODE	MSB							LSB
content	-	-	-	-	-	CM2	CM1	CM0
hard reset value	0	0	0	0	0	1	0	0
soft reset value	-	-	-	-	-	1	0	0
access	R 1)	R 1)	R 1)	R 1)	R 1)	R/W 1)	R/W 1)	R/W 1)

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 18. E981.03 mode register values

Mode	Priority	Register CMODE	Register DEVMODE	Remarks
hard reset	1	don't care	0x00	reset state is active if internal power supply is down
start-up	3	don't care	0x01	
soft reset	4	don't care	0x02	
Analog	5	don't care	0x03	
Normal	5	0x04	0x04	0x04 is the reset value of register CMODE Normal Mode is active in case of CMODE values that do not define an other communication mode.
Bus monitor	5	0x05	0x05	
Busy	4	0x06	0x06	

Table 19. IC product ID (read only) back to Table 8 Register Table

PROD_ID	MSB							LSB
content	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
hard reset value	0	0	0	0	0	1	0	0
soft reset value	never changed							
access	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)
bit description	product ID will be changed in case of feature change.							

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

The state of several pins are accessible via register address PINS. The read value changes with pin voltages without respect to IC state.

Table 20. Mode control and baud rate select pin values back to Table 8 Register Table

PINS	MSB							LSB
content	SETVCC	BS1	BS0	ALARM	0	WK	$\overline{\text{RESET}}$	$\overline{\text{SAVE}}$
access	R	R	R	R	R	R	R	R
bit description	**SETVCC** : this bits reflects the value of the SETVCC pin information **BS1** : this bits reflects the value of the BS1 pin **BS0** : this bits reflects the value of the BS0 pin **ALARM** : this bits reflects the value of the ALARM condition (SETVCC=$V_{SETVCC,ALARM}$) **WK** : this bits reflects the value of the WK pin $\overline{\text{RESET}}$: this bits reflects the value of the $\overline{\text{RESET}}$ pin $\overline{\text{SAVE}}$: this bits reflects the value of the $\overline{\text{SAVE}}$ pin							

1) Access via UART service and SPI possible.

Table 21. Overview trigger register

Register Name	Address	Description
TRIGGER	0x214	wake-up register
TRIGGER_BUF	0x130 ... 0x148	25 byte trigger telegram buffer
TRIGGER_MASK	0x150 ... 0x168	25 byte trigger telegram mask buffer
TRIGGER_LEN1	0x16B	length of trigger telegram (high byte)
TRIGGER_LEN0	0x16C	length of trigger telegram (low byte)

Table 22. Trigger register

back to Table 8 Register Table

TRIGGER	MSB							LSB
content	-	-	-	-	EVENT	EN_OUT	MASK_BUF	BUF
hard reset value	0	0	0	0	0	1	0	0
soft reset value	-	-	-	-	-	1	0	0
access	R 1)	R 1)	R 1)	R 1)	R/W 1)	R/W 1)	R/W 1)	R/W 1)
bit description	**EVENT** : "1": a trigger event was detected "0": no trigger event detected The EVENT bit is initially cleared. If the IC receives a triggering telegram on KNX bus it acknowledges this telegram by sending a BUSY acknowledge on KNX bus and sets the EVENT bit. Any further incoming triggering telegram will not be BUSY acknowledged by the IC as long as the host does not clear the EVENT bit by writing a "0". Acknowledge generation based on auto address mode is not affected by the EVENT bit state. **EN_OUT** : "1": enable output stage (pull down disabled) "0": disable output stage (output tri-state, pull down enabled) **MASK_BUF** : "1": the trigger mask buffer was written completely "0": the trigger buffer was not written completely yet **BUF** : "1": the trigger buffer was written completely "0": the trigger buffer was not written completely yet Bits MASK_BUF and BUF are set by the E981.03 after successful upload using host UART interface. They may be written by the host directly.							

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 23. Alarm state register

Register Name	Address	Description
ALARM_STAT	0x213	alarm status register
ALARM_BUF	0x110... 0x128	25 byte alarm telegram buffer
ALARM_LEN1	0x169	length of alarm telegram (high byte)
ALARM_LEN0	0x16A	length of alarm telegram (low byte)

The alarm state register is used to signal the state of the alarm functionality and to control sending of the alarm telegram. Reading the register is allowed any time using any interface. Writing to the register is only recommended to clear the SENT bit and allow resending of the alarm telegram. A successful alarm telegram transmission is confirmed to the host by sending a L_Data.confirm service on host UART interface.

Table 24. Alarm status register Power supply registers

back to Table 8 Register Table

ALARM_STAT	MSB							LSB
content	-	-	-	-	-	PEND	BUF	SENT
hard reset value	0	0	0	0	0	0	0	0

ALARM_STAT	MSB						LSB
soft reset value	-	-	-	-	-	-	-	-
external access	R 1)	R 1)	R 1)	R 1)	R 1)	R/(W) 1)	R/W 1)	R/W 1)
bit description	**PEND** : "1": an alarm transmission is either pending, under transmission or sent (e.g. in case of alarm pin activation during transmission of a "normal" telegram) "0": no alarm is pending or sent Writing to the register using UART U_WriteReg service clears the PEND bit independent of the value that is written to that bit. Writing using SPI shall not change the value of the PEND bit which is not controlled by the E981.03 but is in the responsibility of the host controller. **BUF** : "1": the alarm buffer was written completely "0": the alarm buffer was not written completely yet The bit is set by the E981.03 after successful upload using host UART interface services. It may be written by the host directly to activate alarm functionality without using upload procedure via host UART interface or after uploading a alarm telegramm by SPI. The alarm telegram buffer is not checked for correctness in this case. **SENT** : "1": an alarm telegram was sent "0": no alarm telegram was sent The bit is set after sending of an alarm telegram. It can be reset by the host processor by writing a "0". The host should never write an "1" to the SENT bit. If the bit SENT is set no alarm telegram is transmitted regardless of the alarm condition. An ongoing alarm telegram transmission on EIB bus (states AlarmTelegramWait and AlarmTelegramTransmit) is not interrupted by writing a "0" to the SENT bit. A reading by UART Interface delete this bit. A SPI read do not delete this and the User have to do this.							

1) Access via UART service and SPI possible. For write access read the remarks of every bit carefully. In case of hard reset the register is reset to the hard reset value.

Table 25. Power supply registers

Register Name	Address	Description
PS_CTRL	0x20E	power supply control register
PS_STAT	0x3BF	power supply status register

Table 26. Power supply control register

back to Table 8 Register Table

PS_CTRL	MSB							LSB
content	VIO_SW	-	VCC_ON1 1)	VCC_ON0 1)	-	-	V20_ON1 1)	V20_ON0 1)
hard reset value	0	0	1	1	0	0	1	1
soft reset value	0	-	1	1	-	-	1	1
external access	R/W 2)	R	R/W 2)	R/W 2)	R	R	R/W 2)	R/W 2)
bit description	**VCC_ON** : "00": VCC is to switch off 1) "01","10","11": V_{CC} is to switch on The bits do not reflect the state of the V_{CC} supply. The actual state is reflected by PS_STAT register. **V20_ON** : "00": V_{20} is to switch off 1) "01","10","11": V_{20} is to switch on The bits do not reflect the state of the V_{20} supply. The actual state is reflected by PS_STAT register. **VIO_SW:** When VCC = 5 V and VIO = 3.3 V: write "1" to VIO_SW bit to reduce power consumption of E981.03. In all other cases this bit has no effect.							

1) The bits VCC_ON and V20_ON are doubled for safety reasons. VCC and V20 supplies are switched off only if both ON bits have value "0". Otherwise the supply is switched on and the ON bits are set to value "1" by the E981.03 itself.

2) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

In case VCC supply is switched off and either register PS_CTRL access or U_Reset.request UART service are used to switch VCC on the following will occur:

- VCC is switched on
- VCC is below its reset limit
- RESET will be activated
- soft reset will be performed

Remark:
As a result the E981.03 will restart with soft reset in these cases. Especially V20 will be switched on too.

Table 27. Power supply status register back to Table 8 Register Table

PS_STAT	MSB							LSB
content	-	-	-	-	-	-	VCC_ON	V20_ON
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)
bit description	**VCC_ON** : this bit represents the actual state of the VCC supply. "1": V_{CC} is switched on. "0": V_{CC} is switched off. **V20_ON** : this bit represents the actual state of the V20 supply. "1": V_{20} is switched on. "0": V_{20} is switched off.							

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 28. Bus current source registers

Register Name	Address	Description
MAX_BUS_CURR	0x20F	set the maximum DC bus current
BUS_CURR_STAT	0x3B0	actual ADC value of DC bus current
CURRENT_SLOPE	0x210	set up the maximum bus current slope

Table 29. Maximum DC bus current back to Table 8 Register Table

MAX_BUS_CURR	MSB							LSB
content	MAXCURR7	MAXCURR6	-	-	-	-	-	-
hard reset value	1	1	0	0	0	0	0	0
soft reset value	1	1	-	-	-	-	-	-
access	R/W 1)	R/W 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)
bit description	**MAXCURR** : maximum DC bus current selection							

1) For write access read the remarks of every bit carefully. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 30. Maximum DC bus current selection

MAXCURR7	MAXCURR6	Maximum DC bus current		
		min	typ	max
1	0	11.4 mA	12 mA	12.6 mA
1	1	17.1 mA	18 mA	18.9 mA
0	0	22.8 mA	24 mA	25.2 mA
0	1	28.5 mA	30 mA	31.5 mA

Table 31. Actual value of DC bus current back to Table 8 Register Table

BUS_CURR_STAT	MSB							LSB
content	CURR7	CURR6	CURR5	CURR4	CURR3	CURR2	CURR1	CURR0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 32. Set up the maximum bus current slope

back to Table 8 Register Table

CURRENT_SLOPE	MSB						LSB
content	-	-	-	-	-	-	SL1	SL0
hard reset value	0	0	0	0	0	0	0	1
soft reset value	-	-	-	-	-	-	0	1
access	R	R	R	R	R	R	R/W 1)	R/W 1)
bit description	see following table for SL values.							

1) Access via UART service and SPI possible. For write access read the remarks of every bit carefully. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 33. Bus current slope selection values

SL1	SL0	Slope limitation mode, mA/ms
0	0	0.25
0	1	0.5 (default)
1	0	1.25
1	1	2.5

Table 34. Clock registersSet up the maximum bus current slope

Register Name	Address	Description
CLK_CTRL	0x209	host clock control register
CLK_FAC0	0x20A	lower 8 bit of the clock divider register
CLK_FAC1	0x20B	upper 8 bit of the clock divider register

Table 35. Host clock control register

back to Table 8 Register Table

CLK_CTRL	MSB							LSB
content	-	-	-	-	-	EXT_Q	-	ENQ
hard reset value	0	0	0	0	0	0	0	1
soft reset value	-	-	-	-	-	0	-	1
access	R	R	R	R	R	W 1)	R	R/W 1)
bit description	**EXT_Q** : „1“: XTAL is used as clock input from external clock source, EXTAL is left open and internal capacitors are disconnected „0“: a quartz is connected to XTAL and EXTAL **ENQ** : „1“: crystal or clock enabled „0“: crystal or clock disabled and XTAL grounded useful e.g. for analog mode							

1) For write access read the remarks of every bit carefully. In case of soft and hard reset the state machine writes mentioned values.

Table 36. Clock divider register (low part)

back to Table 8 Register Table

CLK_FAC0	MSB							LSB
content	F7	F6	F5	F4	F3	F2	F1	F0
hard reset value	0	0	1	1	0	0	0	0
soft reset value	0	0	1	1	0	0	0	0
access	R/W 1)	R/W 1)	R/W 1)	R/W 1)	R/W 1)	R/W 1)	R/W 1)	R/W 1)

1) Access via UART service and SPI possible. For write access read the remarks of every bit carefully. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 37. Clock divider register (high part)

back to Table 8 Register Table

CLK_FAC1	MSB						LSB
content	F7	F6	F5	F4	F3	F2	F1	F0
hard reset value	1	1	1	0	0	0	1	1
soft reset value	1	1	1	0	0	0	1	1
access	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]

1) Access via UART service and SPI possible. For write access read the remarks of every bit carefully. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

The clock divider has a total reset value of 58.254. When using other quartz frequencies than 7.3728 MHz the value has to be changed to

$D_Q = f_{Quartz} / 126.76532\ Hz - 1$

Before changing the clock divider register values the timing unit of the E981.03 runs with the accuracy of the RC oscillator. Communication using the host UART interface has to take that accuracy into account. Specified UART and **KNX** communication parameter ranges are not guaranteed before adaption of the clock divider register.

The PLL has a tolerance of approximately 10% to input frequency for locking. As a result quartz frequencies in the range between $f_{Quartz, nom}$ – 10% and $f_{Quartz, nom}$ + 10% may be regarded as the nominal quartz frequency resulting in incorrect timing at the **KNX** and UART interfaces. It is highly recommended not to use quartz frequencies in that range or to change the CLK_FAC registers using SPI after each reset of the E981.03.

Individual Node Address

Each **KNX** device has a unique individual address in a network. The individual address is a 2 byte value that consists of an 8 bit subnetwork address and an 8 bit device address. The device address may have any value between 0 and 255.
The individual node address can be uploaded to the E981.03 from host using

- service request U_SetAddress on UART interface (see chapter 7.1 UART-Service Host -> UART) or writing to the appropriate RAM addresses (see chapter 7.3 SPI Logical Layer for details) and validate the address by writing to the KNX_ADR_STAT register.

After upload address evaluation in E981.03 is activated. After both hard and soft reset the address evaluation of E981.03 is deactivated.
The device address shall be unique within a sub-network.

The device address in E981.03 is not initialized to a defined value.

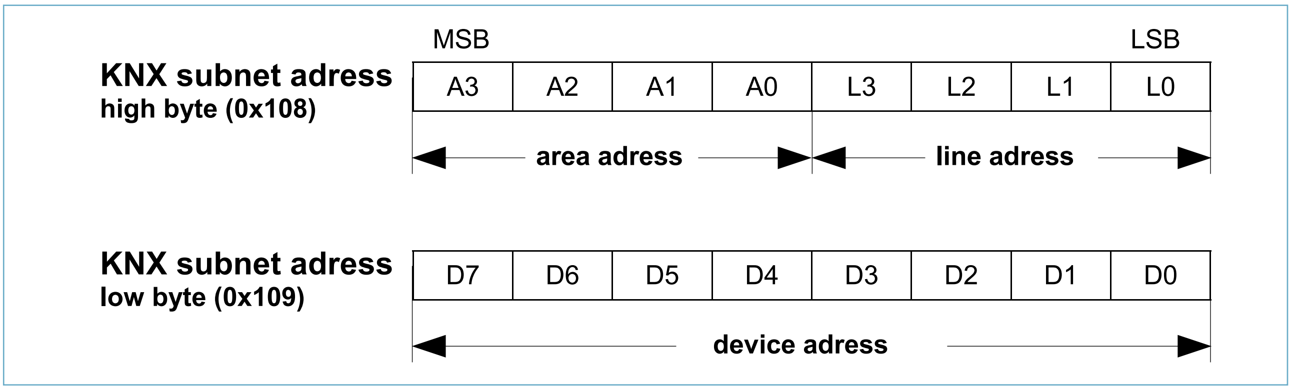


Figure 16. KNX individual address

Table 38. **KNX** address register

Register Name	Address	Description
KNX_ADR_STAT	0x216	status of the address
KNX_ADR_HIGH	0x108	**KNX** subnet adress high byte
KNX_ADR_LOW	0x109	**KNX** subnet adress low byte

Table 39. Status of the **KNX** address

back to Table 8 Register Table

KNX_ADR_STAT	MSB						LSB
content	-	-	-	-	-	-	VALID
hard reset value	0	0	0	0	0	0	0
soft reset value	-	-	-	-	-	-	0
access	R	R	R	R	R	R	R/W 1)
bit description	**VALID** : "1": the stored address is valid "0": the stored address is invalid the bit is set by the host by writing to the register or by using U_SetAddress service request it is reset. If the Address is configured by SPI the User have to set this bit too. - by the host by writing to the register and - during soft reset						

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 40. Telegram transmission register

Register Name	Address	Description
MAX_RST_CNT	0x217	number of retries in case of not acknowledge and busy
KNX_TR_BUF_STAT	0x215	status of the transmit telegram buffer
KNX_TX_LEN1	0x218	length of the frame in the transmit buffer (bit 8) 1)
KNX_TX_LEN0	0x219	length of the frame in the transmit buffer (bits 7 ... 0) 1)
KNX_TR_BUF	0x000 ... 0x107	264 Byte transmit buffer
KNX_RC_BUF	0x1C0... 0x1FF	64 Byte receiving frame buffer

1) The length of the frame gives the number of bytes stored in the frame transmit buffer including all frame overhead.

Table 41. MAX_RST_CNT

back to Table 8 Register Table

MAX_RST_CNT	MSB						LSB
content	-	BUSY2	BUSY1	BUSY0	-	NACK2	NACK1	NACK0
hard reset value	0	0	1	1	0	0	1	1
soft reset value	-	0	1	1	-	0	1	1
access	R	R/W 1)	R/W 1)	R/W 1)	R	R/W 1)	R/W 1)	R/W 1)
bit description	**ACK** : number of retries in case of not acknowledge (either NACK on no ack frame) **BUSY** : number of retries in case of busy (BUSY or simultaneously BUSY and NACK)							

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 42. Status of the transmit telegram buffer back to Table 8 Register Table

KNX_TR_BUF_STAT	MSB						LSB
content	-	-	-	-	-	-	READY
hard reset value	0	0	0	0	0	0	0
soft reset value	-	-	-	-	-	-	0
access	R	R	R	R	R	R	R/W [1)]
bit description	**READY** : "1": the RAM buffer is ready for transmission "0": the RAM buffer is not yet ready for transmission The bit is set by either the host processor or internal logic and reset after successful transmission. A manual write is only necessary if the frame is uploaded by SPI						

1) *Access via UART service and SPI possible. For write access read the remarks of every bit carefully. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.*

Table 43. Length of the frame in the transmit buffer (bit 8) back to Table 8 Register Table

KNX_TX_LEN1	MSB						LSB
content	-	-	-	-	-	-	LEN8
hard reset value	0	0	0	0	0	0	0
soft reset value	-	-	-	-	-	-	0
access	R	R	R	R	R	R	R/W [1)]

1) *Access via UART service and SPI possible. If a frame is uploaded by SPI the host controller have to set the LEN bits. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.*

Table 44. Length of the frame in the transmit buffer (bits 7 ... 0) back to Table 8 Register Table

KNX_TX_LEN0	MSB						LSB
content	LEN7	LEN6	LEN5	LEN4	LEN3	LEN2	LEN1	LEN0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	0	0	0	0	0	0	0	0
access	R/W [1)]	R/W [1)]	R/W [1)]	R/W [1)]	R/W [1)]	R/W [1)]	R/W [1)]	R/W [1)]

1) *Access via UART service and SPI possible. If a frame is uploaded by SPI the host controller have to set the LEN bits. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.*

Table 45. Acknowledge state register

Register Name	Address	Description
ACK_HOST	0x21A	acknowledge information from host
ACK_**KNX**IC	0x3E9	acknowledge information from E981.03

Table 46. Acknowledge information from host back to Table 8 Register Table

ACK_HOST	MSB							LSB
content	-	-	-	-	RX_ACK	NACK	BUSY	ADR
hard reset value	0	0	0	0	0	0	0	0
soft reset value	-	-	-	-	-	-	-	-
external access	R	R	R	R	R/W [1)]	R/W [1)]	R/W [1)]	R/W [1)]
bit description	**RX_ACK**:„1": acknowledge information from host for frame currently received "0": no acknowledge information from host for frame currently received Bit is set by host access via SPI or UART and reset by internal logic at start of a frame on **KNX** line. **NACK** : not acknowledge flag **BUSY** : busy flag **ADR** : addressed flag all flags are reset by the E981.03 at the beginning of a received frame.							

1) *Access via UART service and SPI possible. If a frame is uploaded by SPI the host controller have to set the LEN bits. In case of hard reset the register is reset to the hard reset value.*

Table 47. Acknowledge information used by E981.03 for previous received telegram back to Table 8 Register Table

ACK_KNXIC	MSB							LSB
content	-	-	-	-	-	NACK	BUSY	ADR
hard reset value	0	0	0	0	0	0	0	0
soft reset value	-	-	-	-	-	-	-	-
access	R	R	R	R	R	R 1)	R 1)	R 1)
bit description	**NACK** : not acknowledge flag **BUSY** : busy flag **ADR** : addressed flag all flags are reset by the E981.03 at the beginning of a received frame.							

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

POLLconf

Register POLL_CONF is completely handled by E981.03 when using host UART interface for communication. When using host SPI interface the host has to handle POLL_CONF register itself.

Table 48. Polling slave register

Register Name	Address	Description
POLL_CONF	0x21B	status of a polling slave
POLL_ADR_HIGH	0x10A	high byte
POLL_ADR_LOW	0x10B	low byte
POLL_SLOT	0x10C	polling slot
POLL_DATA	0x10D	polling data

Table 49. Status of a polling slave back to Table 8 Register Table

POLL_CONF	MSB							LSB
content	-	-	-	-	-	-	-	VALID
hard reset value	0	0	0	0	0	0	0	0
soft reset value	-	-	-	-	-	-	-	0
access	R	R	R	R	R	R	R	R/W 1)
bit description	**VALID** : "1": the data in the polling slave RAM area is valid for transmission "0": the data in the polling slave RAM area is invalid This bit is set by either the U_PollingState UART service request or direct writing to the register by the host. If the configuration is don by SPI the User have to set this bit too. It is reset by the E981.03 at the begin of a L_PollData.request frame reception on **KNX** bus (**KNX** control field 0xF0 was received).							

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 50. UART registers

Register Name	Address	Description
UART_CTRL	0x208	UART control register
UART_STAT	0x2A0	UART status register

The UART_CTRL register is used to control properties of the UART by host processor software. It is not modified by the E981.03. The UART_STAT register is used to signal UART state to the host processor software. The host is not allowed to modify the UART_STAT register.

Table 51. UART control register

back to Table 8 Register Table

UART_CTRL	MSB							LSB
content	-	-	-	TXDEL	CRC	-	ON1	ON0
hard reset value	0	0	0	0	0	0	1	1
soft reset value	-	-	-	0	0	-	1	1
access	R	R	R	R/W [1)]	R/W [1)]	R	R/W [1)]	R/W [1)]
bit description	**TXDEL**: "1": activate constant transmission delay between end of UART service and start of transmission on **KNX** bus "0": transmission delay between end of UART service and start of transmission on EIB bus is variable (faster) **CRC**: "1": the UART CRC is enabled (not available in analog mode and not at 9.6kBd) "0": the UART CRC is disabled **ON1** : **ON0** : "-1" or "1-": the UART is switched on "00": the UART is switched off							

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

1. The bit ON is doubled for safety reasons.
   UART interface is switched off only if both ON bits have value "0".
   Otherwise UART interface is switched on and the ON bits are set to value "1" by the E981.03 itself.
2. Bits ON1 and ON0 can not be modified using U_WriteReg service request.
   Use SPI to switch UART on and off.
   Bits TXDEL and CRC can be modified using either U_WriteReg service request or SPI.
3. Bit CRC is used to activate CRC calculation on UART to host communication. CRC is not used in case of **KNX** bus monitor mode or 9.6 k baud UART speed, independent on the value of the CRC bit of register UART_CTRL.

Table 52. UART status register

back to Table 8 Register Table

UART_STAT	MSB							LSB
content	-	-	-	-	-	-	-	ON
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R	R	R	R	R	R	R	R [1)]
bit description	**ON** : "1": the UART interface is currently on "0": the UART interface is currently off. This may be because of Analog Mode activation or because of a host write access to the UART_CTRL register							

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

UART Byte Receiver

The parity bit of every received byte from the host will be checked by the E981.03. Errors will be reported to the host controller by sending a State.indication service with receiver error flag set to the host as soon as possible.

The UART receiver accepts frames up to a maximum baud rate deviation of 3%. The signals can be transmitted without a break.

Table 53. UART receiver registers

Register Name	Address	Description
UART_RX	0x2A3	previous received byte

Table 54. Previous received byte

back to Table 8 Register Table

UART_RX	MSB						LSB
content	D7	D6	D5	D4	D3	D2	D1	D0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	-(not reset)							
access	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

UART Byte Transmitter

TXD idle-level in any other mode but **KNX** Analog Mode is "1".

The UART transmitter has a baud rate deviation of less than 1% during byte frame transmission. Subsequent bytes may be transmitted without a break.

Table 55. UART transmitter registers

Register Name	Address	Description
UART_TX	0x2A4	UART transmitter data register

Table 56. UART transmitter data register

back to Table 8 Register Table

UART_TX	MSB							LSB
content	D7	D6	D5	D4	D3	D2	D1	D0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	-(not reset)							
access	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)	R 1)

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 57. SPI registers

Register Name	Address	Description
SPI_CTRL	0x205	SPI control register
SPI_STAT	0x310	SPI status register
SPI_PINS	0x206	SPI pin access

Table 58. SPI control register

back to Table 8 Register Table

SPI_CTRL	MSB							LSB
content	-	-	-	-	-	-	ON1	ON0
hard reset value	0	0	0	0	0	0	1	1
soft reset value	-	-	-	-	-	-	1	1
access	R	R	R	R	R	R	R/W 1)	R/W 1)
bit description	**ON1** : **ON0** : "-1" or "1-": the SPI is switched on "00": the SPI is switched off							

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 59. SPI status register

back to Table 8 Register Table

SPI_STAT	MSB							LSB
content	-	-	-	-	-	-	-	XERR
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R	R	R	R	R	R	R	R 1)
bit description	**XERR** : XOR error detected							

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Register SPI_PINS is used for SPI pin value accesses. Bits $\overline{SCS}$ and SCK reflect the state of IC pins in any case of operation mode.
When SPI is switched off (bits ON1 and ON0 of register SPI_CTRL are both „0“) MOSI and MISO are used as general purpose input / output of the E981.03 that can be controlled by host processor. Pins $\overline{SCS}$ and SCK can be used as general purpose input pin.

Table 60. SPI pin access back to Table 8 Register Table

SPI_PINS	MSB							LSB
content	-	-	MOSIEN	MISOEN	MISO	MOSI	SCSN	SCK
hard reset value	register bits reflect always the state of the physical pins defining reset values makes no sense							
soft reset value								
SPI switched on	0	0	0	1	pin values			
SPI switched off access	R	R	R/W 1)	R/W 1)	R/W 1)	R/W 1)	R 1)	R 1)
bit description	**MOSIEN** : this bit set the pin direction 0 means high ohmic input 1 mean output. **MISOEN** : this bit set the pin direction 0 means high ohmic input 1 mean output. (enable for tri-state output) **MISO** : if the pin is used as a input this bit reflects the input state and if the pin is used as a output the user write the output level. **MOSI** : if the pin is used as a input this bit reflects the input state and if the pin is used as a output the user write the output level. **SCSN** : this bit reflects the input state of the $\overline{SCS}$ pin **SCK** : this bit reflects the input state of the SCK pin							

1) Access via UART service and SPI possible.

Table 61. RESET_CTRL

Register Name	Address	Description
RESET_CTRL	0x201	RESET_CTRL control register

Table 62. RESET_CTRL control register back to Table 8 Register Table

RESET_CTRL	MSB							LSB
content	-	-	-	-	-	-	-	RST
hard reset value	0	0	0	0	0	0	0	0
soft reset value	-	-	-	-	-	-	-	0
access	R	R	R	R	R	R	R	R/W 1)
bit description	**RST** : Writing a “1” to bit RST results in a transition to soft reset state. Writing to the RESET_CTRL register is the way to initiate a soft reset via either host SPI or host UART interfaces.							

1) Access via UART service and SPI possible. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Digital monitoring registers

The measurement values are scaled to limit them below the supply voltage (V33I) of the ADC and analog to digital converted. For scaling values look at chapter Electrical Charecteristics section Monitoring Functions.

Table 63. Voltage supervision registers

Register Name	Address	Description
ADC_VBUSP_MEAN	0x39D	mean value for V_{BUSP} voltage 1 LSB=$V_{BUSP,mean}$*$scale_{VBUSP,ADC}$/V33I +- 5%
ADC_VSTRES	0x397	ADC result for the (scaled) voltage on V_{ST} 1 LSB=V_{VST}*$scale_{VST,ADC}$/V33I +- 5%
ADC_V20RES	0x398	ADC result for the (scaled) voltage on V_{20} 1 LSB=V_{20}*$scale_{V20,ADC}$/V33I +- 5%
ADC_VCCRES	0x399	ADC result for the (scaled) voltage on pin V_{CC} 1 LSB=V_{CC}*$scale_{VCC,ADC}$/V33I +- 5%
ADC_VIORES	0x39A	ADC result for the (scaled) voltage on V_{IO} 1 LSB=V_{IO}*$scale_{VIO,ADC}$/V33I +- 5%

Table 64. Mean value for V_{BUSP} voltage back to Table 8 Register Table

ADC_VBUSP_MEAN	MSB						LSB
content	V7	V6	V5	V4	V3	V2	V1	V0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 65. ADC result for the (scaled) voltage on V_{ST} back to Table 8 Register Table

ADC_VSTRES	MSB							LSB
content	V7	V6	V5	V4	V3	V2	V1	V0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 66. ADC result for the (scaled) voltage on V_{20} back to Table 8 Register Table

ADC_V20RES	MSB							LSB
content	V7	V6	V5	V4	V3	V2	V1	V0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 67. ADC result for the (scaled) voltage on pin V_{CC} back to Table 8 Register Table

ADC_VCCRES	MSB							LSB
content	V7	V6	V5	V4	V3	V2	V1	V0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Table 68. ADC result for the (scaled) voltage on V_{IO}

back to Table 8 Register Table

ADC_VIORES	MSB						LSB
content	V7	V6	V5	V4	V3	V2	V1	V0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Temperature Supervision Register

The temperature supervision is necessary for protection in case of high power dissipation in failure cases, for example short circuit of supply outputs. For details read chapter 8.3 Temperature Supervision.

Table 69. Temperature supervision registers

Register Name	Address	Description
ADC_TEMPRES	0x39E	ADC result temperature scan

Table 70. ADC result temperature scan

back to Table 8 Register Table

ADC_TEMPRES	MSB							LSB
content	T7	T6	T5	T4	T3	T2	T1	T0
hard reset value	0	0	0	0	0	0	0	0
soft reset value	- (not reset)							
access	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]	R [1)]

1) Access via UART service and SPI possible. In case of hard reset the register is reset to the hard reset value.

Analog Monitor Pin

The pin AOUT is used to monitor several voltages. For details read chapter 5.5 AOUT.

Table 71. Analog monitor register

Register Name	Address	Description
AOUT_SRC	0x212	AOUT source select register
AOUT_CTRL	0x211	AOUT control register

Table 72. Source selector register for multiplexer on analog monitor pin

back to Table 8 Register Table

AOUT_SRC	MSB							LSB
content	-	-	-	-	-	-	S1	S0
hard reset value	0	0	0	0	0	0	1	0
soft reset value	-	-	-	-	-	-	1	0
access	R	R	R	R	R	R	R/W [1)]	R/W [1)]

1) Access via UART service and SPI possible. For write access read the remarks of every bit carefully. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

Table 73. Analog monitor multiplexer sources

AOUT_SRC value	Source
0x00	none; output is high impedance
0x01	temperature voltage
0x02	V_{BUSP} / 8 or V_{BUSP} / 12 depending on AOUT_CTRL register setting
0x03	bandgap voltage

Table 74. Bus voltage divider selection register

back to Table 8 Register Table

AOUT_CTRL	MSB						LSB
content	-	-	-	-	-	-	DIV
hard reset value	0	0	0	0	0	0	1
soft reset value	-	-	-	-	-	-	1
access	R	R	R	R	R	R	R/W [1)]

1) Access via UART service and SPI possible. For write access read the remarks of every bit carefully. In case of hard or soft reset the register is reset to the hard reset value or soft reset value respectively.

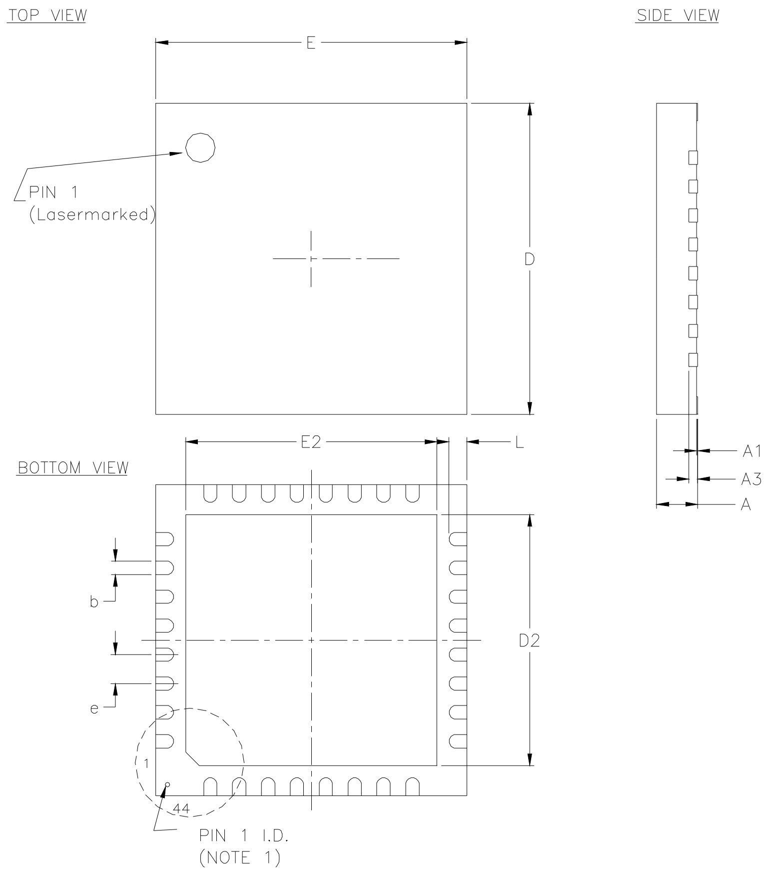
Table 75. Analog BUSP voltage multiplexer

AOUT_CTRL value	Source
0	V_{BUSP} / 12
1	V_{BUSP} / 8

In case of VIO = 3.3 V and bus voltage divider selection of V_{BUSP} / 12 pin voltage AOUT will not be higher than VIO even if V_{BUSP} / 12 is higher.

11 Package Information

The E981.03 is available in a Pb free, RoHS compliant, QFN32L7 plastic package according to JEDEC MO-220 K, variant VKKC-2. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020D with a soldering peak temperature of (260±5) °C.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.25	0.30	0.35	0.010	0.012	0.014
Package length / width	D / E	--	7.00 BSC	--	--	0.276 BSC	--
Length / width of exposed pad	D2 / E2	5.50	5.65	5.80	0.217	0.223	0.229
Lead pitch	e	--	0.65 BSC	--	--	0.026 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		32			32	

Note: the mm values are valid, the inch values contains rounding errors

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