# 3.3V, PCI Express® 3.0 2-Lane, 2:1 Mux/DeMux Switch, with Single Enable

## Features

- 4 Differential Channel, 2:1 Mux/DeMux
- PCI Express® 3.0 Performance, 8.0Gbps
- Bi-directional Operation
- Low Bit-to-Bit Skew, 10ps max
- Low channel-to-channel skew, 20ps max
- Low Crosstalk: -35dB@4 GHz
- High Off Isolation: -22dB@4 GHz (8.0Gbps)
- Low insertion loss: -1.3dB@4 GHz (8.0Gbps)
- Return loss: -21dB@4 GHz
- Support for DP1.2 - HBR2, HBR, RBR
- Supply Voltage 3.3V
- Packaging (Pb-free & Green):
  – 42-contact, TQFN (ZH42)

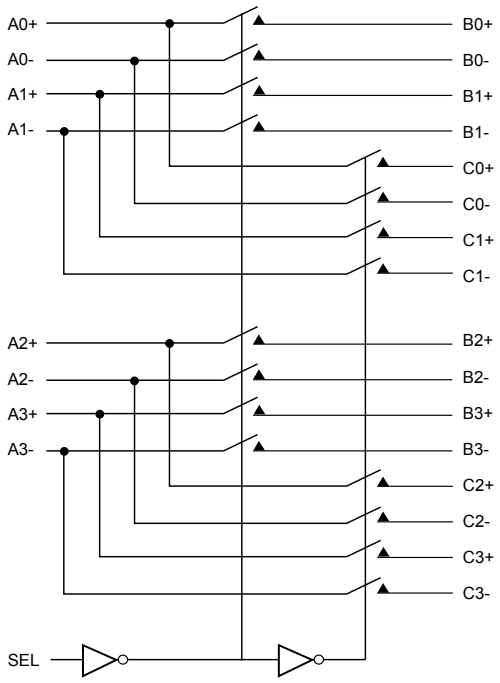
## Description

Pericom Semiconductor's PI3PCIE3412 is an 8 to 4 differential channel multiplexer/demultiplexer switch. This solution can switch 2 full PCI Express® 3.0, lanes to one of two locations. Using a unique design technique, Pericom has been able to minimize the impedance of the switch such that the attenuation observed through the switch is mininal. The unique design technique also offers a layout targeted for PCI Express signals, which minimizes the channel to channel skew as well as channel to channel crosstalk as required by the PCI Express specification. PI3PCIE3412 can also be used for application up to 12Gbps

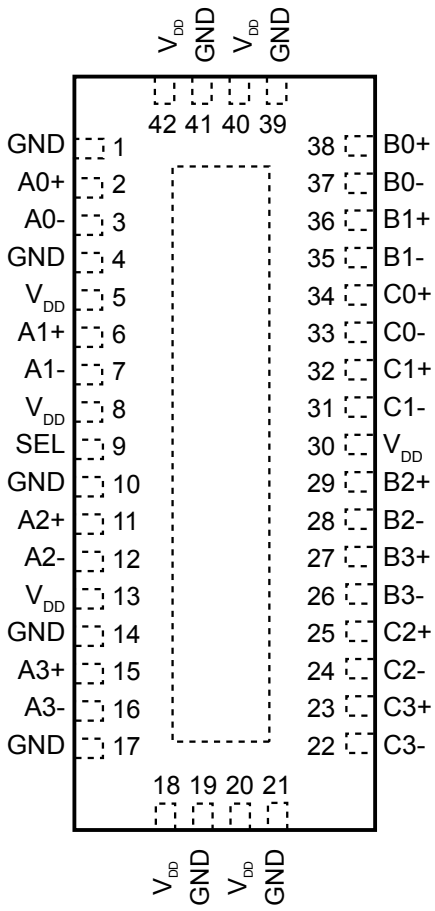
## Application

Routing of PCI Express 3.0, DP1.2, USB3.0, SAS2.0, SATA3.0, XAUI, RXAUI signals with low signal attenuation.

## Block Diagram




## Pin Configuration (Top-side view)




## Truth Table

| Function | SEL |
|---|---|
| $A_N$ to $B_N$ | L |
| $A_N$ to $C_N$ | H |

## Pin Description

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 2<br>3 | A0+<br>A0– | I/O | Signal I/O, Channel 0, Port A |
| 6<br>7 | A1+<br>A1– | I/O | Signal I/O, Channel 1, Port A |
| 11<br>12 | A2+<br>A2– | I/O | Signal I/O, Channel 2, Port A |
| 15<br>16 | A3+<br>A3– | I/O | Signal I/O, Channel 3, Port A |
| 38<br>37 | B0+<br>B0– | I/O | Signal I/O, Channel 0, Port B |
| 36<br>35 | B1+<br>B1– | I/O | Signal I/O, Channel 1, Port B |
| 29<br>28 | B2+<br>B2– | I/O | Signal I/O, Channel 2, Port B |
| 27<br>26 | B3+<br>B3– | I/O | Signal I/O, Channel 3, Port B |
| 34<br>33 | C0+<br>C0– | I/O | Signal I/O, Channel 0, Port C |
| 32<br>31 | C1+<br>C1– | I/O | Signal I/O, Channel 1, Port C |
| 25<br>24 | C2+<br>C2– | I/O | Signal I/O, Channel 2, Port C |
| 23<br>22 | C3+<br>C3– | I/O | Signal I/O, Channel 3, Port C |
| 9 | SEL | I | Operation mode Select<br>(when SEL=0: A→B, when SEL=1: A→C |
| 5, 8, 13,18, 20, 30, 40, 42 | $V_{DD}$ | Pwr | 3.3V ±10% Positive Supply Voltage |
| 1, 4, 10,14, 17, 19, 21, 39, 41, Center Pad | GND | Pwr | Power ground |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Supply Voltage to Ground Potential | –0.5V to +4.6V |
| Channel DC Input Voltage | –0.5V to 1.5V |
| DC Output Current | 120mA |
| Power Dissipation | 0.5W |
| SEL DC Input Voltage | –0.5V to 4.6V |

**Note:** Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | 3.3V Power Supply | | 3.0 | 3.3 | 3.6 | V |
| $I_{DD}$ | Total current from $V_{DD}$ 3.3V supply | SEL = 0V or $V_{DD}$ | | 0.15 | 1 | mA |
| $V_{I/O}$-DIF | Differential Voltage (differential pins) | | | | 1.6 | $V_{ppd}$ |
| $V_{I/O-CM}$ | Common Mode Voltage (differiential pins) | | 0 | | 0.8 | V |
| $T_{CASE}$ | Case temperature range for operation within spec. | | -40 | | 85 | Celsius |

## DC Electrical Characteristics for Switching over Operating Range

| Parameters | Description | Test Conditions[1] | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ - SEL | Input HIGH Voltage, SEL Input | | 2 | | 3.6 | V |
| $V_{IL}$ - SEL | Input LOW Voltage, SEL Input | | 0 | | 0.8 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$ = Max., $I_{IN}$ = –18mA | | –0.7 | –1.2 | |
| IIH | Input HIGH Current, SEL | $V_{DD}$ = Max., $V_{IN}$ = $V_{DD}$ | | | ±5 | µA |
| $I_{IL}$ | Input LOW Current, SEL | $V_{DD}$ = Max., $V_{IN}$ = 0V | | | ±5 | |
| $I_{IN}$ - SEL | Input Leakage Current, SEL Input | $V_{IN}$ = $V_{IH}$ - SEL Max or $V_{IL}$ - SEL Min | –10 | | +10 | µA |
| IIH | Input HIGH Current, $A_X$, $B_X$, $C_X$ | $V_{DD}$ = Max., $V_{IN}$ = 1.5V | –10 | | +10 | µA |
| $I_{IL}$ | Input LOW Current, $A_X$, $B_X$, $C_X$ | $V_{DD}$ = Max., $V_{IN}$ = 0V | –10 | | +10 | |
| $I_{OZH}$ | HighZ HIGH Current, $B_X$, $C_X$ | $V_{DD}$ = Max., $V_{IN}$ = 1.5V | –10 | | +10 | µA |
| $I_{OZL}$ | HighZ LOW Current, $B_X$, $C_X$ | $V_{DD}$ = Max., $V_{IN}$ = 0V | –10 | | +10 | µA |
| $C_{I/O-ON}$ | ON state I/O capacitance | | | 1.5 | | pF |
| $R_{ON}$ | ON state resistance | $V_{DD}$ = 3.3V, IO = 8mA, $V_{IN}$ = 0.8V | | 5 | | Ω |

**Note:**

1. Typical values are at $V_{DD}$ = 3.3V, $T_A$ = 25°C ambient and maximum loading.

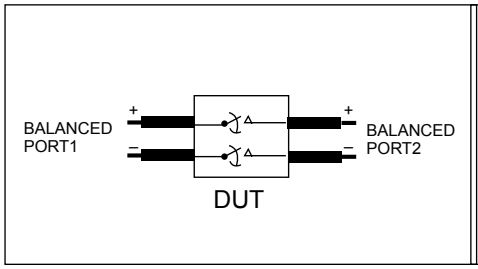
## Switching Characteristics

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PZH}$, $t_{PZL}$ | Line Enable Time - SEL to $A_N$, $B_N$, $C_N$ | | 2 | 20 | 25 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Line Disable Time - SEL to $A_N$, $B_N$, $C_N$ | | 0.5 | 5 | 25 | |
| $t_{b-b}$ | Bit-to-bit skew within the same differential pair | | | 5 | 10 | ps |
| $t_{ch-ch}$ | Channel-to-channel skew | | | | 20 | ps |

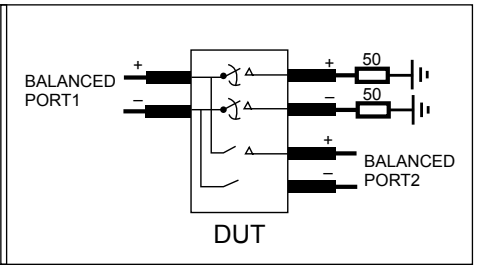
## Dynamic Electrical Characteristics

| Param-eter | Description | Test Conditions | Min. | Typ.(1) | Max. | Units |
|---|---|---|---|---|---|---|
| DDIL | Differential Insertion Loss ($V_{IN}$ = -10dBm, DC = 0V) | f= 50MHz - 1.25GHz<br>f=1.25GHz - 2.5GHz<br>f=2.5GHz - 4GHz<br>f=5GHz | | -0.8<br>-1.0<br>-1.3<br>-1.8 | -1<br>-1.2<br>-1.6<br>-2.2 | dB |
| $DDIL_{OFF}$ | Differential Off Isolation | f= 50MHz - 1.25GHz<br>f=1.25GHz - 2.5GHz<br>f=2.5GHz - 4GHz<br>f=5GHz | -26.3<br>-21.4<br>-17.6<br>-16 | -32.9<br>-26.7<br>-22<br>-20 | | dB |
| DDRL | Differential Return Loss | f= 50MHz - 1.25GHz<br>f=1.25GHz - 2.5GHz<br>f=2.5GHz - 4GHz<br>f=5GHz | -20<br>-18.4<br>-16.8<br>-9.6 | -25<br>-23<br>-21<br>-12 | | dB |
| DDNEXT | Near End Crosstalk | f= 50MHz - 1.25GHz<br>f=1.25GHz - 2.5GHz<br>f=2.5GHz - 4GHz<br>f=5GHz | -34.1<br>-30.5<br>-28.1<br>-27.2 | -42.6<br>-38.1<br>-35.1<br>-34 | | dB |
| $V_{IF}$ | Max Signal Frequency Range | Insertion loss 1.5dB, $V_{IN}$=0.623Vpp, DC=0V | | 4.0 | | GHz |
| | | Insertion loss 1.5dB, $V_{IN}$=0.623Vpp, DC=0.9V | | 4.0 | | |
| | | Insertion loss 3dB, $V_{IN}$=0.623Vpp, DC=0V | | 8.0 | | |
| | | Insertion loss 3dB, $V_{IN}$=0.623Vpp, DC=0.9V | | 8.0 | | |
| BW | -3dB Bandwidth | | | 8.2 | | GHz |

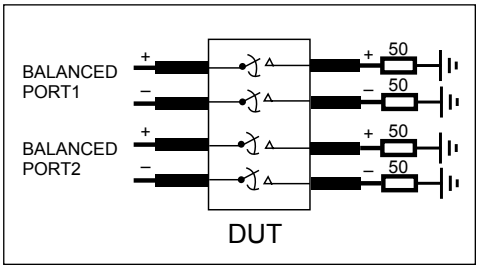
**Notes:**
1. Guaranteed by design. Typical values are at $V_{DD}$ = 3.3V , $T_A$ = 25°C ambient and maximum loading.




**Diff. Insertion Loss and Return Test Circuit**

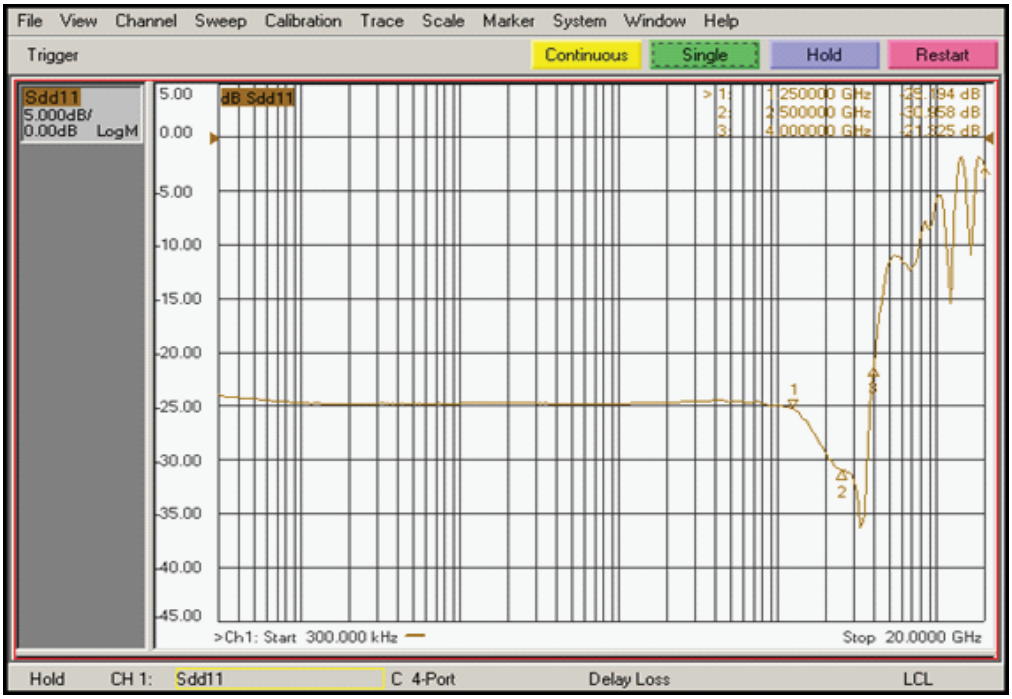



**Diff. Off Isolation Test Circuit**

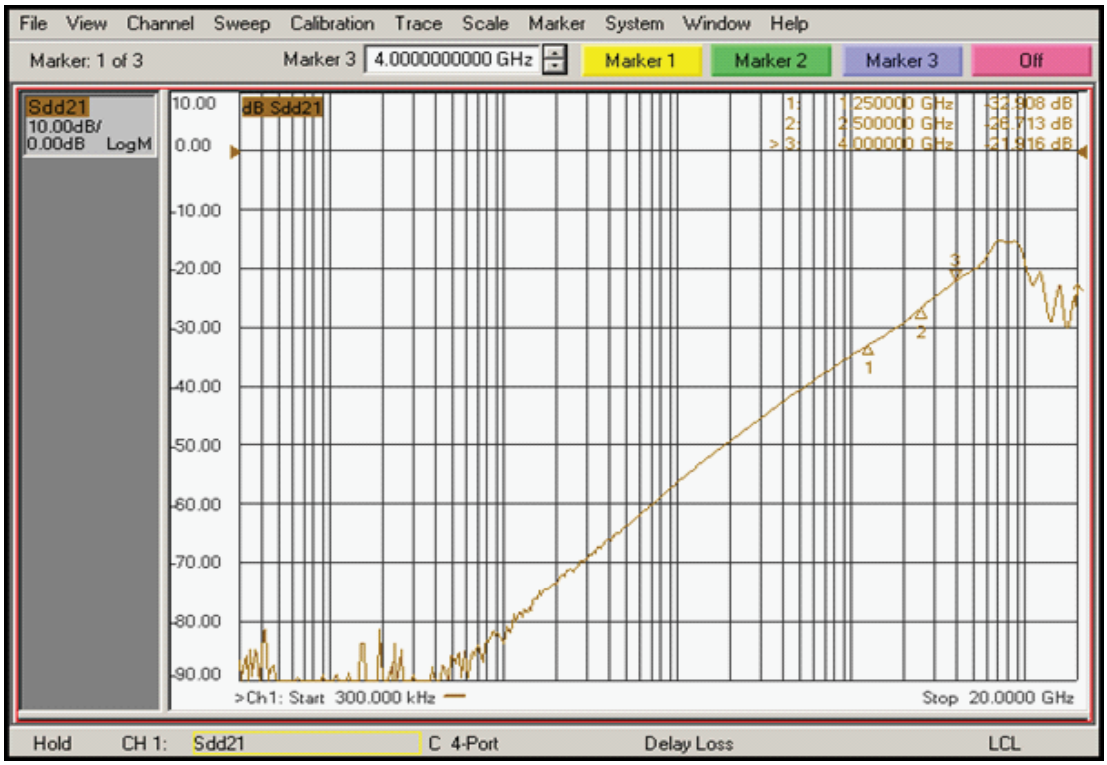



**Diff. Near End Xtalk Test Circuit**

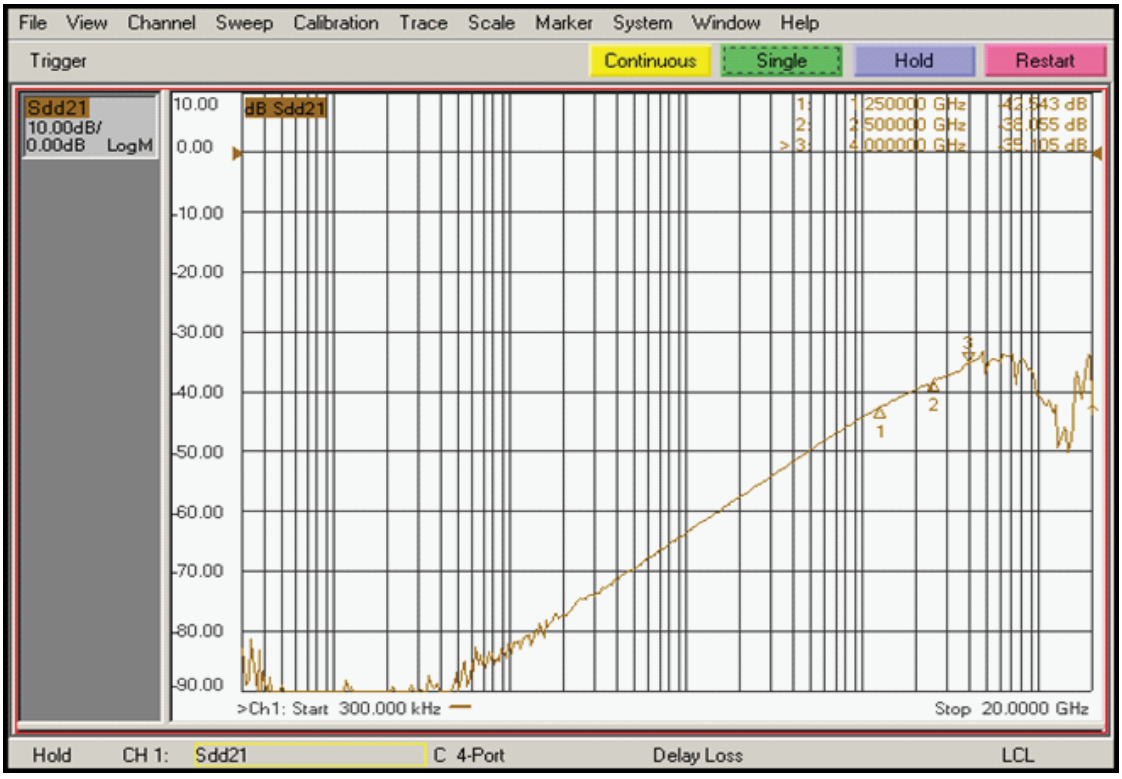

**Differential Insertion Loss**



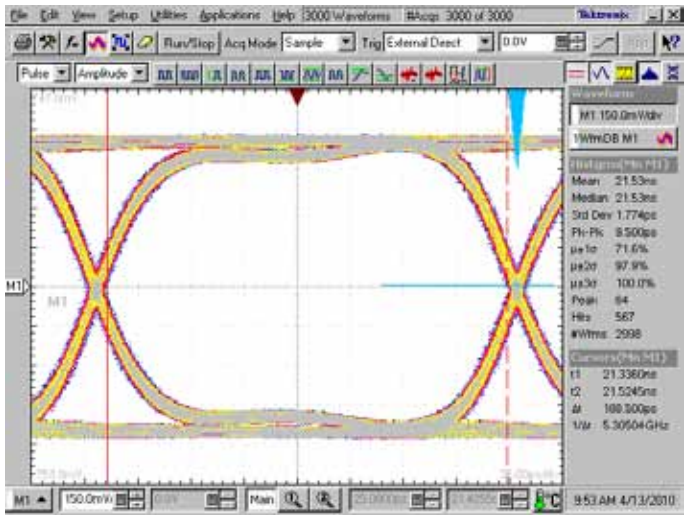

**Differential Return Loss**



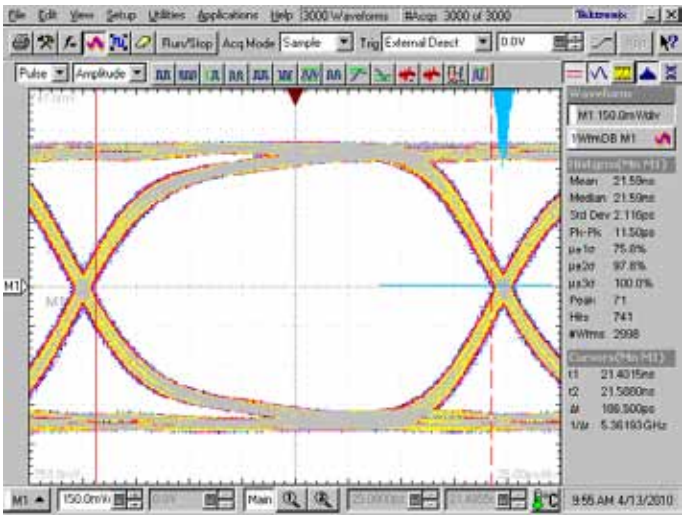

**Differential Off Isolation**



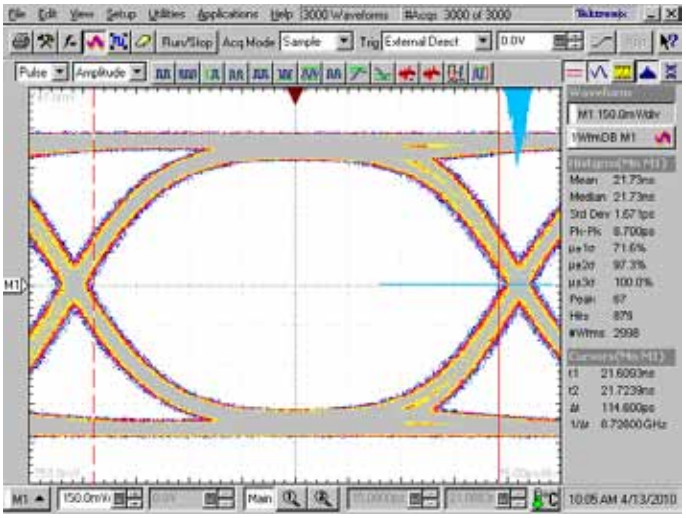

**Differential Crosstalk**



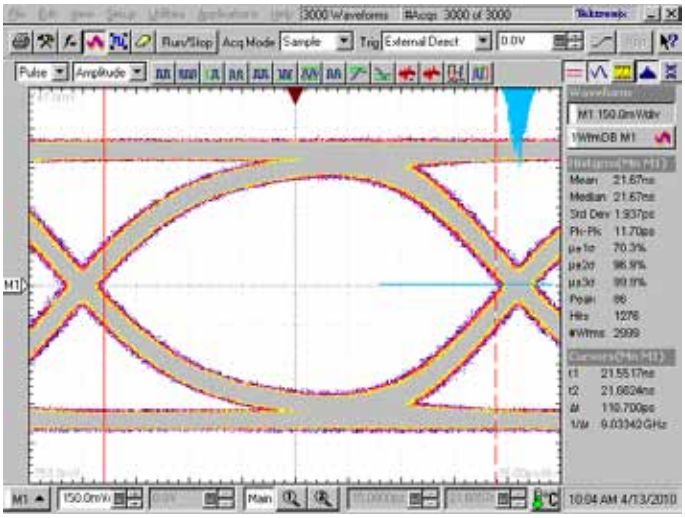
**5.0 Gbps RX signal eye without PI3PCIE3412**



**5.0 Gbps RX signal eye with PI3PCIE3412**

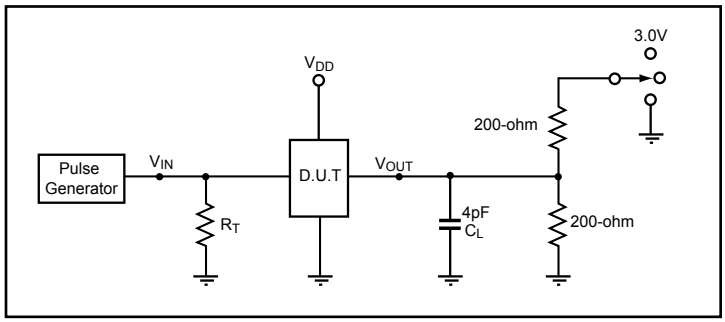


**8.0 Gbps RX signal eye without PI3PCIE3412**



**8.0 Gbps RX signal eye with PI3PCIE3412**

## Test Circuit for Electrical Characteristics(1-5)



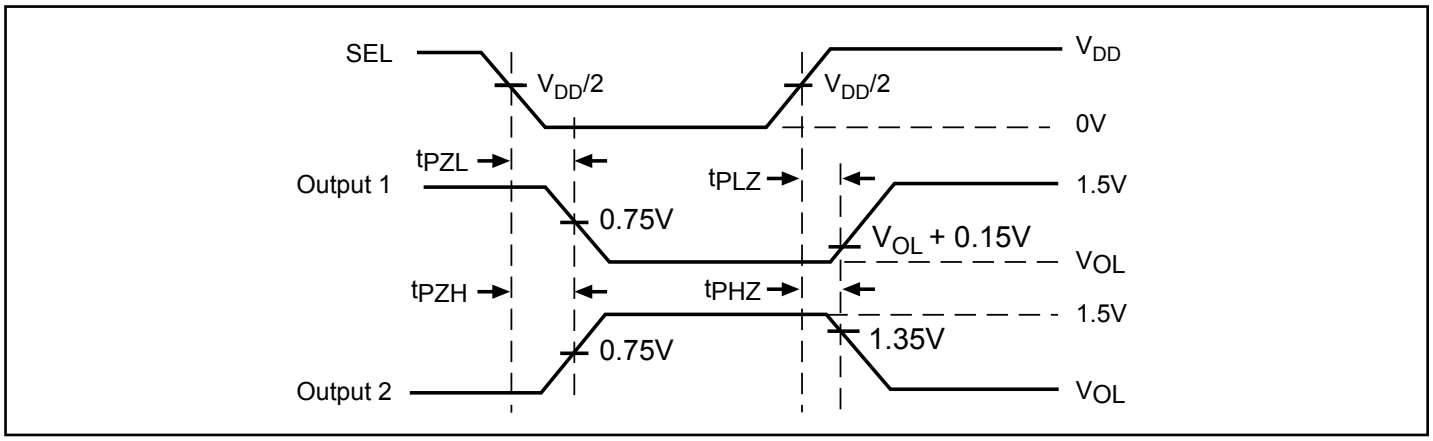

## Switch Positions

| Test | Switch |
|---|---|
| $t_{PLZ}$, $t_{PZL}$ | 3.0V |
| $t_{PHZ}$, $t_{PZH}$ | GND |
| Prop Delay | Open |

**Notes:**

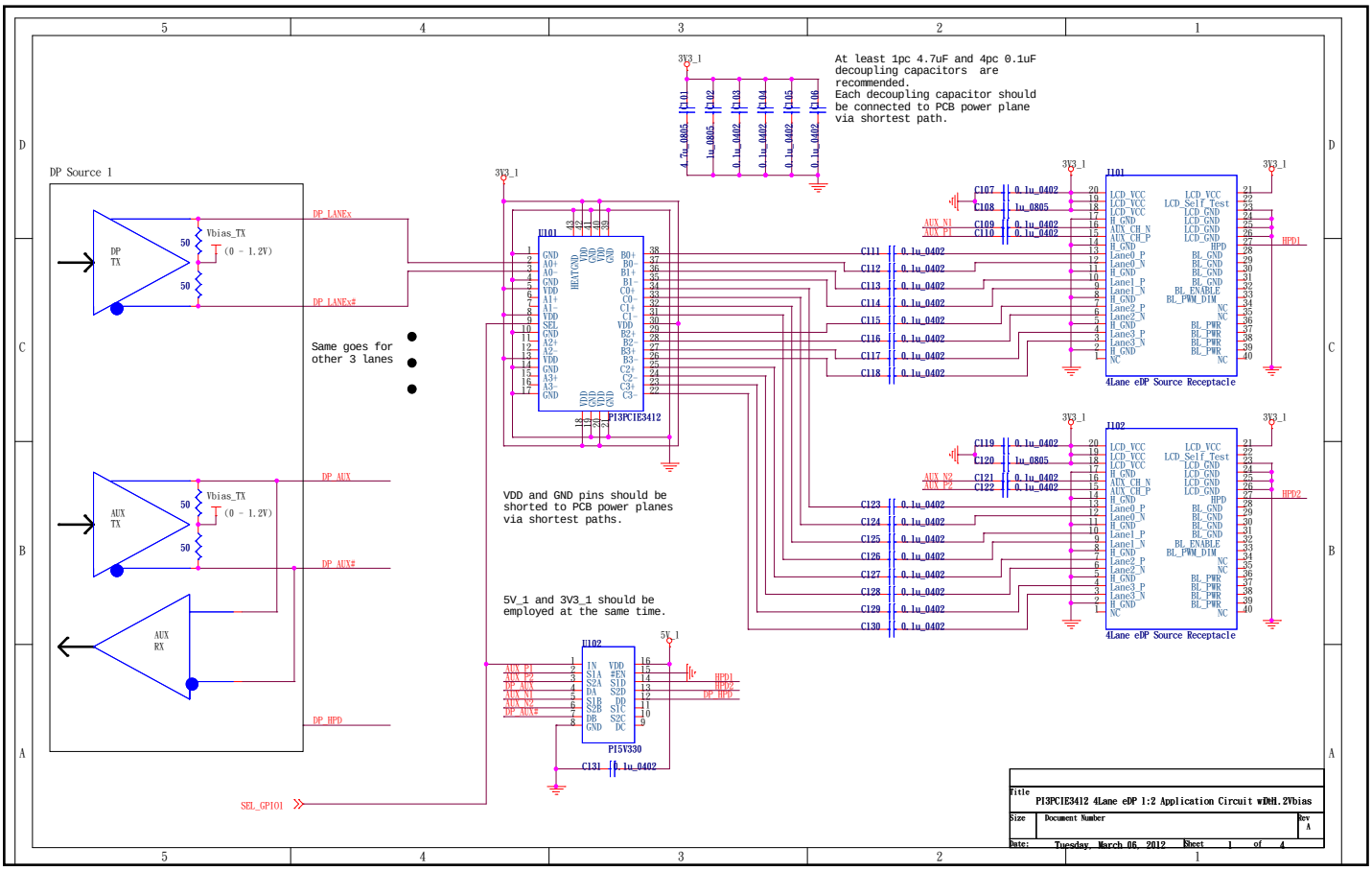
1. $C_L$ = Load capacitance: includes jig and probe capacitance.
2. $R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
5. The outputs are measured one at a time with one transition per measurement.

## Switching Waveforms

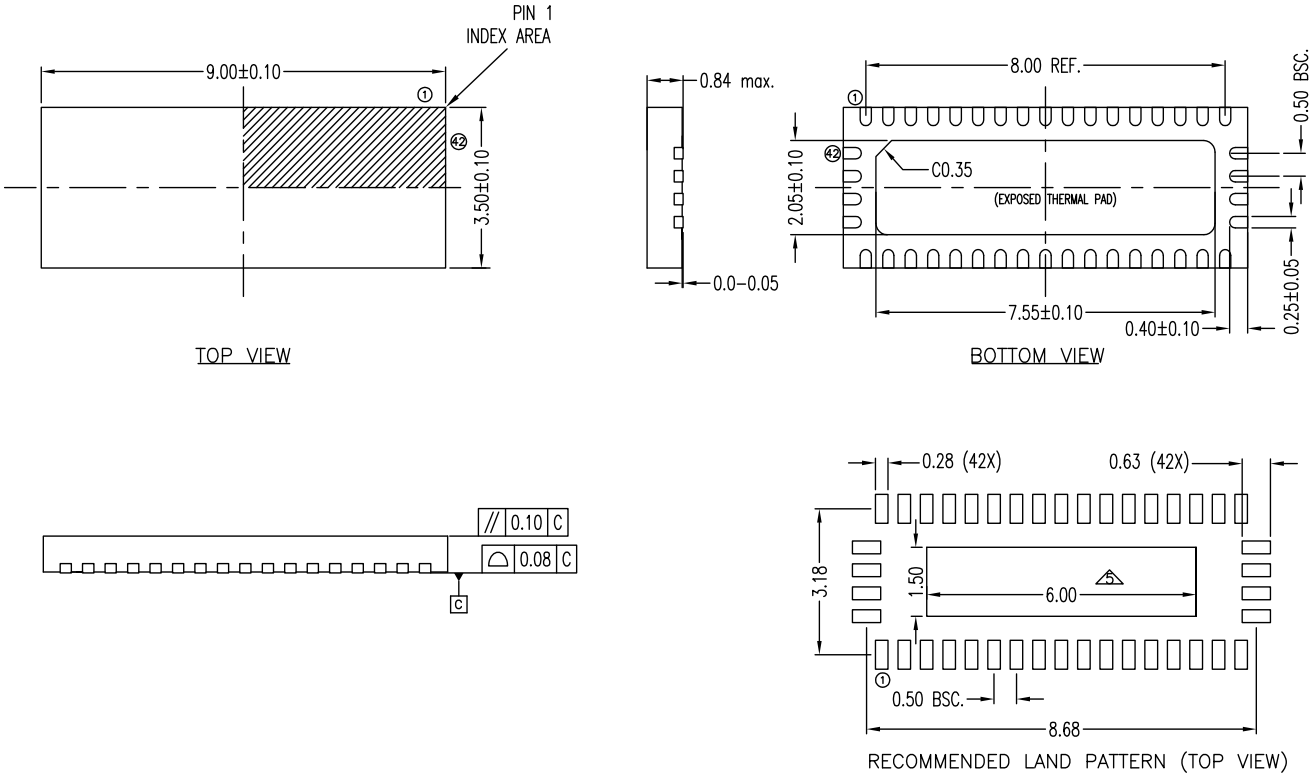



**Voltage Waveforms Enable and Disable Times**

## DP1.2 Application



## Packaging Information




**Notes:**
1. All dimensions are in millimeters. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220.
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area

| | |
|---|---|
| PERICOM Enabling Serial Connectivity | DATE: 11/14/12 |
| DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN) | |
| PACKAGE CODE: ZH42 | |
| DOCUMENT CONTROL #: PD-2035 | REVISION:D |

**Note:**
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

## Ordering Information

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI3PCIE3412ZHE | ZH | Pb-free & Green, 42-contact TQFN |

**Notes:**
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging