

RJF0411JPD

40V, 34A Silicon N Channel
Thermal FET Power Switching

R07DS1258EJ0100
Rev.1.00
Jun 23, 2015

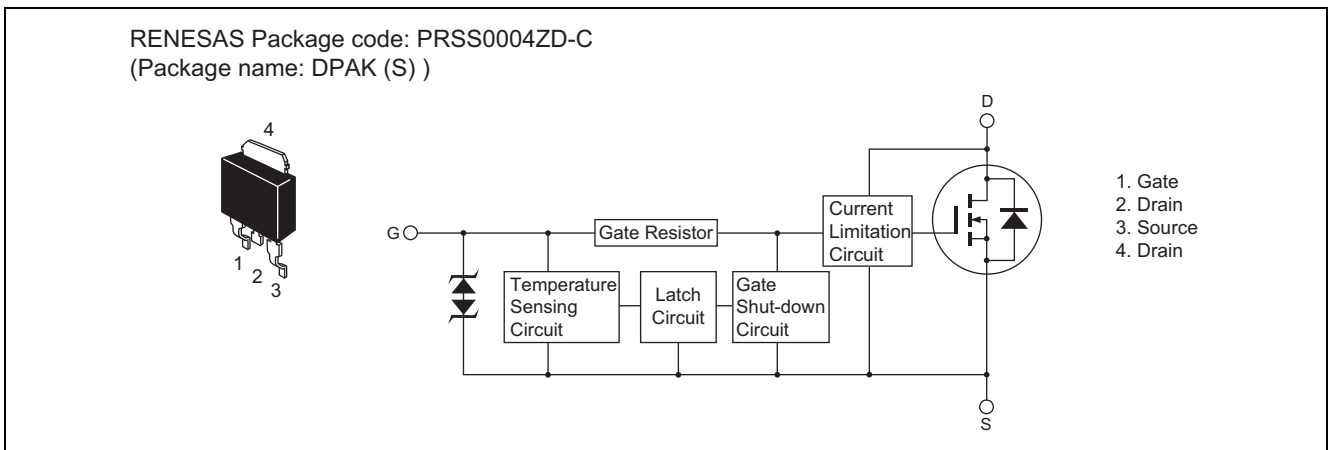
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation.
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V.
- AEC-Q101 Compliant.
- Endurance capability against to ESD.

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	40	V
Gate to source voltage	V _{GSS}	16	V
Gate to source voltage	V _{GSS}	-2.5	V
Drain current	I _D ^{Note3}	34	A
Body-drain diode reverse drain current	I _{DR}	34	A
Avalanche current	I _{AP} ^{Note 2}	5	A
Avalanche energy	E _{AR} ^{Note 2}	166	mJ
Channel dissipation	P _{ch} ^{Note 1}	40	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. Value at Tc = 25°C
 2. T_{ch} = 25°C, R_g ≥ 50 Ω
 3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	3.5	—	—	V	
	V _{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	100	μA	V _i = 8 V, V _{DS} = 0
	I _{IH2}	—	—	50	μA	V _i = 3.5 V, V _{DS} = 0
	I _{IL}	—	—	1	μA	V _i = 1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	0.8	—	mA	V _i = 8 V, V _{DS} = 0
	I _{IH(sd)2}	—	0.35	—	mA	V _i = 3.5 V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V _{op}	3.5	—	12	V	
Drain current (Current limitation value)	I _{D limit}	34	—	—	A	V _{GS} = 5 V, V _{DS} = 10 V ^{Note 4} T _c ≤ 80°C

Note: 4. Pulse test

Electrical Characteristics

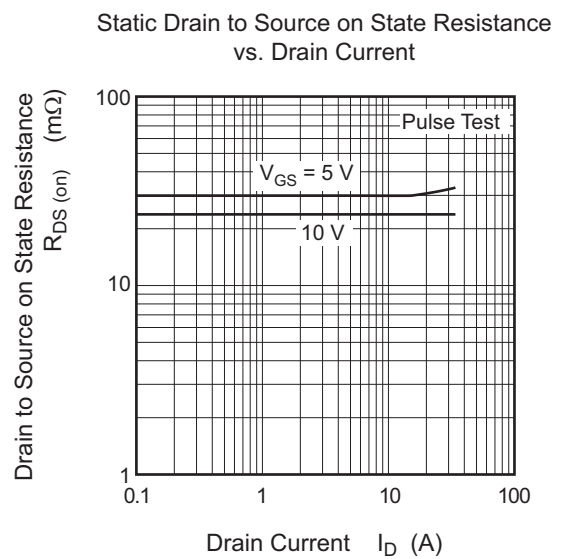
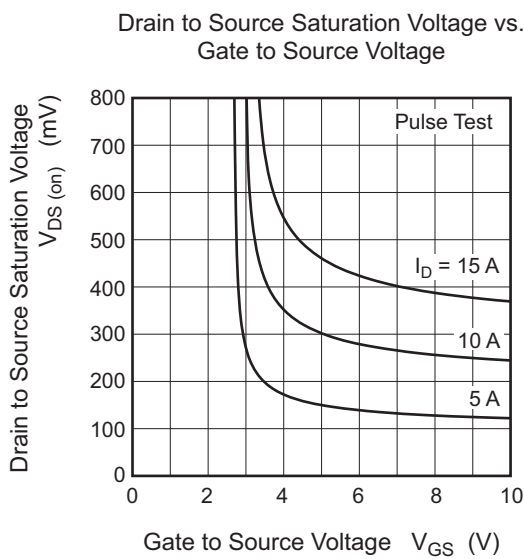
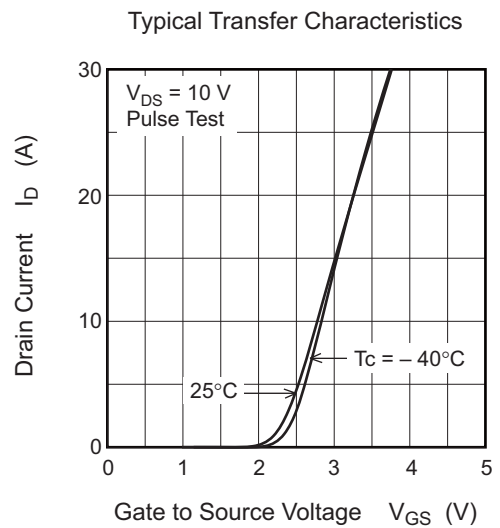
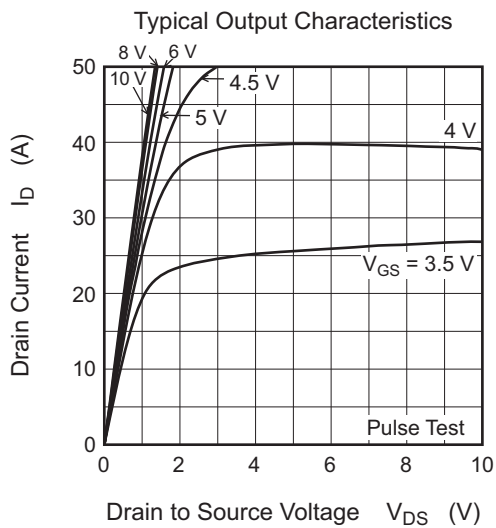
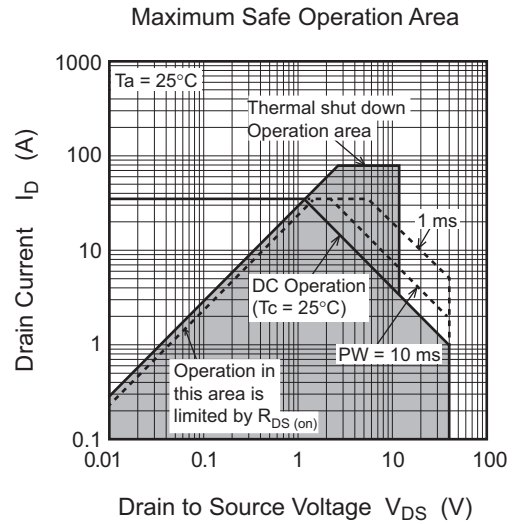
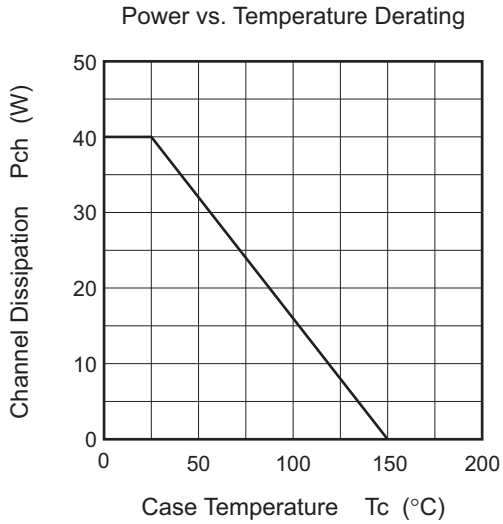
(Ta = 25°C)

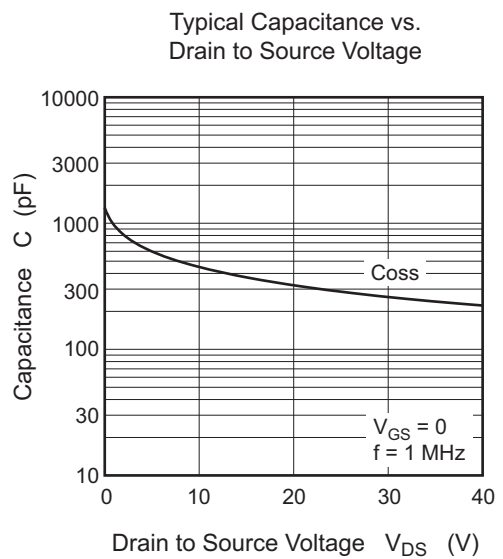
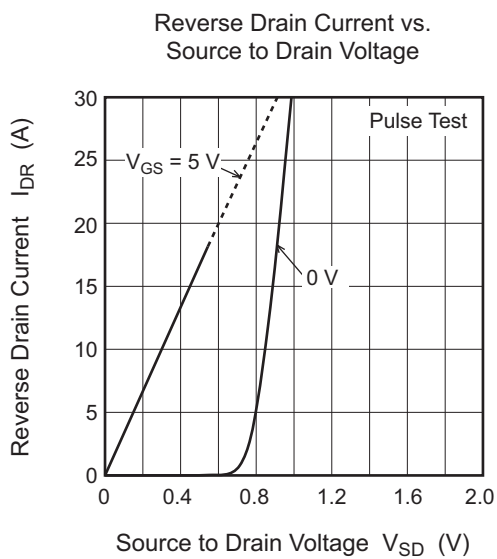
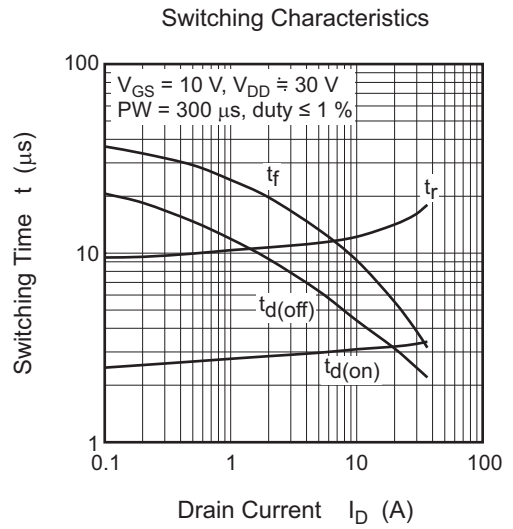
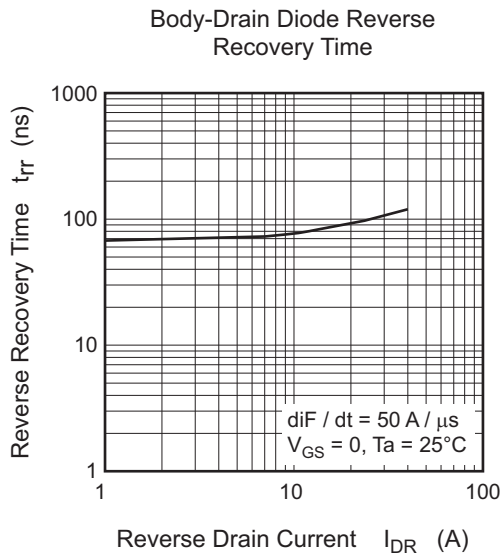
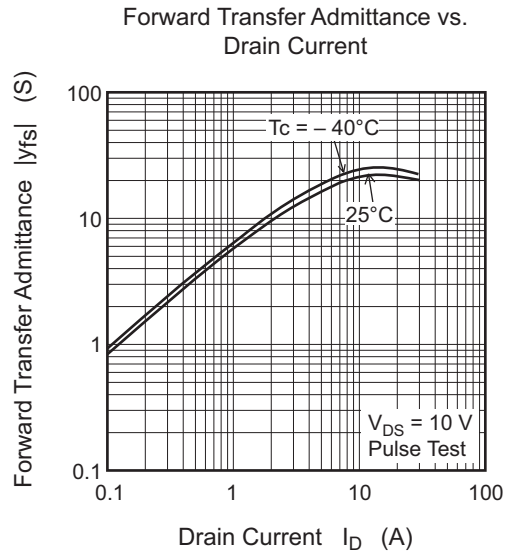
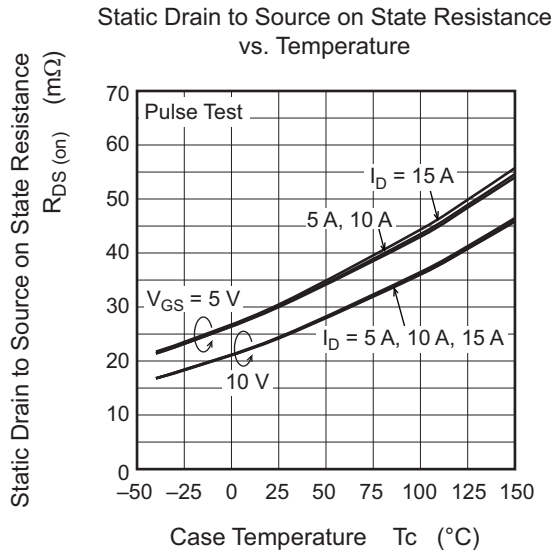
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	—	—	40	A	V _{GS} = 3.5 V, V _{DS} = 10 V ^{Note 5}
	I _{D2}	—	—	10	mA	V _{GS} = 1.2 V, V _{DS} = 10 V
	I _{D3}	34	—	—	A	V _{GS} = 5 V, V _{DS} = 10 V ^{Note 5} T _c ≤ 80°C
	I _{D4}	34	—	—	A	V _{GS} = 4.5 V, V _{DS} = 10 V ^{Note 5} T _c ≤ 80°C
Drain to source breakdown voltage	V _{(BR)DSS}	40	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	16	—	—	V	I _G = 800 μA, V _{DS} = 0
	V _{(BR)GSS}	-2.5	—	—	V	I _G = -100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	100	μA	V _{GS} = 8 V, V _{DS} = 0
	I _{GSS2}	—	—	50	μA	V _{GS} = 3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	1	μA	V _{GS} = 1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	-100	μA	V _{GS} = -2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	0.8	—	mA	V _{GS} = 8 V, V _{DS} = 0
	I _{GS(OP)2}	—	0.35	—	mA	V _{GS} = 3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 32 V, V _{GS} = 0, T _c = 110°C
Gate to source cutoff voltage	V _{GS(off)}	1.1	—	2.1	V	V _{DS} = 10 V, I _D = 1 mA
Forward transfer admittance	y _{fs}	12	21.9	—	S	I _D = 15 A, V _{DS} = 10 V ^{Note 5}
Static drain to source on state resistance	R _{DS(on)}	—	29.9	43	mΩ	I _D = 15 A, V _{GS} = 5 V ^{Note 5}
	R _{DS(on)}	—	23.8	37	mΩ	I _D = 15 A, V _{GS} = 10 V ^{Note 5}
Output capacitance	C _{oss}	—	416	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	3	—	μs	V _{GS} = 10 V, I _D = 15 A, R _L = 2 Ω
Rise time	t _r	—	12.8	—	μs	
Turn-off delay time	t _{d(off)}	—	4	—	μs	
Fall time	t _f	—	9.9	—	μs	
Body-drain diode forward voltage	V _{DF}	—	0.96	—	V	
Body-drain diode reverse recovery time	t _{rr}	—	109	—	ns	I _F = 30 A, V _{GS} = 0 di _F /dt = 50 A/μs
Over load shut down operation time ^{Note 6}	t _{os1}	—	0.26	—	ms	V _{GS} = 5 V, V _{DD} = 16 V

Notes: 5. Pulse test

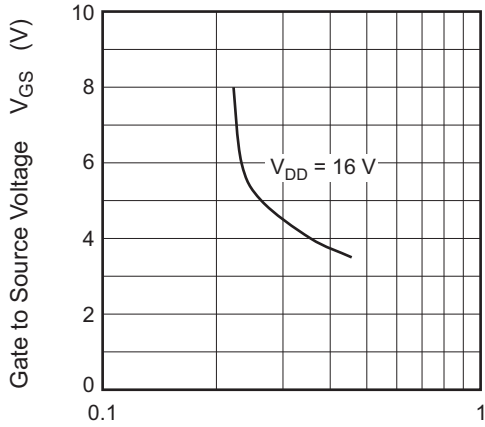
6. Including the junction temperature rise of the over loaded condition.

Main Characteristics



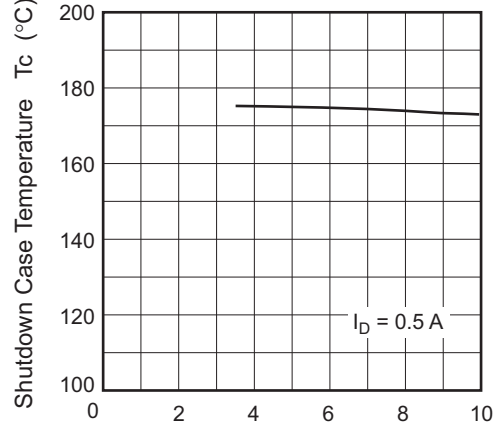


Gate to Source Voltage vs. Shutdown Time of Load-Short Test



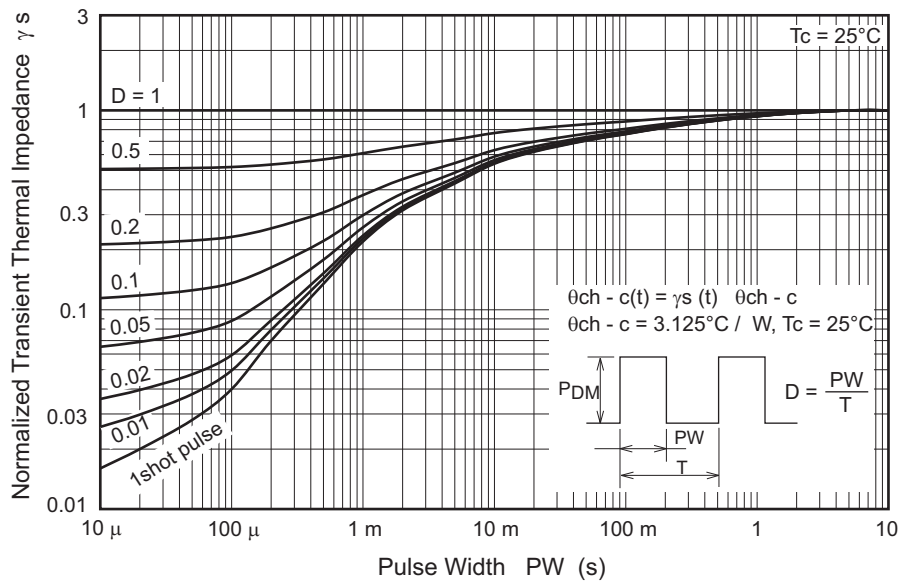
Shutdown Time of Load-Short Test PW (ms)

Shutdown Case Temperature vs. Gate to Source Voltage

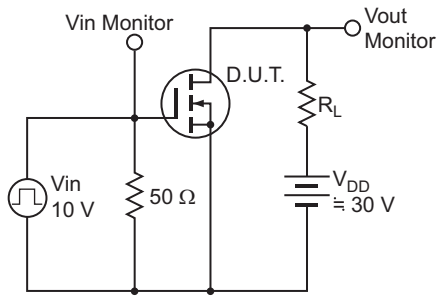


Gate to Source Voltage V_GS (V)

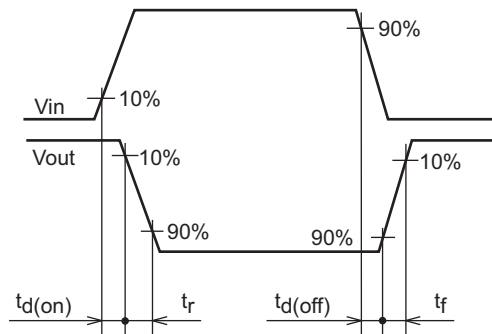
Normalized Transient Thermal Impedance vs. Pulse Width



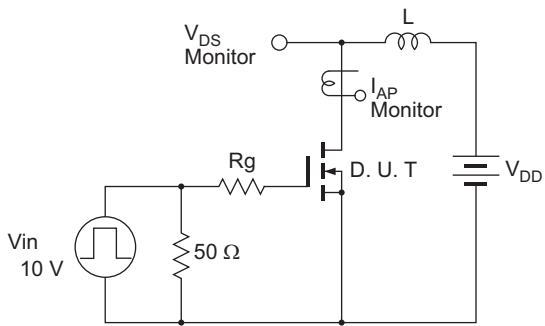
Switching Time Test Circuit



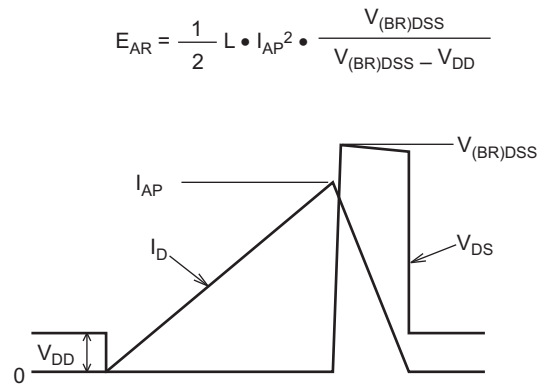
Waveform



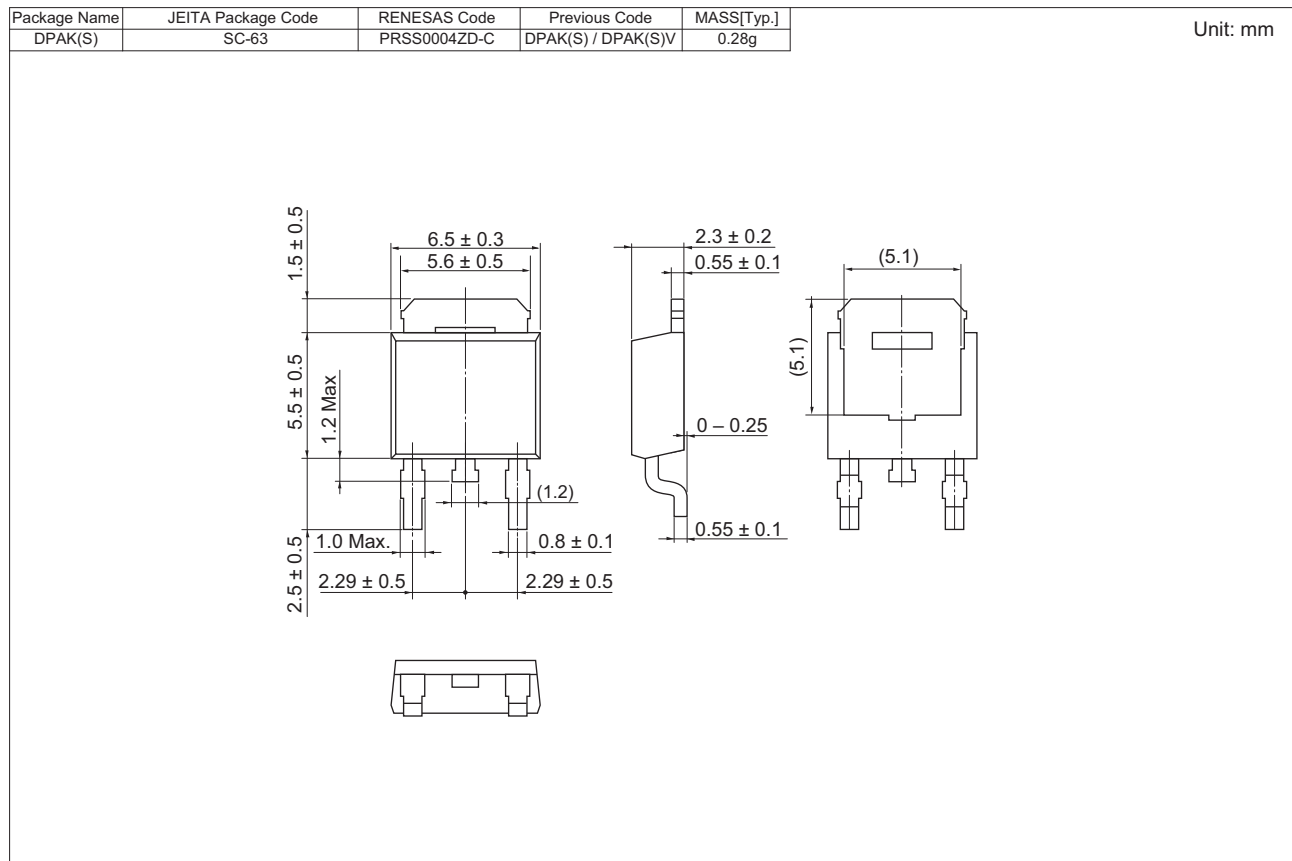
Avalanche Test Circuit



Avalanche Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJF0411JPD-00-J3	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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