



**Advanced Power
Electronics Corp.**

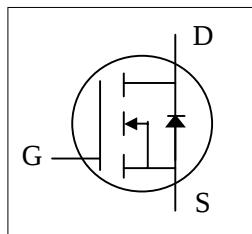
AP9970GW-HF

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Simple Drive Requirement
- ▼ Lower On-resistance
- ▼ RoHS Compliant & Halogen-Free

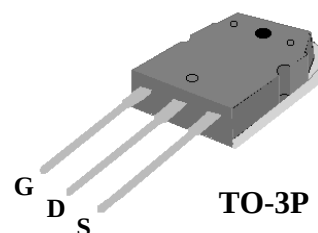


BV_{DSS}	60V
$R_{DS(ON)}$	3.2m Ω
I_D^3	240A

Description

AP9970 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-3P package is widely preferred for commercial-industrial applications. The device is suited for switch mode power supplies, DC-AC converters and high current high speed switching circuits.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Drain Current (Chip)	240	A
$I_D@T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	120	A
$I_D@T_C=100^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	120	A
I_{DM}	Pulsed Drain Current ¹	480	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	375	W
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	0.4	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	40	$^\circ\text{C}/\text{W}$



AP9970GW-HF

Electrical Characteristics@T_J=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =60A	-	-	3.2	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =60A	-	105	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =60V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =40A	-	125	200	nC
Q _{gs}	Gate-Source Charge	V _{DS} =48V	-	12	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	74	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =30V	-	65	-	ns
t _r	Rise Time	I _D =40A	-	240	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =25Ω	-	250	-	ns
t _f	Fall Time	V _{GS} =10V	-	350	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	4100	6560	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	1320	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	650	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =60A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time ²	I _S =10A, V _{GS} =0V	-	75	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	175	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Package limitation current is 120A.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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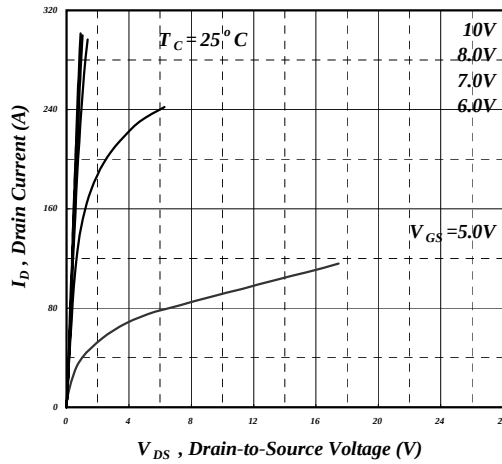


Fig 1. Typical Output Characteristics

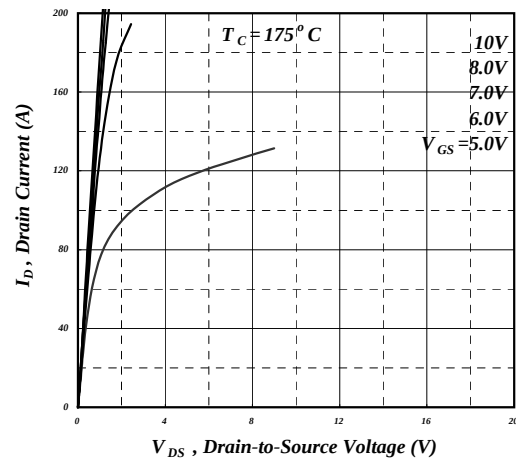


Fig 2. Typical Output Characteristics

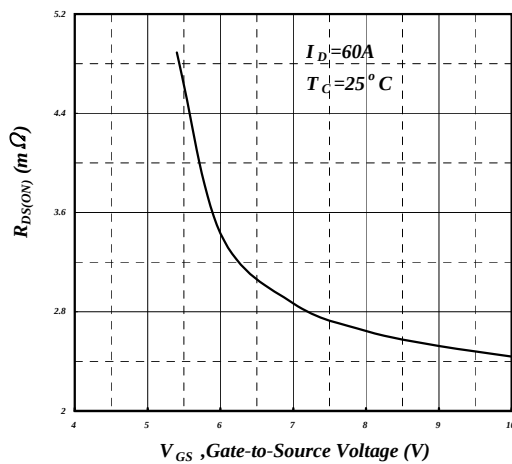


Fig 3. On-Resistance v.s. Gate Voltage

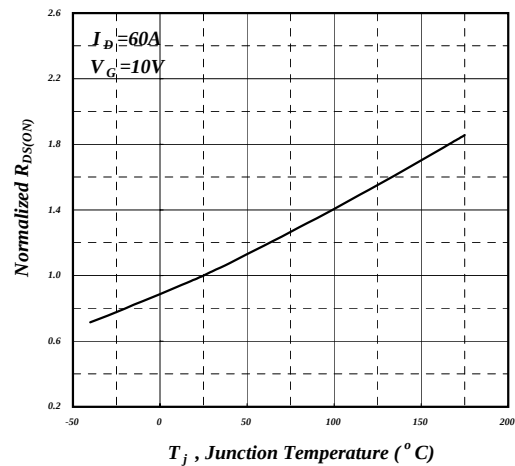


Fig 4. Normalized On-Resistance v.s. Junction Temperature

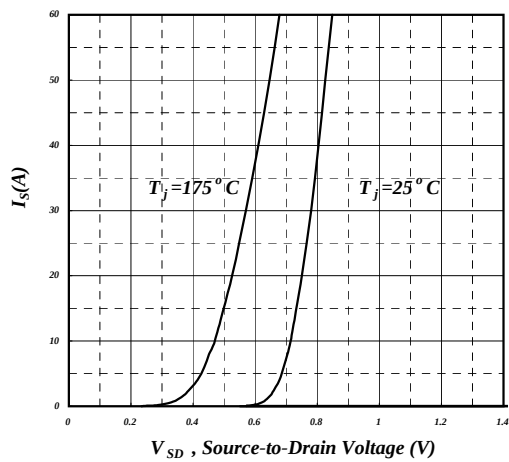


Fig 5. Forward Characteristic of Reverse Diode

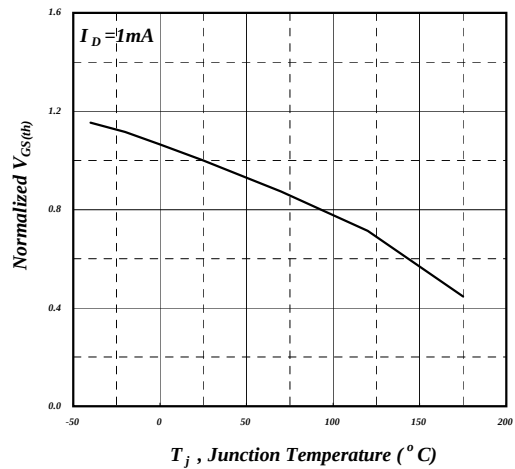


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

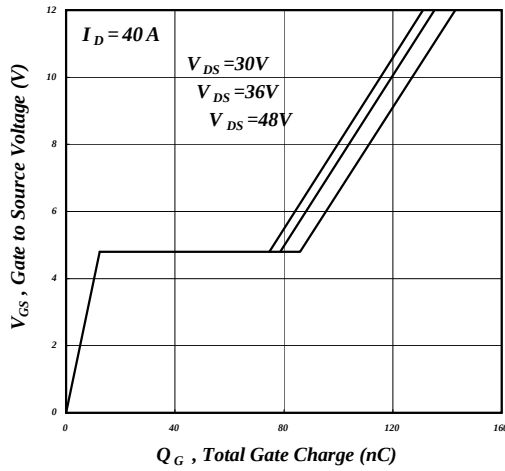


Fig 7. Gate Charge Characteristics

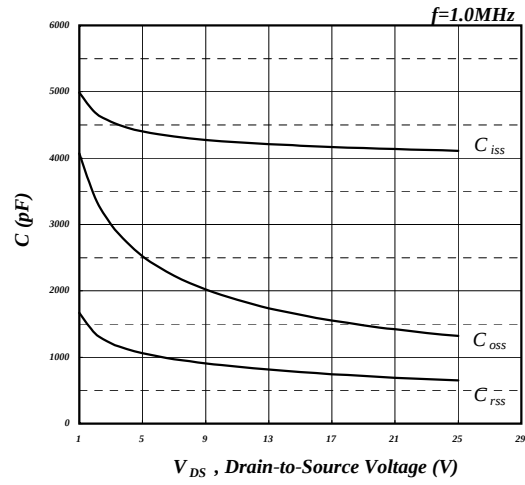


Fig 8. Typical Capacitance Characteristics

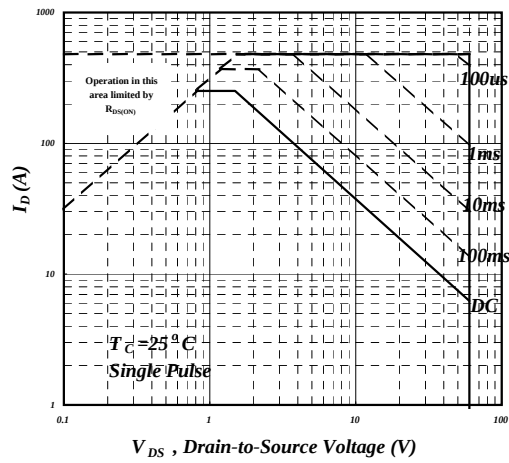


Fig 9. Maximum Safe Operating Area

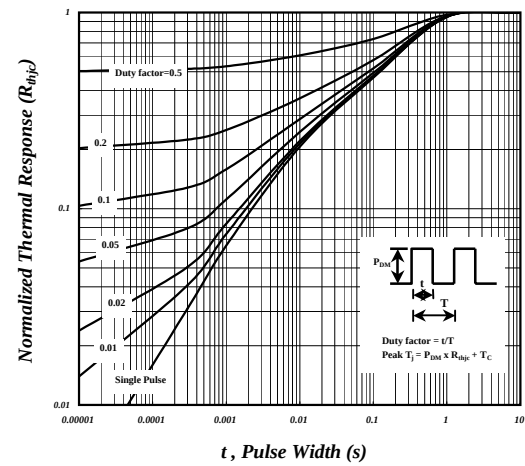


Fig 10. Effective Transient Thermal Impedance

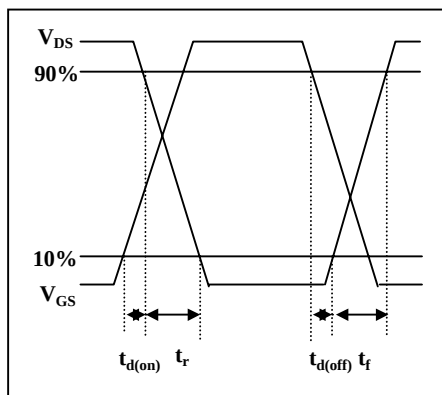


Fig 11. Switching Time Waveform

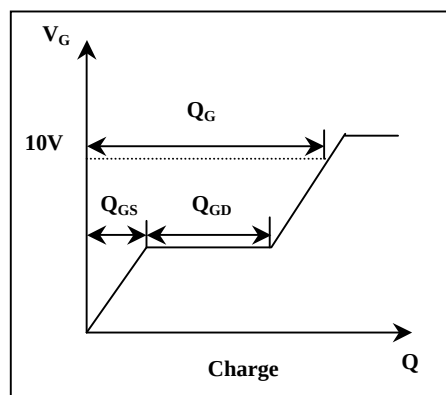


Fig 12. Gate Charge Waveform



MARKING INFORMATION

