PD-94283E

International
IOR Rectifier

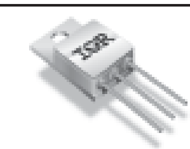
IRHMS597160
JANSR2N7550T1

RADIATION HARDENED POWER MOSFET THRU-HOLE (Low-Ohmic TO-254AA)

100V, P-CHANNEL
REF: MIL-PRF-19500/713
R5™ TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number
IRHMS597160	100K Rads (Si)	0.05Ω	-45A	JANSR2N7550T1
IRHMS593160	300K Rads (Si)	0.05Ω	-45A	JANSF2N7550T1



Low-Ohmic
TO-254AA

International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm^2)).The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Ratings
- Dynamic dv/dt Ratings
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electically Isolated
- Ceramic Eyelets
- Light Weight
- High Electrical Conductive Package

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = -12V, T_C=25°C	Continuous Drain Current	-45	A
I_D @ V_{GS} = -12V, T_C=100°C	Continuous Drain Current	-28.5	
I_{DM}	Pulsed Drain Current ①	-180	
P_D @ T_C = 25°C	Max. Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	480	mJ
I_{AR}	Avalanche Current ①	-45	A
E_{AR}	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-6.0	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	
	Weight	9.3 (Typical)	g

For footnotes refer to the last page

12/13/07

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.13	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.05	Ω	V_{GS} = -12V, I_D = -28.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
g_{fs}	Forward Transconductance	24	—	—	S	V_{DS} > -15V, I_{DS} = -28.5A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-10	µA	V_{DS}= -80V ,V_{GS}=0V
		—	—	-25		V_{DS} = -80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	170	nC	V_{GS} =-12V, I_D = -45A
Q_{gs}	Gate-to-Source Charge	—	—	65		V_{DS} = -50V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	30		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = -50V, I_D = -45A
t_r	Rise Time	—	—	100		V_{GS} =-12V, R_G = 1.2Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		
t_f	Fall Time	—	—	100		
$L_S + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C_{iss}	Input Capacitance	—	6110	—	pF	V_{GS} = 0V, V_{DS} = -25V
C_{oss}	Output Capacitance	—	1574	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	115	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-45	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-180		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_j = 25°C, I_S = -45A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	200	ns	T_j = 25°C, I_F =-45A, di/dt ≤ -100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	1.6	µC	V_{DD} ≤ -50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	0.6	°C/W	
R_{thCS}	Case-to-Sink	—	0.21	—		
R_{thJA}	Junction-to-Ambient	—	—	48		Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si)[1]		300KRads(Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0		V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V_{GS} =-20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		V_{GS} = 20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	—	-10	µA	V_{DS} = -80V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.05	—	0.05	Ω	V_{GS} = -12V, I_D =-28.5A
V_{SD}	Diode Forward Voltage ④	—	-5.0	—	-5.0	V	V_{GS} = 0V, I_S = -45A

1. Part number IRHMS597160 (JANSR2N7550T1)
2. Part number IRHMS593160 (JANSF2N7550T1)

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V)					
				@VGS=0V	@VGS=5V	@VGS=10V	@VGS=15V	@VGS=17.5V	@VGS=20V
Br	37.9	252.6	33.1	-100	-100	-100	-100	-100	-100
I	59.7	314	30.5	-100	-100	-100	-100	-75	-25
Au	82.3	350	28.4	-100	-100	-100	-30	—	—

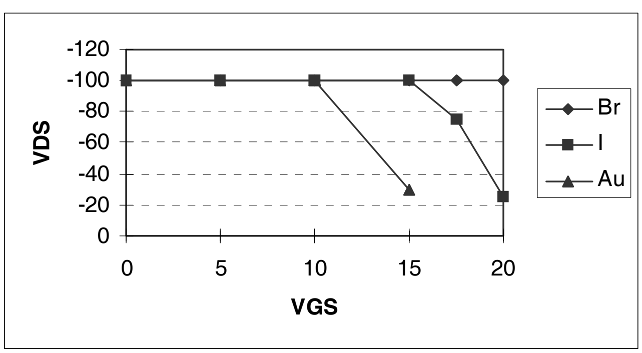


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

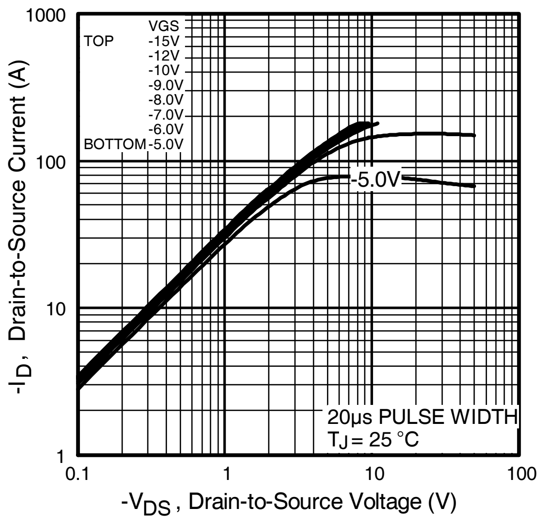


Fig 1. Typical Output Characteristics

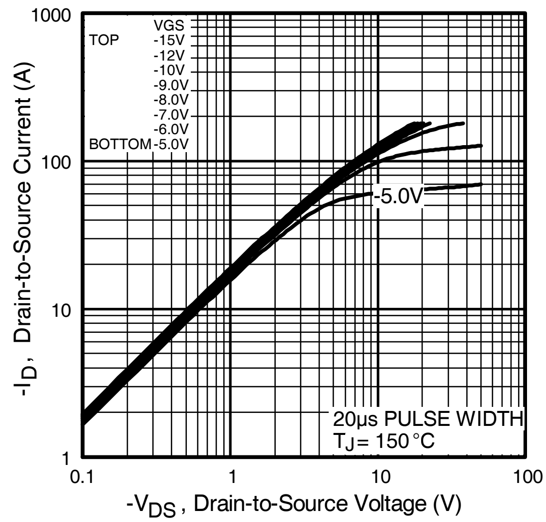


Fig 2. Typical Output Characteristics

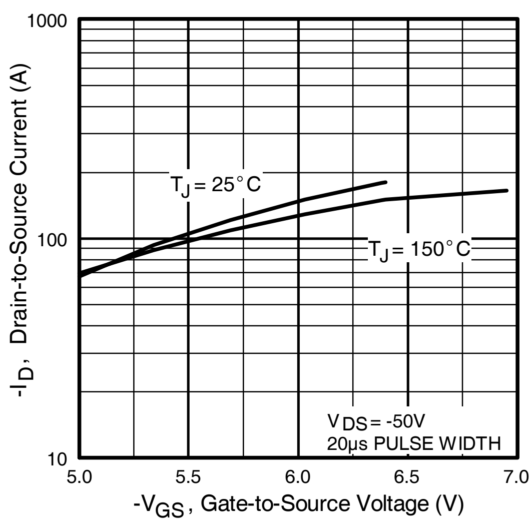


Fig 3. Typical Transfer Characteristics

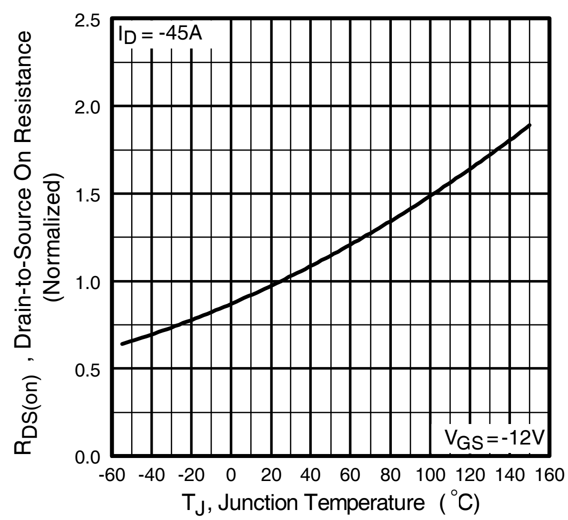


Fig 4. Normalized On-Resistance Vs. Temperature

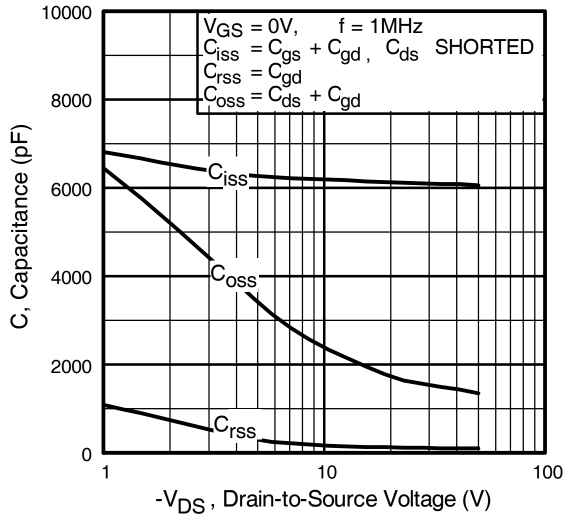


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

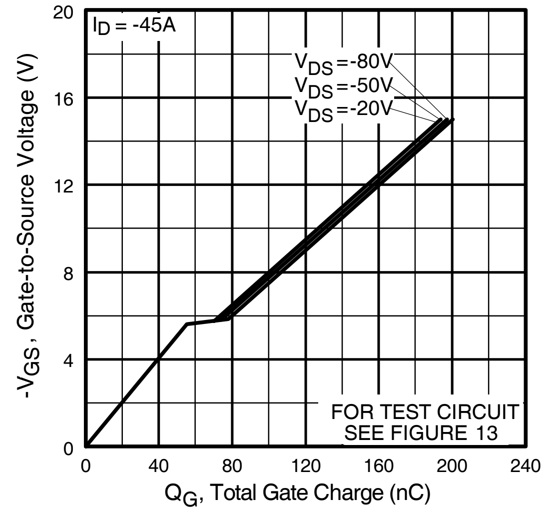


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

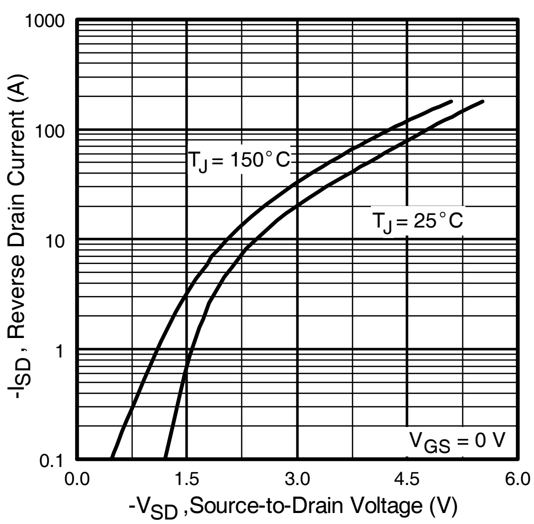


Fig 7. Typical Source-Drain Diode Forward Voltage

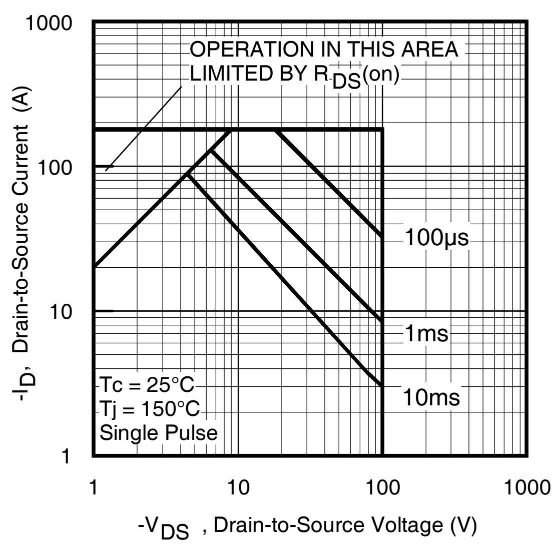


Fig 8. Maximum Safe Operating Area

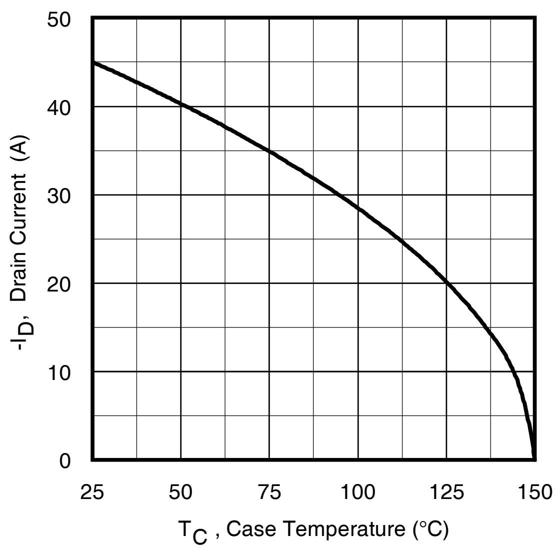


Fig 9. Maximum Drain Current Vs. Case Temperature

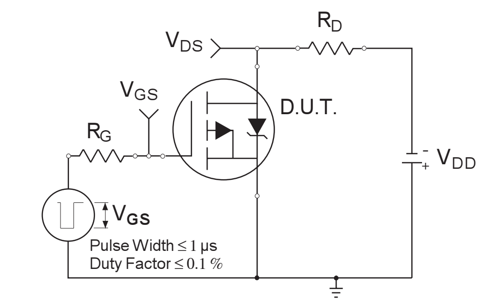


Fig 10a. Switching Time Test Circuit

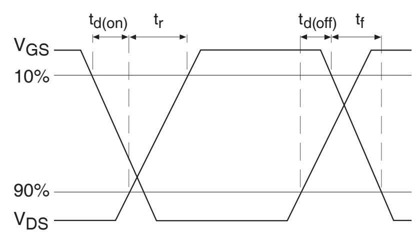


Fig 10b. Switching Time Waveforms

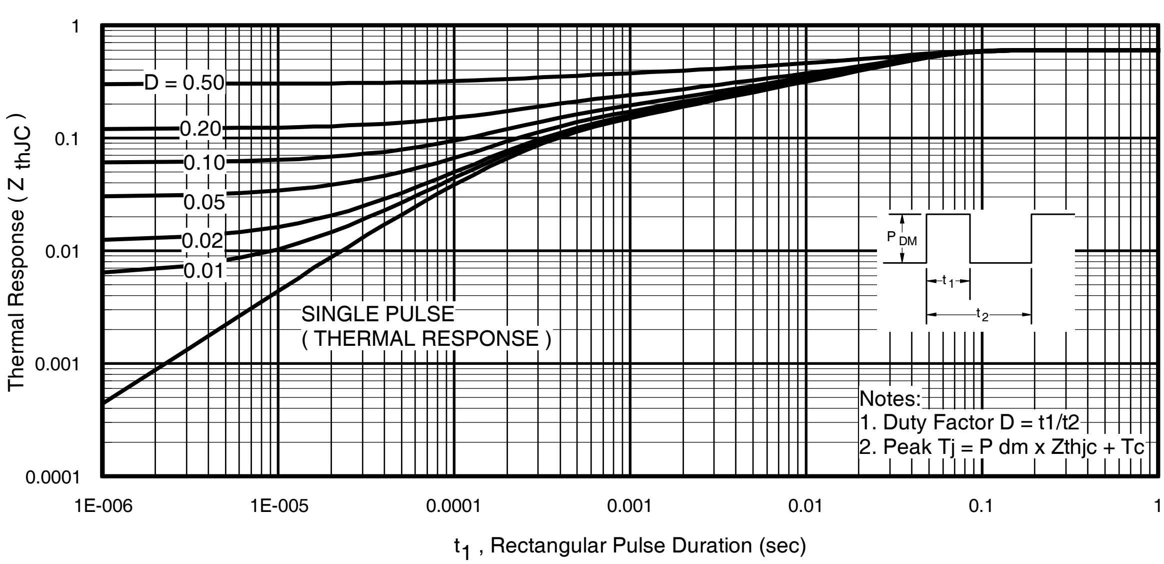


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

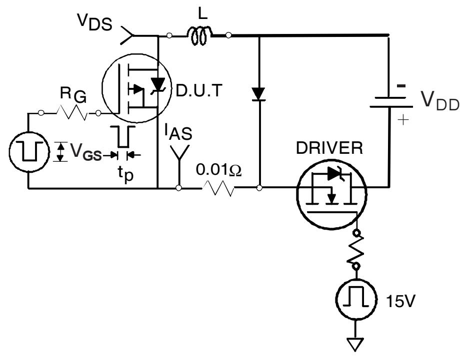


Fig 12a. Unclamped Inductive Test Circuit

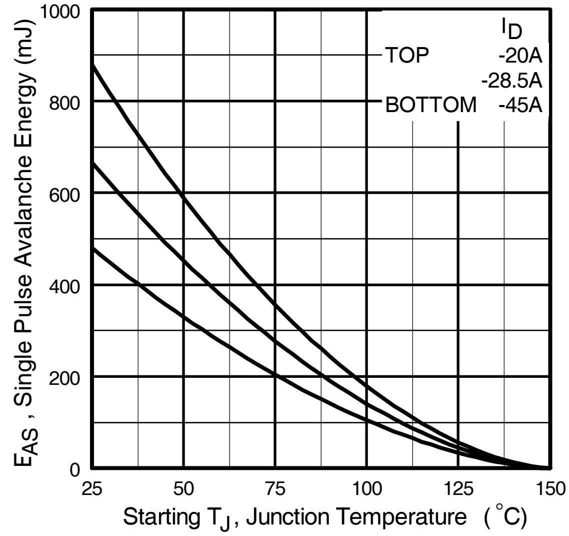


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

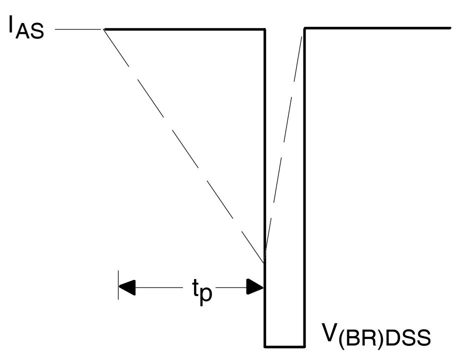


Fig 12b. Unclamped Inductive Waveforms

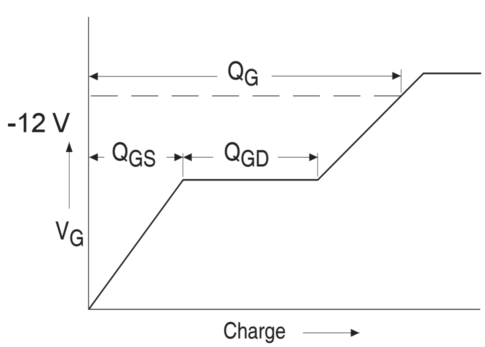


Fig 13a. Basic Gate Charge Waveform

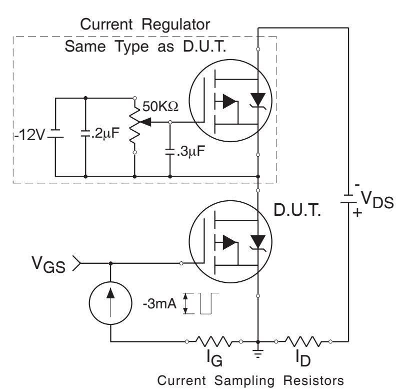


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -50V, starting T_J = 25°C, L=0.48mH Peak I_L = -45A, V_{GS} = -12V

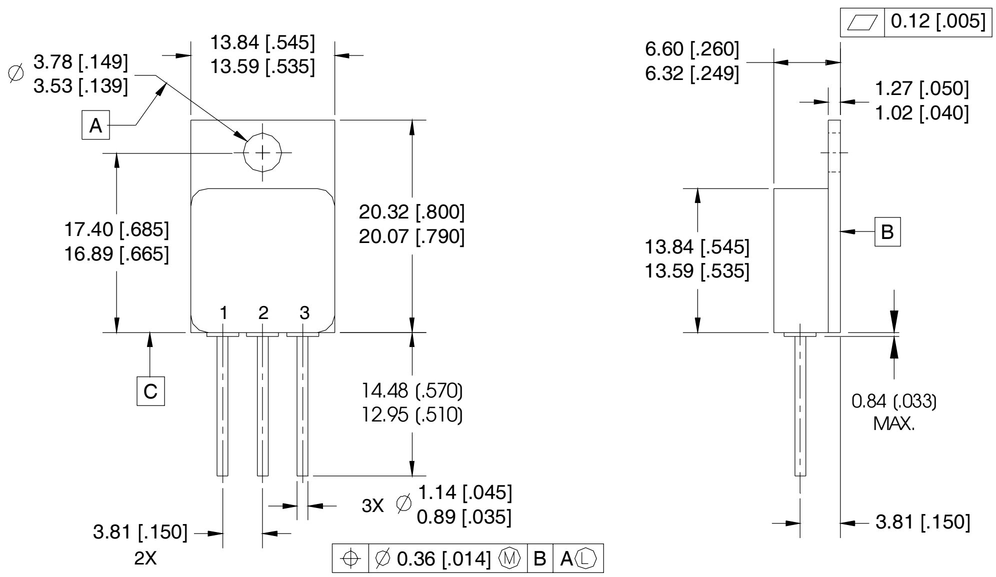
③ $I_{SD} \leq$ -45A, di/dt $\leq$ -365A/µs, $V_{DD} \leq$ -100V, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300µs; Duty Cycle $\leq$ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** -12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** -80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — Low-Omic TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

1 = DRAIN
2 = SOURCE
3 = GATE

CAUTION

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

International IOR Rectifier

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