SY10

Date: August 30, 2002

• INTRODUCTION

The SY10 - an accurate time and frequency source that had been designed as a subsystem level module. The module is designed to work within ATM, SONET, SDH, and wireless systems where synchronization is vital. The SY10 is an excellent synchronization solution for timing, with jitter and wander compliance per the specified within ITU-T Recommendations G.812/G.813 and Bellcore GR-1244-CORE. The SY10 is an enhanced version of SY01 and is designed for Stratum 3 and Stratum 3E, but also holds certain features that can make it useful for SONET Minimum Clock (SMC) or other kinds of system clocks.

• FEATURES

√ A synchronization solution for timing, jitter and wander concerns in a single module.

√ Complies with ITU-T Recommendations G.812/813 and Bellcore GR-1244-CORE for Stratum 3 and Stratum 3E applications.

√ Supports modes of operation: Locked, Holdover and Free-run.

√ Accepts reference inputs from up to six independent sources from 8KHz to 77.76MHz

√ Provides up to 3 output from 8KHz to 77.76MHz (Two user select and one fixed at 8KHz)

√ Loop filtering utilizing specific software application in the digital signal processor (DSP).

√ Continuously monitors and evaluate input reference signals.

√ Phase build-out for output clock.

√ Creates a history buffer for Holdover mode operation.

√ Alarm and status signals and messages.

√ Host interface SPI for configuring and remote monitoring.

√ Supports Master/Slave configuration of two SY10 with minimum phase error between two clocks.

√ Provides “hit-less” switching during switching between the clocks.

√ Pin compatible with 18 pins SY01 module.

√ Small dimensions of 1.82 x 1.82 x 0.7 inch. (0.60 inch with no mechanical cover)

• APPLICATION

The SY10, a Synchronous Equipment Clock (SEC), fulfills clock regeneration function for STRATUM 3 and 3E equipment for: ATM, SDH, PDH, and SONET networks. It was designed for network system manufacturers such as: Access Switches, Core Switches, Cross Connects, Digital Multiplexers-Exchangers, and SDH/SONET equipment. The unit is also suitable for PCS, WLL, and Wireless Base Stations. Wherever a Timing unit with high performance specifications is required, the SY10 can be embedded within the network system and provide all necessary frequencies and interfaces.

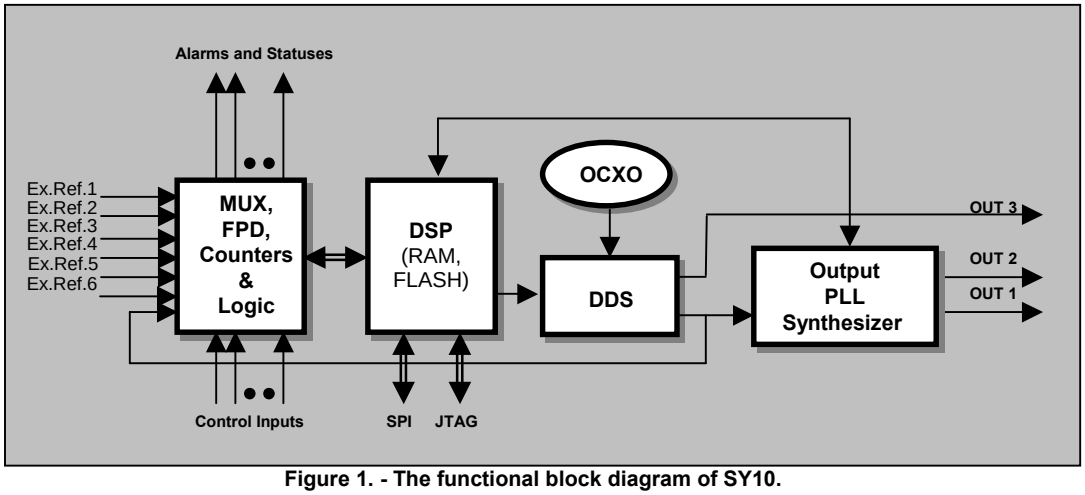


Figure 1. - The functional block diagram of SY10.

• DESCRIPTION

The SY10 synchronization module is a Digital PLL (DPLL), which utilizes application specific software in the digital signal processor (DSP). The DSP is complemented by fast hardware logic (FPGA) where all multiplexers, counters, dividers, phase detectors, output frequency converters and other control logic circuits are completely implemented. The functional block diagram with maximum configuration is shown in figure 1. The module has three phase lock loop – primary PLL, secondary and utility PLL. The primary PLL utilizes a Direct Digital Synthesis (DDS) technique combined with a high stability OCXO in order to provide an accurate and fast DPLL response and eliminates the requirement for an OCXO with high pullability. The primary loop is a low bandwidth loop that filters a major part of the wander and the jitter at the input. The output of the primary PLL is connected to the secondary PLL synthesizer that is also a DPLL but with a wider loop bandwidth. The secondary PLL loop has also another input that comes from the SEC IN pin. Depending on the master–slave mode, the secondary loop utilizes either one of the inputs. The output of secondary PLL is connected to the utility PLL that is an analog phase lock loop.

- The outputs of secondary and utility PLL provide three independent output signals.
- The SPI serial communication interface provides a flow of messages between the module and a host processor.
- The JTAG interface provides an easy access for future software upgrade re-programming without removing the module from the system.

The SY10 software provides several features such as:

- switching between the references inputs on the basis of monitoring and estimation of the input signals and internal state diagram;
- real time calculation of the filtering algorithm for jitter and wander in according to the approved standards;
- alarm, status and messaging functions using output pins and serial communication port.

For other configurations, please contact Raltron.

✓ The module operates in the following three timing modes:

Free-run
In this mode, the unit is unlocked to either of the inputs. The accuracy of the output frequencies in this mode is ±4.6ppm. Free-run mode is typically used when a master clock source is required, not valid history of data for the Holdover mode, or immediately following system power-up before network synchronization is achieved. In the Free-run Mode, the SY10 provides timing and synchronization signals that are based on the accuracy of on-board oscillators only, and are not synchronized to the reference signals.

Holdover

In this mode, the module has lost its reference inputs and is utilizing stored timing data, called history, to control the output frequency. Holdover Mode is typically used while the network synchronization is temporarily disrupted. In Holdover Mode, the SY10 provides timing, based on data from the history buffer, while unlocked to an external reference signal. The history data is determined while the device is locked to an external reference signal. The stability of the output signal in holdover mode depends primarily on the stability of on-board oscillator and environment effects where the clock is mounted. The SY10 uses an OCXO as an on-board oscillator but other types of oscillators are available.

Locked to Reference
In this mode, the output of the module is phase locked to any of input references. The output frequency tracks the selected input reference. The "Locked to Reference Modes" is typically used when a slave clock source is synchronized to the network. In these modes, the SY10 provides timing signals, which are synchronized, to one of six references inputs (REF1 to REF6). The input reference signals may have a variety of nominal frequencies, which are typically specified by the end user. When the modes are selected the unit goes through a reference evaluation, and then a frequency acquisition, and finally to phase locking.

Local Reference Oscillator

Depending on the type of clock, a local reference oscillator is selected. For example: for a Stratum 3E type of clock, the local oscillator is a high stability SC-cut OCXO that meets this standard requirements for frequency drift and jitter noise.

Input References

The SY10 module accepts six input references EX REF1 to EX REF6. End users can specify the frequencies within a range of 8 kHz to 77.76 MHz. The input reference signals are HCMOS/TTL levels with timing characteristic in accordance with Bellcore GR-1244-core 3.2.1.R3-1 or equivalent standards. Please note that the end user must specify the input frequencies at the time of order.

Monitoring and Evaluation of the Input References

Using an advanced algorithm the input references are continuously monitored and evaluated by the module. There are three techniques used in the algorithm for each of reference, presence of the reference, frequency offset during the time when the unit is phase locked to the reference, and frequency offset when the unit in not phase locked to the reference. The SY10 rejects all reference signals whose frequency accuracy is offset by more than ±13 PPM. At any given event that requires a switching in the operation mode, the timing module unit performs a reference evaluation test of the new target reference. Since such evaluation is a continuous process, the switching takes very short time (typically less then a second). Providing a successful evaluation, the unit switches to frequency and phase locking mode. On the other hand, if the reference was not qualified the unit switches to a holdover mode.

Filtering in the DPLL

The SY10 dynamically changes its loop bandwidth according to the status of the DPLL. In the primary PLL there are five stages that the DPLL goes through before phase lock mode is achieved. The first stage is frequency acquisition that takes place until the frequency becomes equal to the reference. The second stage is the phase acquisition stage that takes place until a new phase reference is acquired. The other stages are tracking stages (1, 2 and 3) (hint: the DPLL is locked and tracks the phase reference with a very low loop bandwidth). This method of three tracking stages ensures minimum locking time and minimum phase jumps and shifts during acquisition or transition. It also provides phase build-out during switching or rearrangement. The secondary PLL operates similarly to the primary PLL with an exception of a wider bandwidth (hint: it has only three stages) – the first is frequency acquisition, second is phase acquisition and third one is tracking mode. Please see detail in state diagram.

History Buffer for HOLDOVER mode

Frequency and timing data is continuously collected in the history buffer during the time when the unit is locked to any of the input references. The history buffer is actually a circular buffer in memory that keeps valid data for HOLDOVER mode during the last 90 seconds of operation. When the SY10 enters to HOLDOVER mode the data

from the buffer is validated and processed. The history buffer can be cleared by writing one to bit HLRST in CFG2 register.

Output Signals

The SY10 module provides three output signals OUT, OPT OUT1 and OPT OUT2. The outputs are generated by the internal oscillators VCXO and scaled by the output frequency converters. Two VCXO oscillators can be used per module providing two independent frequency types and the third one (OPT OUT2) is derived from one of them. The performance of the module significantly depends on the output oscillator and special care is taken to define their specifications. The used VCXO are high quality crystal oscillators with very low output jitter. The frequency of the oscillator is specified according to the network application where the SY10 will be used. The frequency converters divide signal from the oscillator to the specified frequencies.

Indications

The SY10 provides detailed monitoring and indication of operation of the unit. Two types of monitoring and status indicating are provided:

- Visual indication: Using ten on board color mounted LED's that indicate the operating mode of the SY10. The LED indicators are mainly placed for system troubleshooting, and testing.

- Electronic indications: Using ten digital outputs that report status and alarms from the SY10. These alarms are mainly used for communication between the module and network equipment.

The internal LED indicators are:

Signal	LED
Holdover	super light red LED, ON when the module is in holdover mode.
REF1	green LED, ON when the module is locked to reference 1.
REF2	green LED, ON when the module is locked to reference 2.
REF3:.	green LED, ON when the module is locked to reference 3
REF4:	green LED, ON when the module is locked to reference 4.
REF5	green LED, ON when the module is locked to reference 5.
REF6	green LED, ON when the module is locked to reference 6.
FREERUN	orange LED, ON when the unit is in free running mode.
UNLOCK	red LED, ON when the module is not locked to the selected reference signal.
ALARM	red LED, ON when there is an alarm in the module

Control

Several controls pins are available for the user to control the operation of the SY10 Primary PLL. The three external inputs CNT1, CNT2 and CNT3 provide the feature to change the state of operation. Below, the truth table shows behavior of the SY10 module according to the control inputs states.

CNT3	CNT2	CNT1	MODE OF OPERATION
0	0	0	Free-run
0	0	1	Locked to REF1
0	1	0	Locked to REF2
0	1	1	Holdover
1	0	0	Locked to REF3
1	0	1	Locked to REF4
1	1	0	Locked to REF5
1	1	1	Locked to REF6

To change the operation of Secondary PLL (Master-Slave) can be change using MS/FR control pin.

MS/FR†	MODE OF OPERATION
1 (or open)	Master (default)
0	Slave

†see explanation about MS/FR below.

The state of operation can be set and changed also using serial communication port, please see below.

The SY10 State Machine – Primary PLL

The state machine of SY10 module can be controlled using one of two interfaces:

1) three external control pins CNT1, CNT2 and CNT3.
2) setting bits (CON0, CON1, CON2 and CON3) in CFG1 register using serial peripheral interface (SPI).

After the reset the module is set to use three external control pins for control function but user can change it by setting bit UI in register CFG1. By setting the UI bit to 1 the module ignores states of the control pins and use bits in CFG1 register for state engine control. On the figure below is shown simplified stated diagram of SY10 module.

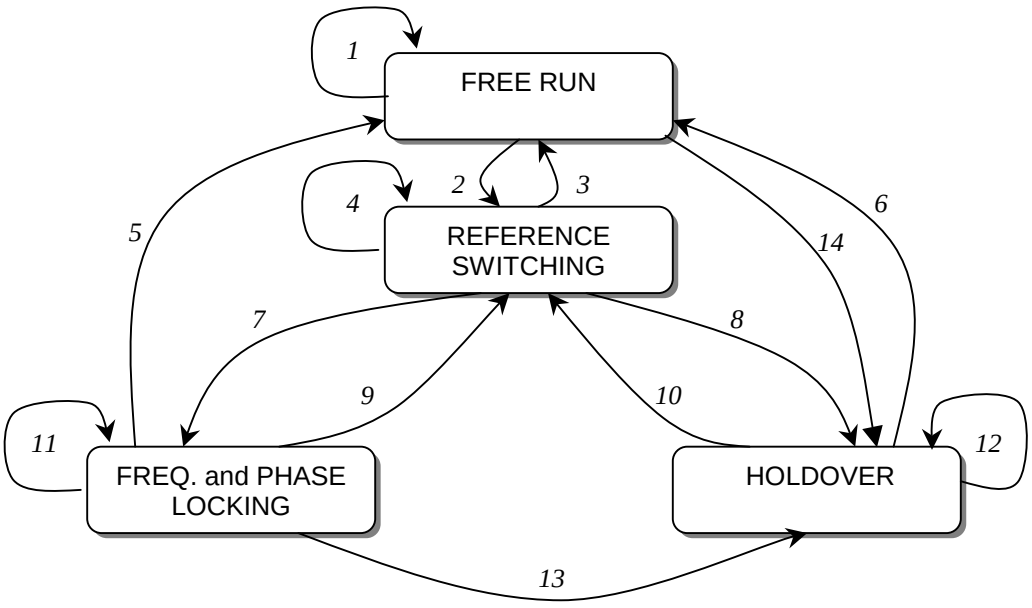


Figure 2 – The SY10 state diagram – Primary PLL.

1) (FREERUN)
The path 1 runs until control signals (CNT1,2,3 pins or CON0,1,2,3 bits in CFG1 register) are set to zero or there is no valid history available on the acquisition buffer for the holdover.

2) (FREERUN_ REFERENCE_SWITCHING)
The path 2 runs when there was any change at control signals.

3) (REFERENCE_SWITCHING_FREERUN)
The path 3 runs when the control signals were changed to zero – the free-run mode was selected.

4) (REFERENCE_SWITCHING)
The path 4 runs until appropriate reference was selected. If the unit is in Auto Switching mode (bit AUTOEN in CFG2 register set to 1) the module will switch in the following conditions:

1) if a reference that was selected by control signals,
2) if the selected reference is not available it will switch based on Priority Table (registers PR1 – PR4).
3) if any of the references are not available it will go to holdover (path 8)

If the unit is in Manual Switching mode (bit AUTOEN in CFG2 register set to 0) the module will switch in following conditions:

1) if a reference that was selected by control signals,
2) if the selected reference is not available it will go to holdover (path 8)

5) (FREQ&PHASE_LOCKING_FREERUN)
The path 5 runs when the control signals were changed to zero – the free-run mode was selected.

6) (HOLDOVER_FREERUN)
The path 6 runs when the control signasl were changed to zero – the free-run mode was selected or there is no valid history available on the acquisition buffer for the holdover.

7) (REFERENCE_SWITCHING_FREQ&PHASE_LOCKING)
The path 7 runs when the reference switching was successfully finished – a reference was qualified and no changes at control signals.

8) (REFERENCE_SWITCHING_HOLDOVER)
The path 8 runs if the following conditions:

1) if control signals were changed to one (0011) – the holdover mode was selected.
2) if the module is in Auto Switching mode (bit AUTOEN in CFG2 register set to 1) the module will switch to the holdover if none of the reference are available.
3) if the module is in Manual Switching mode (bit AUTOEN in CFG2 register set to 0) and selected reference was not qualified or reference was lost during process of evaluation.

9) (FREQ&PHASE_LOCKING_REFERENCE_SWITCHING)
The path 9 runs in the following conditions:

1) if another reference was selected changing control signals.
2) if the module is in Auto Switching mode (bit AUTOEN in CFG2 register set to 1) the module will switch to the reference switching if at least one of the references is available and when the currently selected reference is failing.
3) if the unit was set to operate in Revertive mode (bit REVEN in CFG2 register is set to 1) and previously lost reference is back the module will switch to reuse the same reference.

10) (HOLDOVER_ REFERENCE_SWITCHING)
The path 10 runs in the following conditions:

1) current selected reference was reacquired or if the other reference was selected changing control signals.
2) if the unit was set to operate in Revertive mode (bit REVEN in CFG2 register is set to 1) and previously lost reference is back the module will switch to reuse the same reference.

11) (FREQ&PHASE_LOCKING)
The path 11 runs until the frequency acquisition or the phase locking is in progress with no changes at control pins. The module goes through a few intermediate states in order to accomplish phase tracking. There are three basic intermediate steps that include frequency acquiring, phase acquisition and tracking. Tracking can have additional steps depending of the bandwidth to be achieved.

12) (HOLDOVER)
The path 12 runs until the holdover mode is in progress with no changes at control signals.

13) (FREQ&PHASE_LOCKING_ HOLDOVER)
The path 13 runs in following conditions:

1) if the used reference was lost or was detected bad,
2) if the control signals were changed to one (0011) – the holdover mode was selected.

14) (FREERUN_HOLDOVER)
The path 14 runs only if the control signals were changed to one (0011) and valid history buffer for holdover operation is available – the holdover mode was selected.

SY10 Master-Slave Operation – Secondary PLL

In systems where clock redundancy is required it is possible to connect two SY10 – such connection shown at the figure below. The module has two pins dedicated for this feature – MS/FR and SEC IN. The MS/FR control input selects if the module will operate as master (logic high) or slave in the system. The SEC IN is input for signal that comes from another clock module. In the system always clock "one" operates as master and the second one as slave clock. When operating as a slave the output of SY10 also tracks the master so it provides minimum phase difference between the two clocks. This is very useful as it makes easier "hitless" switching of references. The Master-Slave control can also be done using SPI communication setting the bit MS in register CFGREG1. Please see more in Memory Mapped Registers section. The typical Master-Slave connection block diagram is show on figure below.

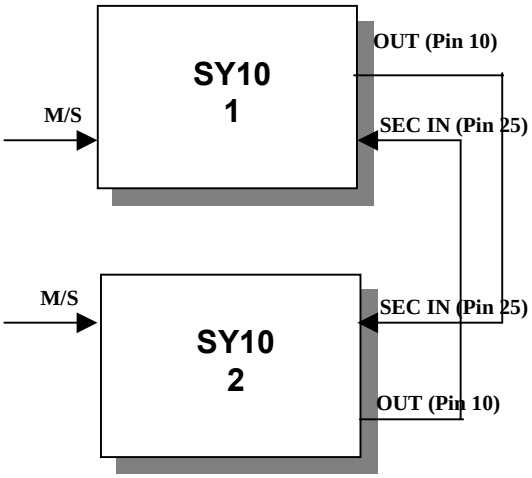


Figure 3. - The Master – Slave connection of two SY10.

The state machine of SY10 Master –Slave operation module can be controlled using one of two interfaces:

3) one external control pin MS/FR.
4) setting MS bit in CFG1 register using serial peripheral interface (SPI).

After the reset the module is set to use the external control pin for control function but user can change it by setting bit UI in register CFG1. By setting the UI bit to 1 the module ignores states of the control pins and use bits in CFG1 register for state engine control. On the figure below is shown simplified stated diagram of SY10 Master –Slave operation.

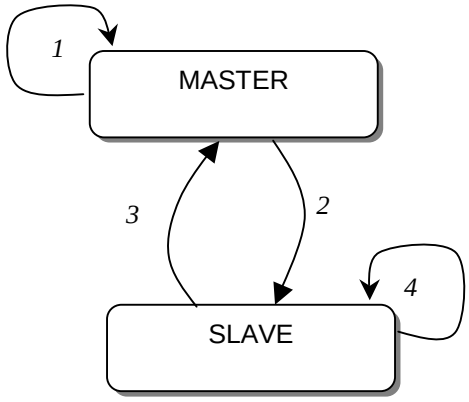


Figure 4. - The SY10 Master – Slave state diagram

1. (MASTER)
The path 1 runs until control signals MS/FR† is set to 1 (or MS bit in CFG1 register is set to 0) or there is no valid signal at SEC IN pin. No valid signal means either not present or not within frequency offset window.

2. (MASTER_SLAVE)
The path 2 runs when there was a change at MS/FR control signal from 1 to 0 (or in case of MS bit in CFGREG1 from 0 to 1) and there is valid signal at SEC IN pin.

3. (SLAVE_MASTER)
The path 3 runs when there was a change at MS/FR control signal from 0 to 1 (or in case of MS bit in CFGREG1 from 1 to 0) or there is no valid signal at SEC IN pin (signal disappeared).

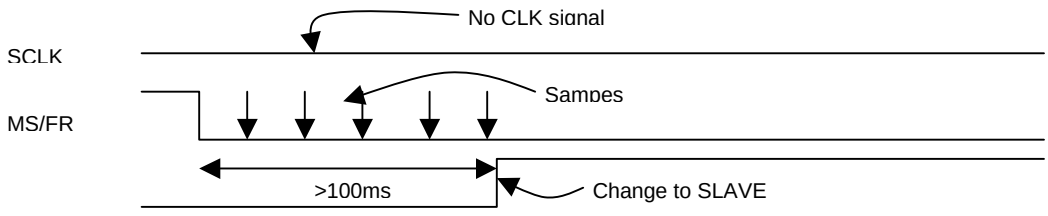
4. (SLAVE)
The path 4 runs until control signal MS/FR is set to 0 (or MS bit in CFG1 register is set to 1) and there is valid signal at SEC IN pin.

†see explanation below!

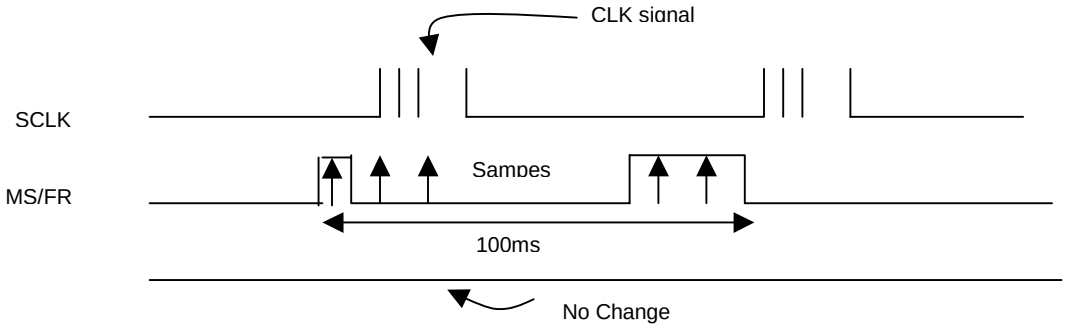
MS/FR shared pin input

Since the MS/FR control input pin shares the function special caution should be taken to drive it. The signal at MS/FR signal is sampled and processed by internal software and decisions are made using following:

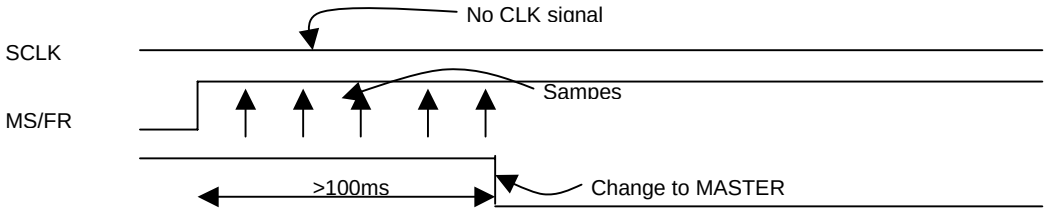
1) To change status of Secondary PLL from Master to Slave using MS/FR the user have to change from 1 to 0 and keep the pin logic low for period longer then 100ms not communicating through SPI. If within that period of time MS/FR signal does not change level (0) and there is no clock signal at SCLK pin (no changing at SCLK for SPI communication) the operation will be changed from Master to Slave.



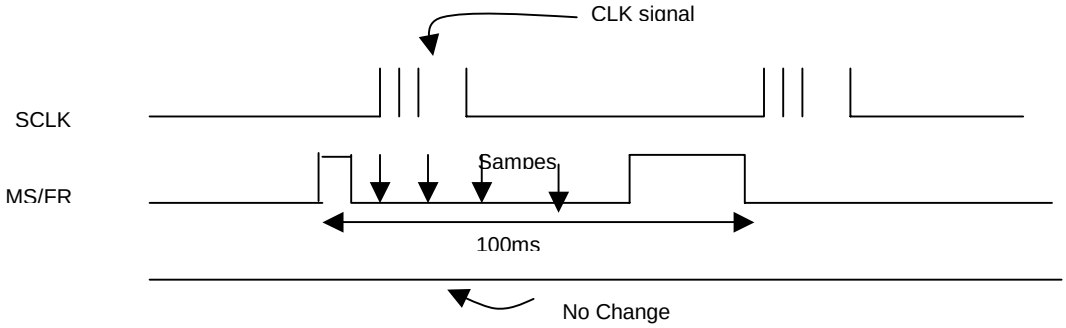
2) To maintain Slave mode while still communicating through SPI signal MS/FR should be set high prior SCLK for no more then 100ms at any given time. Please see timing constrains for SPI communication.



3) To change status of Secondary PLL from Slave to Master the signal MS/FR should be set to high (1) for period longer then 100ms not communicating through SPI.



4) To maintain Master mode while still communicating through SPI signal MS/FR should be set low during SCLK for no more then 100ms at any given time. Please see timing constrains for SPI communication.



Changing mode of operation can be done easier using SPI communication interface – please see next paragraph. For other configuration please contact Raltron Electronics Corp.

- **SERIAL COMMUNICATION BUS – SPI**

The module can be configured, controlled and monitored using an on board serial communication port – SPI provided on the SY10. There are four pins available for this features SCLK, MS/FR, DIN and DOUT. The DIN and DOUT are ports used to transfer command and data in and out of the module. The SCLK is input used to clock the data transfer in and out of the module and MS/FR is shared pin that provides frame synch signal. The SY10 operates only as a slave device on SPI bus so the transfer of the data or command should be initiated by a micro-controller. The micro-controller can read or write to configuration registers and read only from status registers mapped internally into the SY10. Optionally the interface can be implemented in SPI.

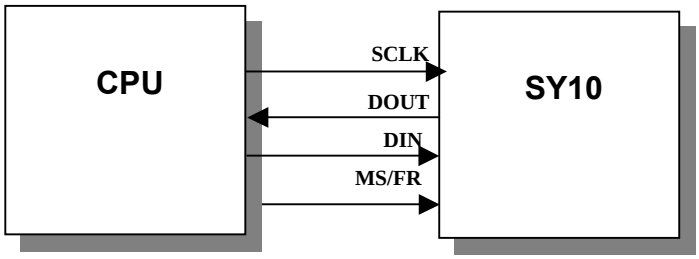


Figure 9. - The SPI serial communication

Communication Protocol for SPI

The interface is synchronous peripheral interface (SPI), the master must to provide clock signal and initiate the communication cycles. There are read and write cycles and each communication cycle that consists of 16 clocks (8+8 bits). Data is latched every rising edge of clock input from most significant bit. The maximal allowed frequency for SCLK is 10MHz - t_{clk}.

Write data cycle

The master sends to the module two bytes (2 x 8bits). First byte is always command byte. The second byte is the data byte contains information to write.

Command byte data format:

7(MSB)	6	5	4	3	2	1	0(LSB)
R/W	X	A5	A4	A3	A2	A1	A0

- A5…A0 - Module register address please see the table 1.
- R/W - Read (1) or Write (0) bit.
- X – not used.

Data byte format:

7(MSB)	6	5	4	3	2	1	0(LSB)
D7	D6	D5	D4	D3	D2	D1	D0

- D7…D0 – Content to be written to the register addressed by A5:A0

Read data cycle

The master sends to the module one-command byte and receives from module information byte (see 1.1 and 1.2).

Command byte data format:

7(MSB)	6	5	4	3	2	1	0(LSB)
R/W	X	A5	A4	A3	A2	A1	A0

- A5…A0 - Module register address please see the table 1.
- R/W - Read (1) or Write (0) bit.

Data byte format:

7(MSB)	6	5	4	3	2	1	0(LSB)
D7	D6	D5	D4	D3	D2	D1	D0

- D7-D0 – Content to be read from the module addressed by A5:A0

SPI Flowchart

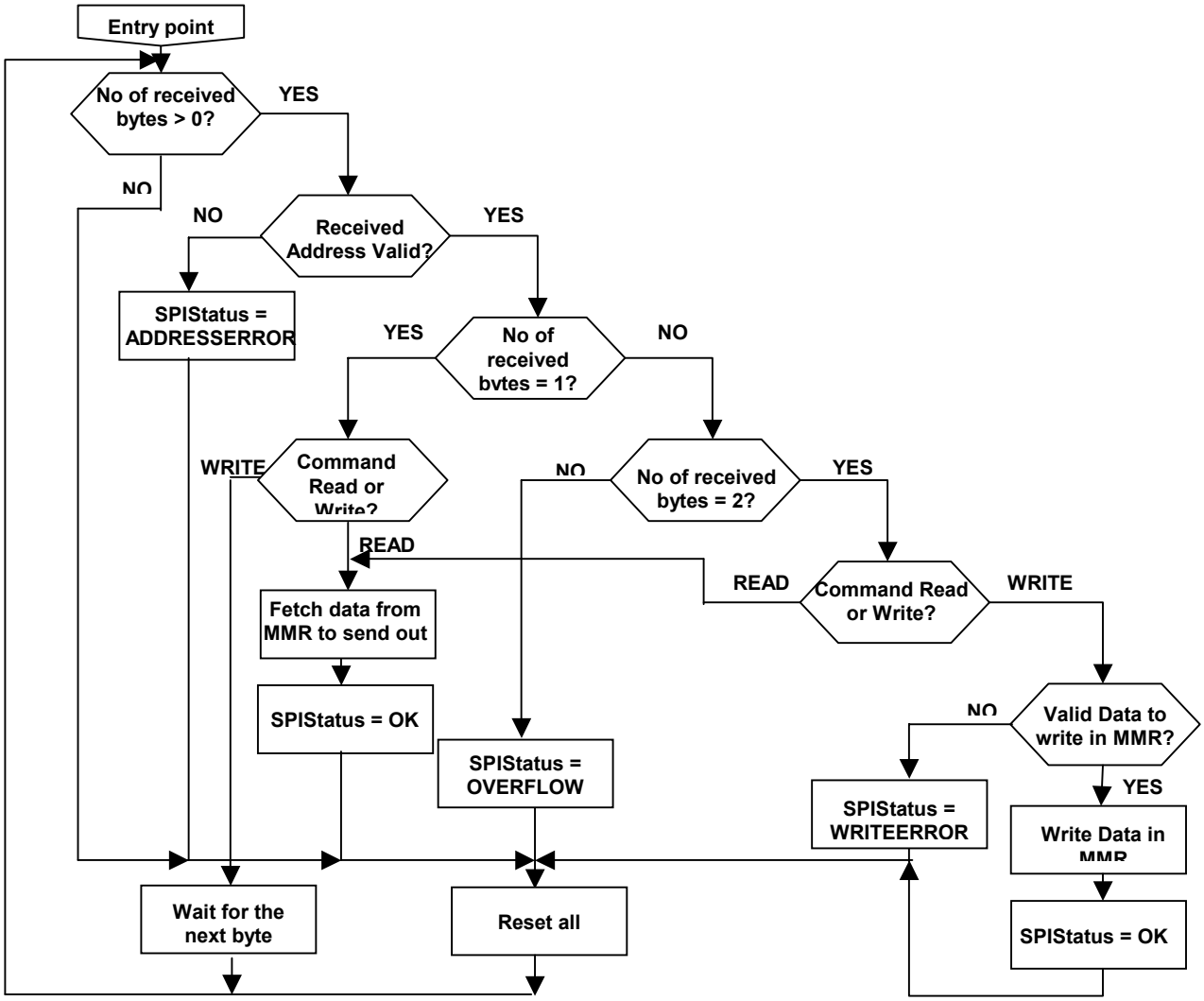


Figure 10. - The SPI flowchart.

Timing diagrams

Please see below the timing diagram for a write and read cycles. Please note that DOUT is not a tri-state output. The minimum value for t_{clk} is 100ns and time out t_{out} is approximately 1sec. The SPI will latch data on input DIN and set data on output DOUT on every rising edge of SCLK however operation mode can be changed operates on request. Changes may include clock polarity, length of data etc. During the read cycle the master have to provide a pause between two bytes of minimum 1ms ($t_{wait} \geq 1ms$).

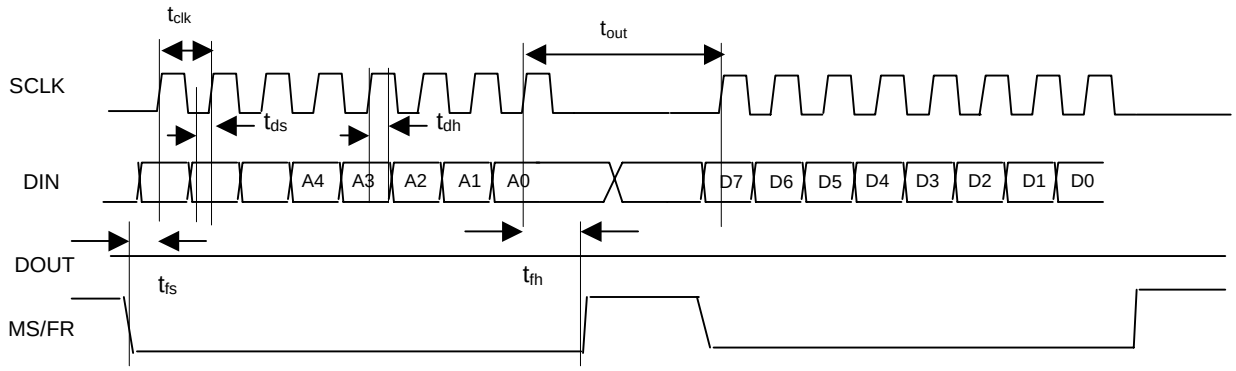


Figure 11. - Write cycle SPI 8-bit

Parameter	Min	Max
t_{clk} – CLK	100ns	
t_{fs} – Time to set FR prior CLK transition	$t_{clk}/2$	
t_{fh} – Time to hold FR after CLK transition	$t_{clk}/2$	
t_{ds}–Time to set data prior CLK transition	10ns	
t_{dh} – Time to hold data after CLK transition	1ns	

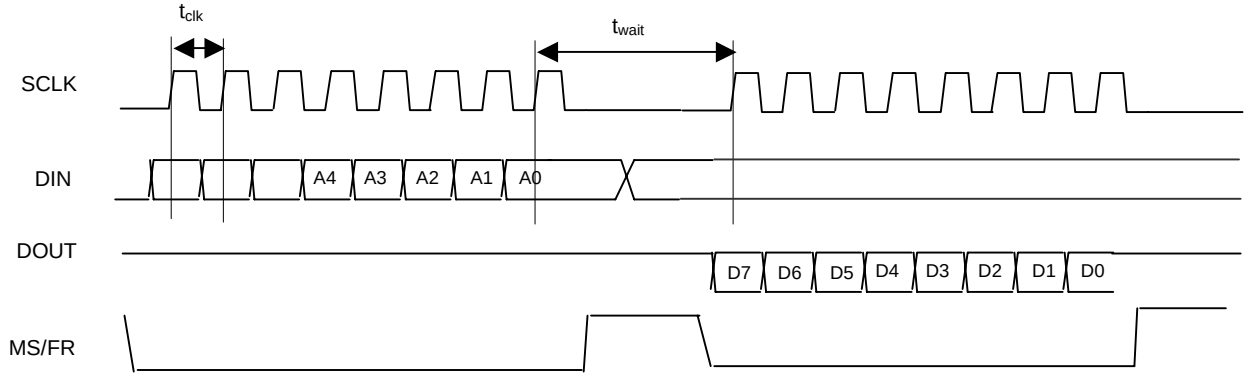


Figure 12. - Read cycle SPI 8-bit

Memory Mapped Registers

There are twenty-eight 8-bit registers accessible through the serial port: 12 registers to write and read data and 16 registers to only read data from module. See table 1 for memory map registers and their purpose.

Addr.	Read	Write	Name	Format								Description
				M							L	
				7	6	5	4	3	2	1	0	
00H	Y	Y	PR1	R23	R22	R21	R20	R13	R12	R11	R10	4-bit priority for references 1-2
01H	Y	Y	PR2	R43	R42	R41	R40	R33	R32	R31	R30	4-bit priority for references 3-4
02H	Y	Y	PR3	R63	R62	R61	R60	R53	R52	R51	R50	4-bit priority for references 5-6
03H	Y	Y	PR4	x	x	x	x	x	x	x	x	Not used
04H	Y	N	RFH1	S7	S6	S5	S4	S3	S2	S1	S0	Ref. 1 frequency shift in ppm
05H	Y	N	RFH2	S7	S6	S5	S4	S3	S2	S1	S0	Ref. 2 frequency shift in ppm
06H	Y	N	RFH3	S7	S6	S5	S4	S3	S2	S1	S0	Ref. 3 frequency shift in ppm
07H	Y	N	RFH4	S7	S6	S5	S4	S3	S2	S1	S0	Ref. 4 frequency shift in ppm
08H	Y	N	RFH5	S7	S6	S5	S4	S3	S2	S1	S0	Ref. 5 frequency shift in ppm
09H	Y	N	RFH6	S7	S6	S5	S4	S3	S2	S1	S0	Ref. 6 frequency shift in ppm
0AH	Y	N	RFH7	x	x	x	x	x	x	x	x	Not used
0BH	Y	N	RFH8	x	x	x	x	x	x	x	x	Not used
0CH	Y	N	RST1	S41	S40	S31	S30	S21	S20	S11	S10	References 1-4 status
0DH	Y	N	RST2	x	x	x	x	S61	S60	S51	S50	References 5-6 status
0EH	Y	N	PSP1	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Status of Primary PLL
0FH	Y	N	PSP2	US3	US2	US1	US0	SS3	SS2	SS1	SS0	Status of Secondary and Utility PLL
10H	Y	Y	PMAX	S7	S6	S5	S4	S3	S2	S1	S0	Maximum frequency pull in ppm
11H	Y	Y	PMIN	S7	S6	S5	S4	S3	S2	S1	S0	Minimum frequency pull in ppm
12H	Y	Y	CFG1	UI	X	X	MS	CON3	CON2	CON1	CON0	Configuration 1
13H	Y	Y	CFG2	X	X	P	F	R	H	R	A	Configuration 2
14H	Y	Y	FA1	F7	F6	F5	F4	F3	F2	F1	F0	Frequency acquisition set for PLL1
15H	Y	Y	BW11	P13	P12	P11	P10	P03	P02	P01	P00	Bandwidth 1 and 0 set for PLL1
16H	Y	Y	BW12	P33	P32	P31	P30	P23	P22	P21	P20	Bandwidth 3 and 2 set for PLL1
17H	Y	Y	FB2	F3	F2	F1	F0	B3	B2	B1	B0	Frequency acquisition (F) and Bandwidth track (B) for PLL2
18H	Y	N	SST	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	SPI status register
19H	Y	N	CID	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0	Customer ID register
1AH	Y	N	SID	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Software ID register
1BH	Y	N	HID	HID7	HID6	HID5	HID4	HID3	HID2	HID1	HID0	Hardware ID register

Table 1. Memory map registers.

Reference Priority Registers (PR1 to PR4) – address 00-03h

There are four registers PR1 – PR4 that specify priority during switching. Every reference has 4-bit priority so two references are defined per register. The priority means that the module in the event of loosing reference will lock to valid reference with higher priority available if bit AUTOEN of register CFG2 is set to one. The initial priority is set by module but can be overridden by customer. The highest priority is 1111b and the lowest priority is 0001b. If priority is set to zero (0000b) the reference will not be used in the module – the status will be "Reference present but not in use".

- R10-R13 – defines reference 1 priority
- R20-R23 – defines reference 2 priority
- R30-R33 – defines reference 3 priority
- R40-R43 – defines reference 4 priority
- R50-R53 – defines reference 5 priority
- R60-R63 – defines reference 6 priority

The default values are:
PR1:0x78h
PR2:0x56h
PR3:0x34h
PR4:0x12h

Frequency Shift Registers (RFH1-RFH8) - address 04-0Bh.

The registers indicate how far the references out of nominal frequency in parts per million (ppm). The resolution is 0.5ppm. The range is ±63ppm. If the frequency above or below ±63ppm range, the +63 or -63 is shown respectively and proper status indicated in Reference Status Registers. The format is 2-s compliment and for example if the content of RFS3 register is 11000111 then the third reference is: -28.5ppm

7(MSB)	6	5	4	3	2	1	0(LSB)
SIGN	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}

The default values are:
RFH1: 0xFFh
RFH2: 0xFFh
RFH3: 0xFFh
RFH4: 0XFFh
RFH5: 0xFFh
RFH6: 0xFFh
RFH7: 0xFFh
RFH8: 0xFFh

Reference Status Registers (RST1-RST2) - address 0C-0Dh

There are 2 reference status registers that hold information about status of references. Each reference has 2-bit status or each register keep statuses for four references. The possible statuses are:

Binary number	Status	Description
00	Not Present	Reference not present or can not be evaluated
01	Present	Reference present but out of frequency range
10	Not in use	Reference present but not in use
11	Reference OK	Reference present and in the frequency range

- S10-S11 – defines status of reference 1
- S20-S21 – defines status of reference 2
- S30-S21 – defines status of reference 3
- S40-S41 – defines status of reference 4
- S50-S51 – defines status of reference 5
- S60-S61 – defines status of reference 6

The default values are:
RST1: 0x00h
RST2: 0x00h

PLL Status Registers (PSP1-PSP2) - address 0E-0Fh

Register PSP1 indicates status of Primary PLL. In the register the 4 least significant bits indicate status of the PLL and the 4 most significant bits indicate reference in use in the loop. The possible statuses of Primary PLL are shown in PSP1:

PS3-PS0	Status description
0000	PLL not locked. This status represents major error.
0001	Frequency Acquisition
0010	Phase Acquisition
0011	Tracking Bandwidth 0
0100	Tracking Bandwidth 1 (SP1 only)
0101	Tracking Bandwidth 2 (SP1 only)
0110	Tracking Bandwidth 3 (SP1 only)
0111	Phase Build-out
1000	Holdover
1001	Free run

The possible reference bits are:

PS7-PS4	Status description
x000	No reference in use (module in Free run or Holdover)
x001	Reference 1

x010	Reference 2
x011	Reference 3
x100	Reference 4
x101	Reference 5
x110	Reference 6
0xxx	Holdover History Buffer Not Available
1xxx	Holdover History Buffer Available

Register PSP2 indicates status of Secondary PLL. In the register the 4 least significant bits indicate status of the Secondary PLL and the 4 most significant bits indicate status of the utility PLL if available.

SS3-SS0	Status description
0000	PLL not locked. This status represents major error.
0001	Frequency Acquisition operating as a master clock
0010	Phase Acquisition operating as a master clock
0011	Tracking Bandwidth operating as a master clock
0100	Frequency Acquisition operating as a slave clock
0101	Phase Acquisition using operating as a slave clock
0110	Tracking Bandwidth using operating as a slave clock

The possible utility PLL status bits.

US3-US0	Status description
0000	Not locked
0001	Locked

The default values are:
PSP1: 0x00h
PSP2: 0x00h

Frequency Pull Range Registers (PMAX and PMIN) - address 10-11h

These registers specify the window of pull-in range and reference acceptance frequency window. The PMAX register specifies maximum frequency window that the module can be locked on and frequency beyond references will be rejected. The PMIN registers frequency window within references will be accepted. The PMAX must be greater then PMIN and both are positive numbers. The data format is unsigned binary 8-bit number, for example if the content of PMAX register is 00011110 and PMIN 00011010 then the pull in range is: ±15ppm and reference acceptance is ±13ppm:

7(MSB)	6	5	4	3	2	1	0(LSB)
2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}

The default values are:
PMAX: 0x1Eh
PMIN: 0x1Ah

Configuration Registers (CFG1 and CFG2) - address 12-13h

Register CFG1 used to set clock mode of operation. The user can select which interface will be used to change the mode of operation by setting bit UI. If the UI bit in CFG1 register is set to 0 (default) the module will change the state in according to three input pins CNT1, CNT2 and CNT3. If the If the UI bit in CFG1 register is set to 1 the module will changed the state in according to four bits (CON0, CON1, CON2 and CON3) in CFG1 registers.
There are 4 bits to set 10 modes of operation:

CON3	CON2	CON1	CON0	Mode of operation
0	0	0	0	Free-run
0	0	0	1	Lock to Reference 1
0	0	1	0	Lock to Reference 2
0	0	1	1	Holdover
0	1	0	0	Lock to Reference 3
0	1	0	1	Lock to Reference 4

0	1	1	0	Lock to Reference 5
0	1	1	1	Lock to Reference 6
1	1	1	0	Not used
1	1	1	1	Not used

Other combinations are not supported and ignored. Bits 7 to 4 of CFG1 are reserved for future use and ignored in this set.
Bit MS in CFG1 sets the module to Master – Slave operation, MS bit 0 (default) the module operates as Master and MS bit 1 the module operates as slave in condition that a signal at SEC IN (pin 25) is present.
Register CFG2 used by customer to control behavior of the module for application needs.

7(MSB)	6	5	4	3	2	1	0(LSB)
X	X	PBD	FREV	RESET	HLRST	REVEN	AUTOEN

AUTOEN - when set to logic high, enabling automatic switching to other reference in the event of loosing current reference according to priority set by registers PR1-PR4. When set to logic low, will not switch to other reference.

REVEN - when set to high, will enable revertive operation.

HLRST - when set to high, will erase previous operation history for holdover.

RESET - when set to high, will initiate internal reset of the module.

FREV – when set to high and if AUTOEN set to high will switch references based on their frequency offset (select the best of available).

PBD - when set to high Phase Build Out is disabled.

The default values are:
CFG1: 0x00h
CFG2: 0x00h

Frequency Acquisition set for Primary PLL (FA1) - address 14h

FA1 register determines the bandwidth during frequency acquisition of PLL. The values of FA0-7 represent frequency acquisition in Hz (0-256Hz).

The default values are:
FA1: 100

Bandwidth set registers for PLL1 (BW11, BW12) - address 15-16h

BW11 and BW12 registers determine the tracking bandwidth of the primary PLL. There four sets of bits each one representing the corresponding tracking bandwidth. The table below shows the available combinations.

Px3	Px2	Px1	Px0	Bandwidth
0	0	0	0	NA
0	0	0	1	0.001Hz
0	0	1	0	0.01Hz

0	0	1	1	0.1Hz
0	1	0	0	1
0	1	0	1	2
0	1	1	0	3
0	1	1	1	10
1	0	0	0	20
All others				TBD

The default values are:
BW11: 0x23h
BW12: 0x01h

Frequency Acquisition and Bandwidth Track for PLL2 (FB2) – address 17h

FB2 register determines bandwidth for Secondary PLL in frequency acquisition and tracking modes. The tables below represent available combinations for B0-B3 (frequency acquisition) and F0-F3 (tracking).

B3	B2	B1	B0	Bandwidth
0	0	0	0	NA
0	0	0	1	10Hz
0	0	1	0	20Hz
0	0	1	1	30Hz
0	1	0	0	40Hz
0	1	0	1	50Hz
0	1	1	0	60Hz
0	1	1	1	70Hz
1	0	0	0	80Hz
1	0	0	1	90Hz
1	0	1	0	100Hz
1	0	1	1	200Hz
1	1	0	0	300Hz
1	1	0	1	400Hz
1	1	1	0	500Hz
1	1	1	1	600Hz

F3	F2	F1	F0	Bandwidth
0	0	0	0	NA
0	0	0	1	3Hz
0	0	1	0	5Hz
0	0	1	1	10Hz
0	1	0	0	15Hz
0	1	0	1	20Hz
0	1	1	0	25Hz
0	1	1	1	30Hz
1	0	0	0	35Hz
1	0	0	1	40Hz
1	0	1	0	50Hz
1	0	1	1	60Hz
1	1	0	0	70Hz
1	1	0	1	80Hz
1	1	1	0	100Hz
1	1	1	1	200Hz

The default value:
FB2: 0x53h.

SPI Status Register (SST) – address 18h

The SST register represents current status of SPI communication. The address can be read only one of the following values:

MESSAGE	VALUE	ACTION
SPIERRSTATOK	0	If correct command was received by the module
SPIERRRECOVERFLOW	2	If more then two bytes are received before the routine handled
SPIERRINVALIDADDR	3	If incorrect address was received by the module
SPIERRINVALIDWRITEADDR	4	If incorrect write address or value was received by the module

Customer ID Register (CID) – address 19h

The CID register contains unique customer identification number.
The default value:
CID: 0x03h.

Software ID Register (SID) – address 1Ah

The SID register contains unique software identification number.

The default value:
SID: 0x18h. (will vary with new updates)

The Standard Timing Application in Systems

A typical timing application for telecommunication equipment is shown at the figure below. The system consists of two Clock Cards (CC1 and CC1) and several Line Cards (LC 1 to LC N). The Clock Cards use two clock modules SY10 to generate two redundant signal references for the whole box and the Line Cards use high frequency synchronizer module SY05 as a high frequency reference signals for communication ICs (for e.g. transceivers). The two Clock Cards are connected in such a way to provide a Master/Slave operation of two clocks. At CC the local processors can configure and monitor SY10 module by serial port SPI. Two reference signals and optionally four status signals from each Clock Card (STATUS 1 and STATUS 2) are distributed to all Line Cards. The STATUS 1 and 2 signals are HOLDOVER (pin 1 at SY10), FREERUN (pin 7), ALARM OUT (pin 11) and PLL UNLOCK (pin 17) and they are connected to the corresponding pins at SY05 modules. For a particular application or a timing application that best fits to you please contact Raltron.

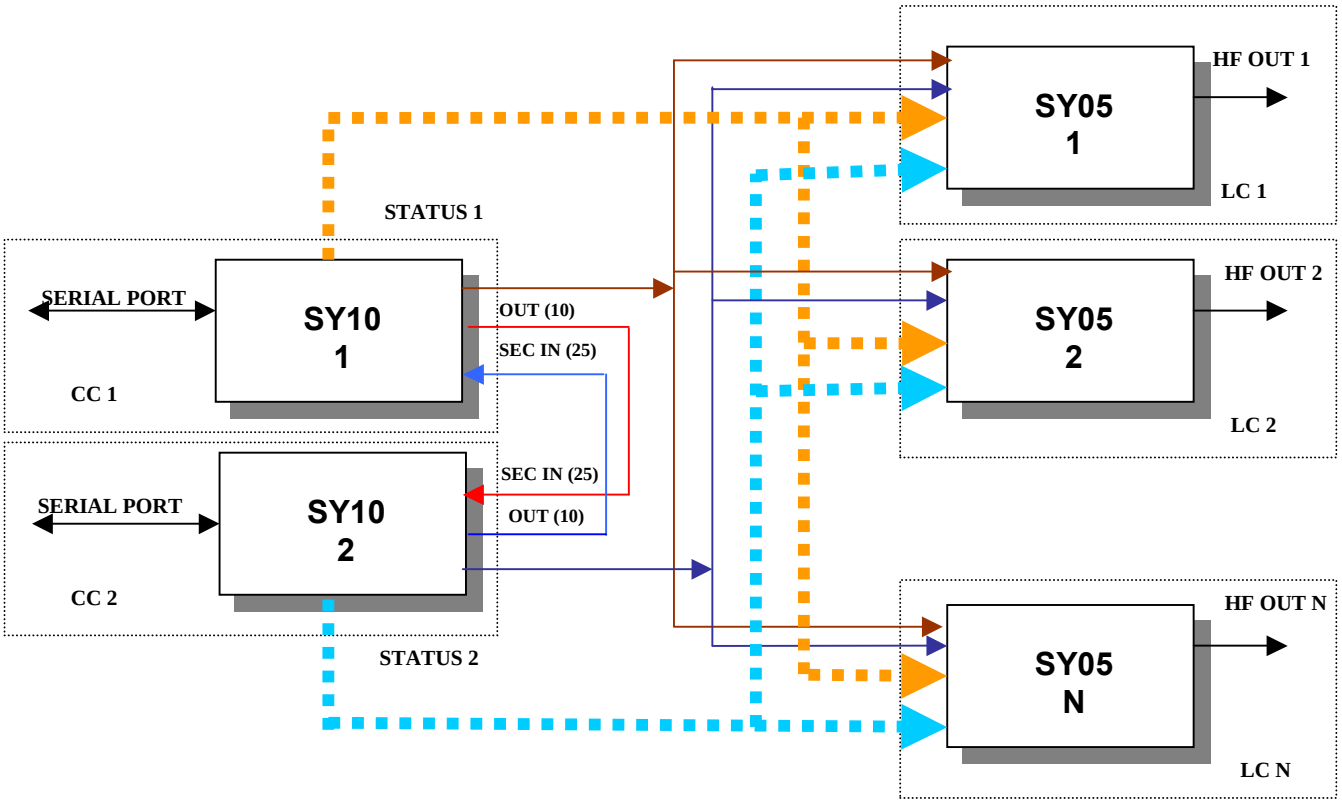


Figure 9. A typical timing application.

- **SPECIFICATIONS**

General Specifications	Mechanical	1.82" (D) x 1.82" (W) x 0.70" (H) 1.8" (D) x 1.8" (W) x 0.60" (H)		Metal box Module on PCB
	Power Supply Warm Up Current Supply Steady State Current Supply Operating Temperature Humidity Internal Oscillators	3.3VDC 700mA max @ 25°C 400mA max. @ 25°C -20°C to 70°C 5% to 95% non-condensing OCXO		Varies from different oscillator used Other ranges available on request SC-cut for Stratum 3E AT-cut for stratum 3
Input Signals	Number of Inputs	6		
	Input reference frequency Signal Level	8kHz to 77.76MHz HCMOS/TTL Compatible		User selectable
	Time Reference characteristics			Bellcore: GR-1244-core 3.2.1.R3-1
Output Signal	Number of Outputs	3		
	Output 1 Output 2	8KHz to 77.76MHZ 8KHz to 77.76MHZ		User define User define
	Output 3	8KHz		
	Signal Level I/O	HCMOS		3.3V levels 5V tolerant
Signal Quality Performance	Jitter Tolerance			Bellcore: GR-1244-core 4.2 ITU-T: G.813
	Phase Transient Tolerance			Bellcore: GR-1244-core 4.4
	Wander Generation			Bellcore: GR-1244-core 5.3 ITU-T: G.812
	Wander Tolerance			Bellcore: GR-1244-core 4.3 ITU-T: G.812
	Jitter Generation and Transfer			Bellcore: GR-1244-core 5.5 ITU-T: G.812
	Wander Transfer			Bellcore: GR-1244-core 5.4 ITU-T: G.812
Frequency Output Performance		Stratum 3E	Stratum 3	
	Free run accuracy	±4.6ppm	±4.6ppm	GR-1244-core 5.1 ITU-T: G.812
	Holdover frequency stability	$\pm 1 \times 10^{-8}$ /24 h	$\pm 0.37 \times 10^{-6}$ /24 h	Bellcore: GR-1244-core 5.2 ITU-T: G.812
	Initial Offset	$\pm 1 \times 10^{-9}$	$\pm 50 \times 10^{-9}$	Bellcore: GR-1244-core 5.2 ITU-T: G.812
	Temperature	$\pm 8 \times 10^{-9}$	$\pm 280 \times 10^{-9}$	
	Drift	$\pm 1 \times 10^{-9}$	$\pm 1 \times 10^{-9}$	Bellcore: GR-1244-core 5.2 ITU-T: G.812
	Phase Build-Out	Yes	No	Bellcore: GR-1244-core 5.7 ITU-T: G.812
	DPLL bandwidth	0.001Hz	0.1Hz	or adjustable up to 20Hz
	Lock Time	<700	<100sec	GR-1244-core 3.5
	Lock accuracy	$\pm 1 \times 10^{-11}$	$\pm 1 \times 10^{-11}$	

- **PIN ASSIGNMENT**

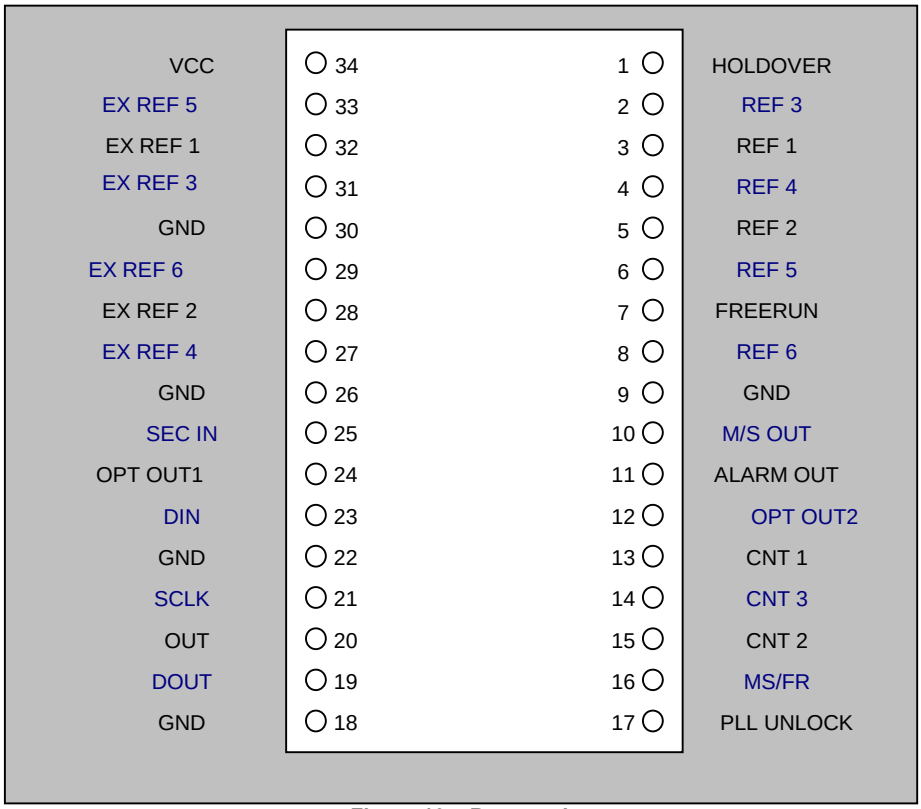


Figure 10 – Bottom view

Pin #	Name	Description
1	HOLDOVER	Holdover Signal -> the output is high when the unit is in holdover mode
2	REF 3	Reference 3 Signal -> See I**ndication** section on page 4
3	REF 1	Reference 1 Signal -> See I**ndication** section on page 4
4	REF 4	Reference 4 Signal -> See I**ndication** section on page 4
5	REF 2	Reference 2 Signal -> See I**ndication** section on page 4
6	REF 5	Reference 5 Signal -> See I**ndication** section on page 4
7	FREERUN	Free-run Signal -> the output is high when the unit is in the free run mode
8	REF 6	Reference 6 Signal -> See I**ndication** section on page 4
10	M/S OUT	Master/Slave Synchronizing output (To be connected to slave module SEC-IN
11	ALARM OUT	Alarm signal -> the output is high when there is an alarm in the module.
12	OPT OUT2	Optional Output 2-> the secondary output of the synchronized signal
13	CNT 1	Control Input 1 -> the external input for selecting mode of the unit – see table.
14	CNT 3	Control Input 3 -> the external input for selecting mode of the unit – see table.
15	CNT 2	Control Input 2 -> the external input for selecting mode of the unit – see table.
16	MS/FR	Master/Slave Selection or Frame SPI Input -> to select master or slave – master/ slave operation of two clocks or in case of using SPI it is Frame synch signal for communication.
17	PLL UNLOCK	PLL Unlocked Signal -> the output is high when the unit is not locked to any of the references
9,18,22,26,30	GND	Ground
34	VCC	Positive Voltage Supply
19	DOUT	Serial Data Output -> SPI serial communication interface data output
20	OUT	Synchronized Output -> the output of the synchronized signal
21	SCLK	Serial Clock Input -> SPI serial communication interface clock input
23	DIN	Serial Data Input/ -> SPI serial communication interface data input
24	OPT OUT1	Optional Output 1-> the secondary output of the synchronized signal,.
25	SEC IN	SEC Input -> the input from the second clock module – master/slave operation of two clocks.
27	EX REF 4	External Reference 4 Input -> the input signal from reference 4
28	EX REF 2	External Reference 2 Input -> the input signal from reference 2
29	EX REF 6	External Reference 6 Input -> the input signal from reference 6
31	EX REF 3	External Reference 3 Input -> the input signal from reference 3
32	EX REF 1	External Reference 1 Input -> the input signal from reference 1
33	EX REF 5	External Reference 5 Input -> the input signal from reference 5

- **MECHANICAL DIMENSIONS**

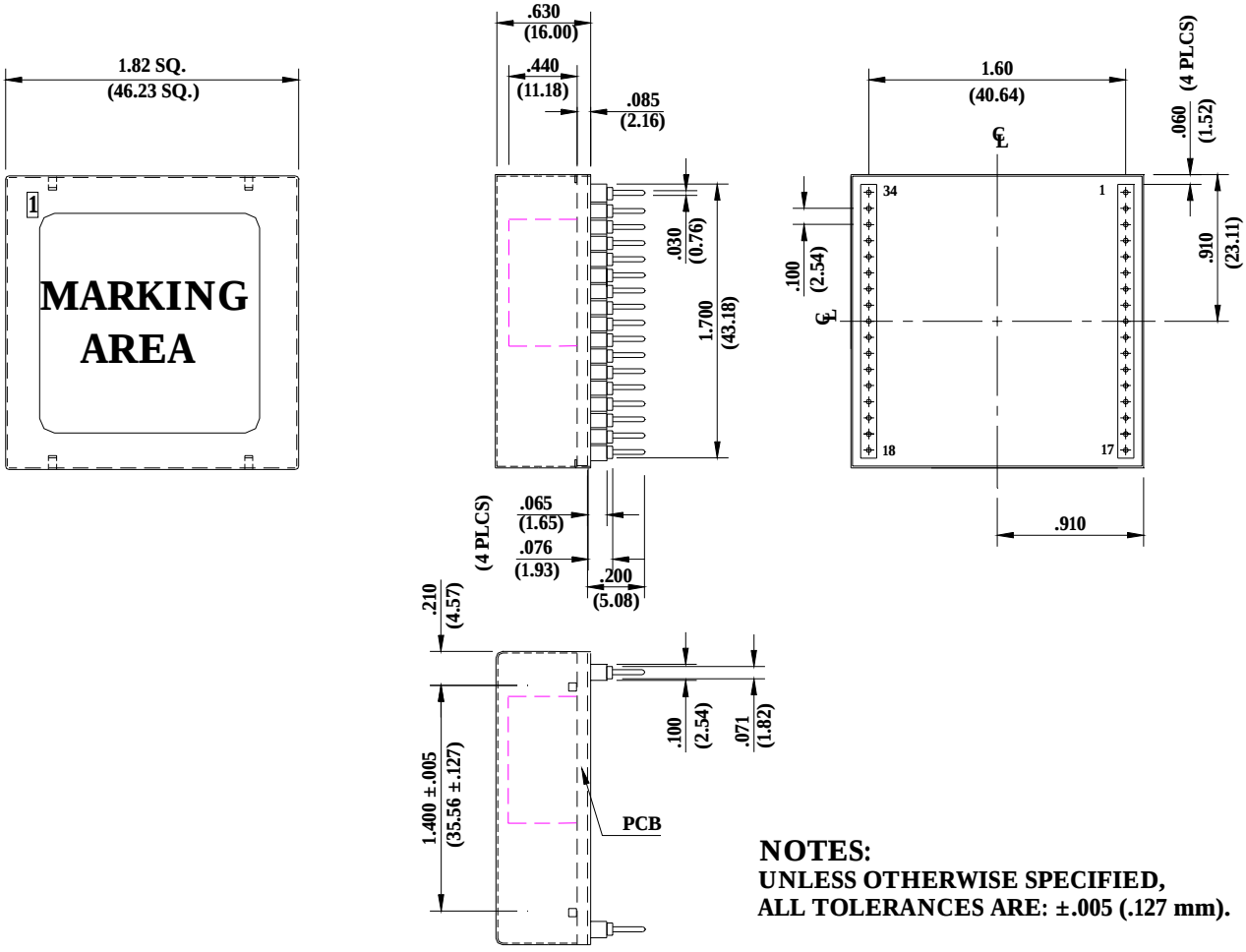


Figure 11 – The mechanical dimensions.

Figure 11 shows the mechanical dimension of the SY10 module. The module can be supplied in two different types of packaging:

- Metal box
- Module without packaging

The label on the module shows part number, factory name, week and year of production. Without metal cover maximum height reaches 0.60".