

# NVGS3130N

## Product Preview

### Power MOSFET

#### 20 V, 5.9 A, Single N-Channel, TSOP-6

##### Features

- Leading Edge Trench Technology for Low On Resistance
- Low Gate Charge for Fast Switching
- Small Size (3 x 2.75 mm) TSOP-6 Package
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR-Free and are RoHS Compliant

##### Applications

- DC-DC Converters
- Lithium Ion Battery Applications
- Load/Power Switching

##### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit	
Drain-to-Source Voltage		V <sub>DSS</sub>	20	V	
Gate-to-Source Voltage		V <sub>GS</sub>	±8	V	
Continuous Drain Current (Note 1)	Steady State	I <sub>D</sub>	T <sub>A</sub> = 25°C	5.9	A
			T <sub>A</sub> = 85°C	4.6	
	t ≤ 10 s	T <sub>A</sub> = 25°C	6.6		
Power Dissipation (Note 1)	Steady State	P <sub>D</sub>	T <sub>A</sub> = 25°C	1.4	W
			t ≤ 10 s	1.7	
Continuous Drain Current (Note 2)	Steady State	I <sub>D</sub>	T <sub>A</sub> = 25°C	4.4	A
			T <sub>A</sub> = 85°C	3.4	
Power Dissipation (Note 2)	Steady State	P <sub>D</sub>	T <sub>A</sub> = 25°C	0.8	W
Pulsed Drain Current	t <sub>p</sub> ≤ 10 s	I <sub>DM</sub>	24	A	
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C	
Source Current (Body Diode)		I <sub>S</sub>	1.1	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

##### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	R <sub>θJA</sub>	110	°C/W
Junction-to-Ambient – t ≤ 10 s (Note 1)		90	
Junction-to-Ambient – Steady State (Note 2)		200	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size

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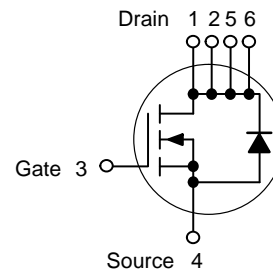


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V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> mAX	I <sub>D</sub> Max
20 V	24 mΩ @ 4.5 V	5.9 A
	32 mΩ @ 2.5 V	5.2 A

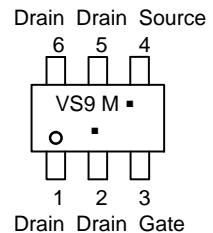
##### N-Channel



##### MARKING DIAGRAM & PIN ASSIGNMENT



TSOP-6  
CASE 318G  
STYLE 1



VS9 = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

##### ORDERING INFORMATION

Device	Package	Shipping†
NVGS3130NT1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 250 μA	20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			9.8		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 16 V, T <sub>J</sub> = 25°C			1.0	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0, V <sub>GS</sub> = ±8 V			100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	0.4	0.6	1.4	V
Negative Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			3.4		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.6 A		19	24	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.9 A		25	32	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.6 A		8.2		S

## CHARGES, CAPACITANCE, & GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 16 V		935		pF
Output Capacitance	C <sub>OSS</sub>			169		
Reverse Transfer Capacitance	C <sub>RSS</sub>			104		
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 10 V		965		pF
Output Capacitance	C <sub>OSS</sub>			198		
Reverse Transfer Capacitance	C <sub>RSS</sub>			110		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 16 V, I <sub>D</sub> = 5.6 A		13.2	20.3	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.60		
Gate-to-Source Charge	Q <sub>GS</sub>			1.5		
Gate-to-Drain Charge	Q <sub>GD</sub>			4.2		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5.0 V, I <sub>D</sub> = 6.2 A		11.8	18.0	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.6		
Gate-to-Source Charge	Q <sub>GS</sub>			1.4		
Gate-to-Drain Charge	Q <sub>GD</sub>			2.7		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 4.5 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 16 V, I <sub>D</sub> = 1 A, R <sub>G</sub> = 3 Ω		6.3	12.6	ns
Rise Time	t <sub>r</sub>			7.3	13.5	
Turn-Off Delay Time	t <sub>d(OFF)</sub>			21.7	35.1	
Fall Time	t <sub>f</sub>			9.7	17.6	

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.0 A	T <sub>J</sub> = 25°C		0.7	1.2	V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 Vdc, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = 1.0 A			20.4		ns
Charge Time	t <sub>a</sub>				8.1		
Discharge Time	t <sub>b</sub>				11.6		
Reverse Recovery Charge	Q <sub>RR</sub>					8.8	

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperature.

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## TYPICAL CHARACTERISTICS

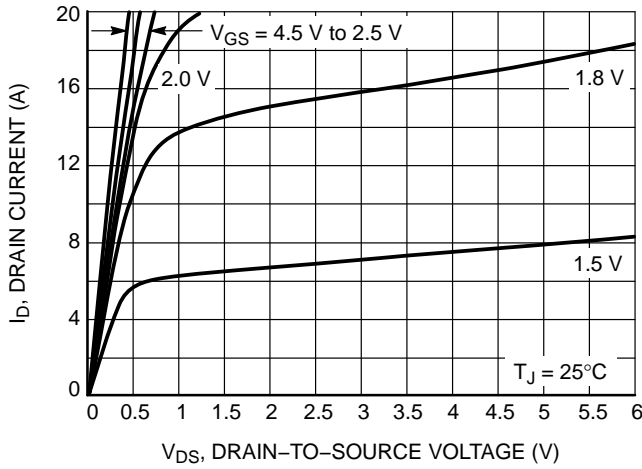


Figure 1. On-Region Characteristics

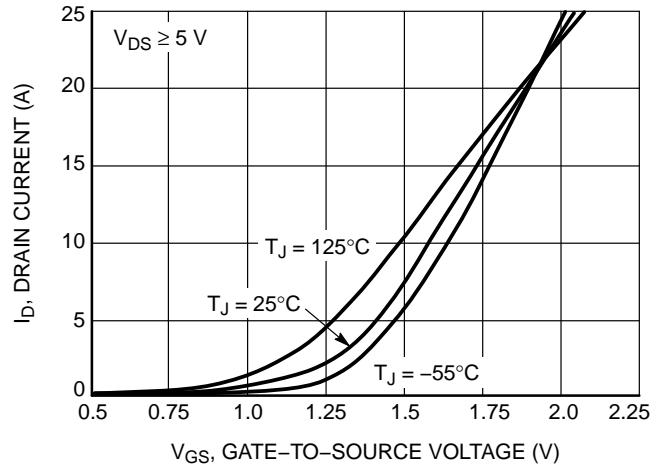


Figure 2. Transfer Characteristics

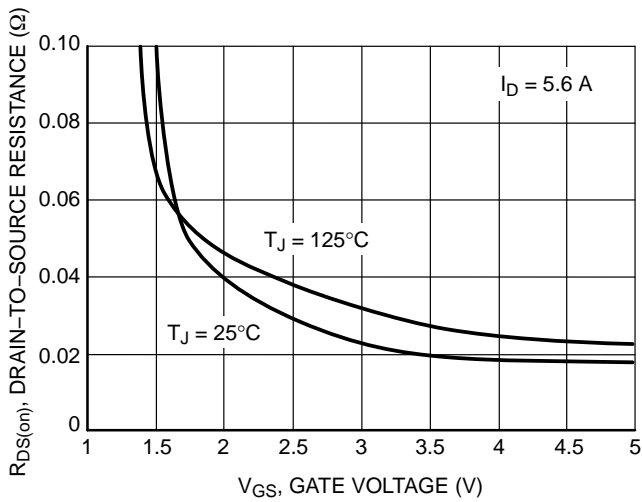


Figure 3. On-Resistance vs. Gate-to-Source Voltage

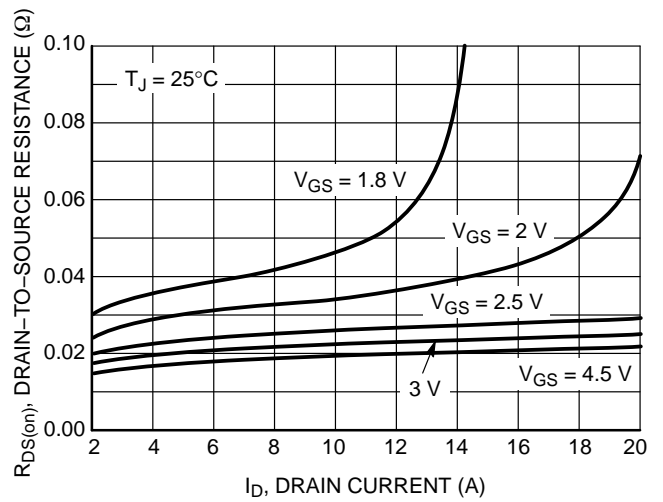


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

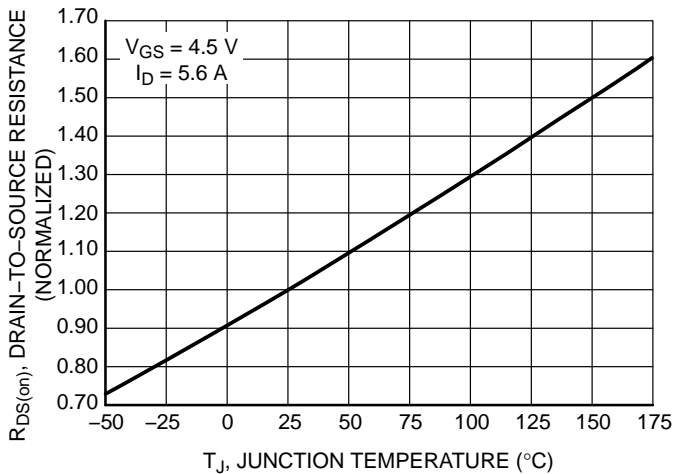


Figure 5. On-Resistance Variation with Temperature

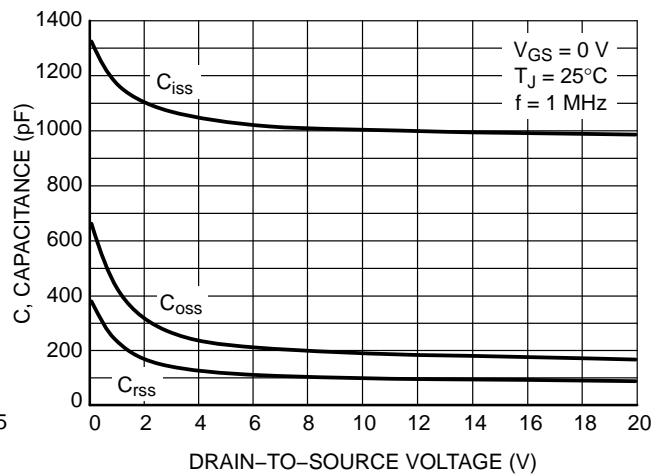
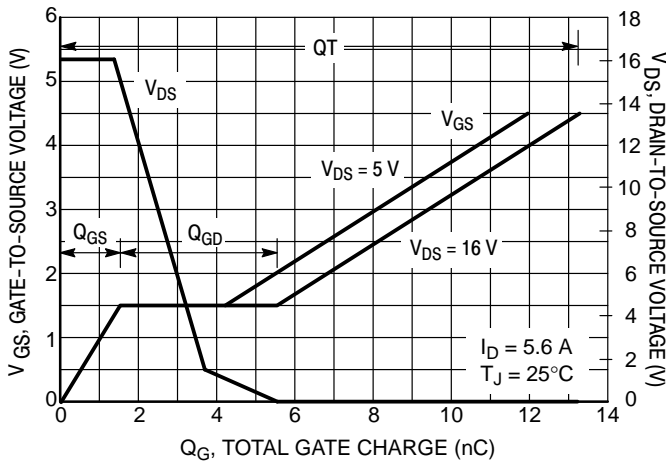


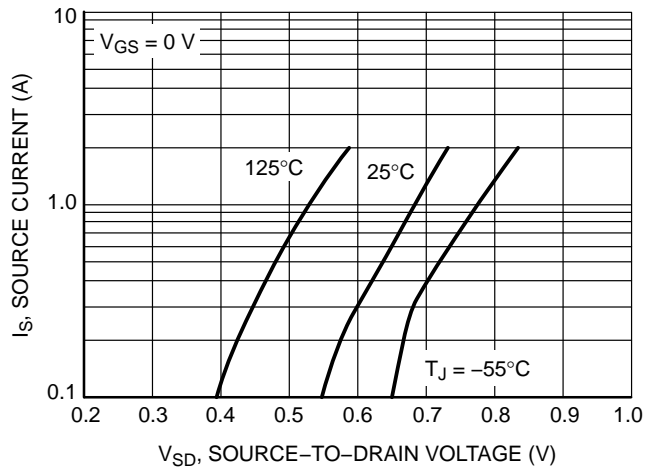
Figure 6. Capacitance Variation

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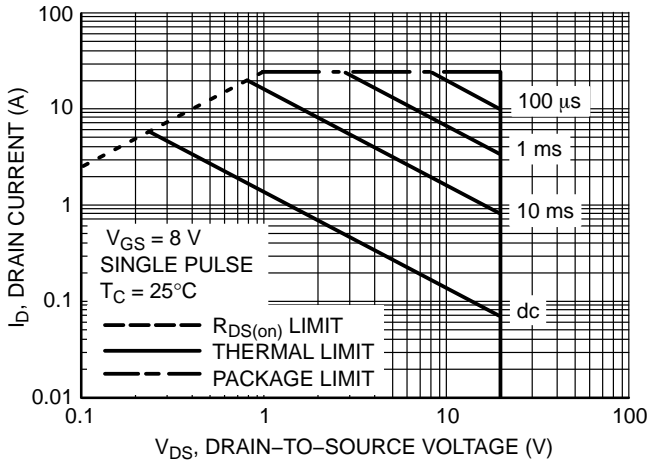
## TYPICAL CHARACTERISTICS



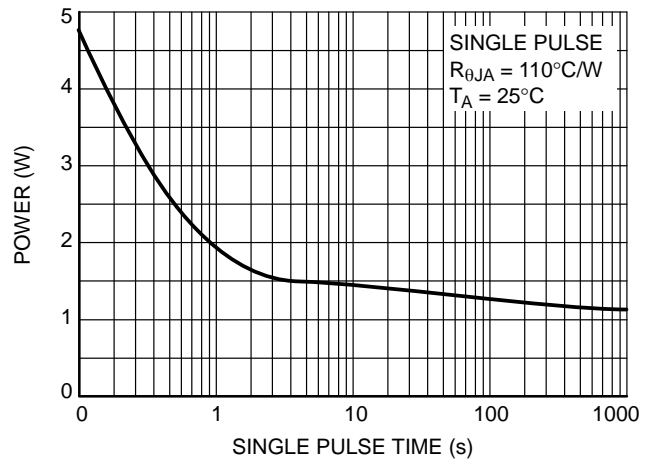
**Figure 7. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge**



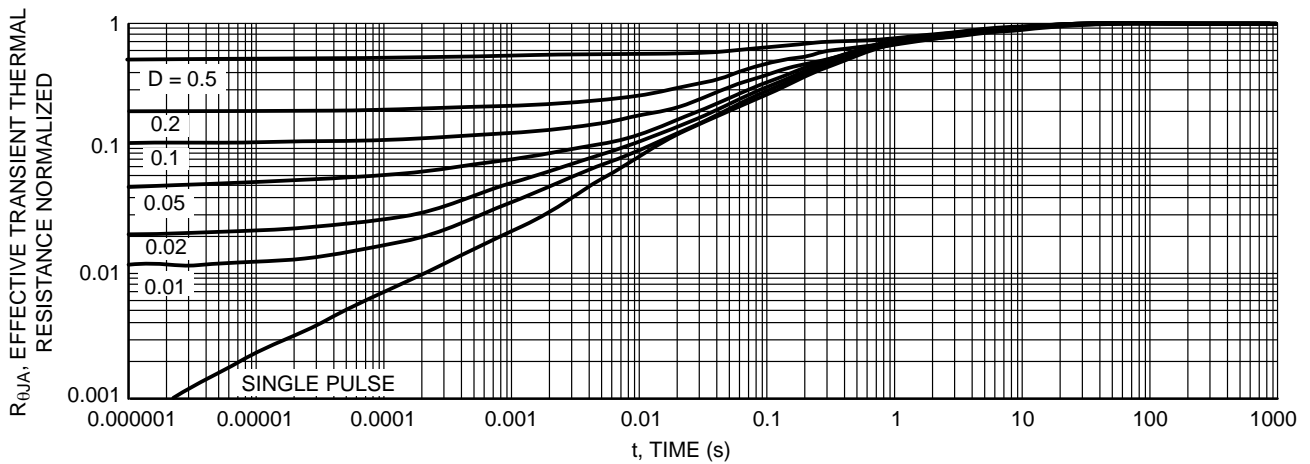
**Figure 8. Diode Forward Voltage vs. Current**



**Figure 9. Maximum Rated Forward Biased Safe Operating Area**



**Figure 10. Single Pulse Maximum Power Dissipation**

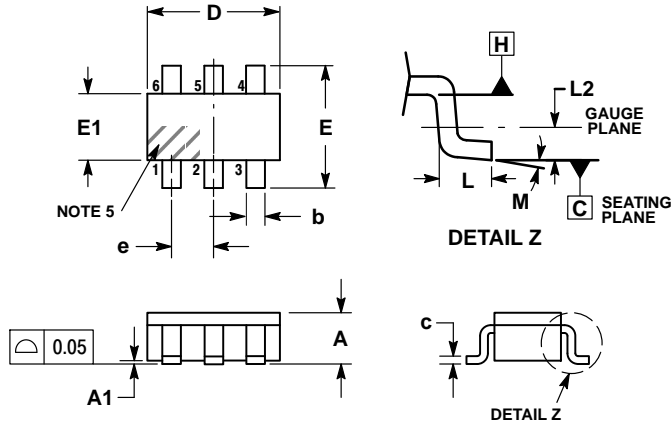


**Figure 11. Thermal Response**

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## PACKAGE DIMENSIONS

### TSOP-6 CASE 318G-02 ISSUE V



#### NOTES:

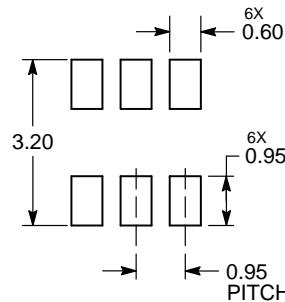
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°


#### STYLE 1:

1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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