STL12N3LLH5

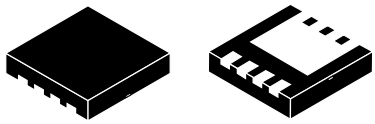
N-channel 30 V, 0.0079 Ω, 12 A, PowerFLAT™ (3.3 x 3.3) STripFET™ V Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STL12N3LLH5	30 V	< 0.009 Ω	12 A (1)

1. The value is rated according Rthj-pcb

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



PowerFLAT™(3.3x3.3)

(Chip scale package)

Applications

- Switching applications

Description

The STL12N3LLH5 is a 30 V N-channel STripFET™ V. This Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

Figure 1. Internal schematic diagram

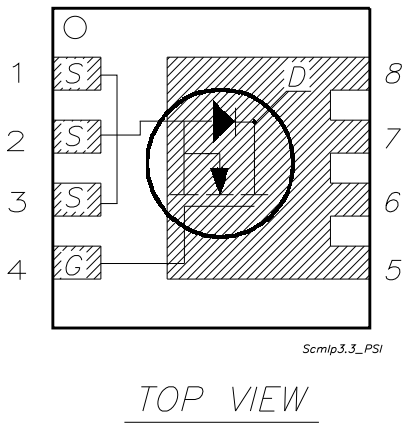


Table 1. Device summary

Order code	Marking	Package	Packaging
STL12N3LLH5	12N3L	PowerFLAT™ (3.3 x 3.3)	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	± 22	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	12	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	7.5	A
I_{DM} (2)	Drain current (pulsed)	48	A
P_{TOT} (3)	Total dissipation at T_C = 25 °C	50	W
P_{TOT} (1)	Total dissipation at T_C = 25 °C	2	W
	Derating factor	0.4	W/°C
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	°C

1. The value is rated according to Rthj-pcb
2. Pulse width limited by safe operating area
3. The value is rated according to Rthj-c

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (drain)	2.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	42.8	°C/W
$R_{thj\text{-}pcb}$ (2)	Thermal resistance junction-pcb	63.5	°C/W

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, t < 10 sec
2. Steady-state

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D=250 µA, V_{GS}=0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS}=max. rating, V_{DS}=max. rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS}=± 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}=10 V, I_D=6 A V_{GS}=4.5 V, I_D=6 A		0.0079 0.0095	0.0090 0.011	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS}=25 V, f=1 MHz, V_{GS}=0		1500 295 39		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D=12 A V_{GS}=4.5 V *(see Figure 14)*		12 4 4.7		nC nC nC
R_G	Gate input resistance	f=1 MHz gate DC bias=0 Test signal level=20 mV Open drain	0.5	1.5	2.5	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=15 V, I_D= 6 A, R_G=4.7 Ω, V_{GS}=4.5 V *(see Figure 13)*	-	9.3 14.5 22.7 4.5	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		15	A
I_{SDM}(1)	Source-drain current (pulsed)		-		60	A
V_{SD}(2)	Forward on voltage	I_{SD}=12 A, V_{GS}=0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=12 A, di/dt=100 A/µs, V_{DD}=20 V, Tj=150 °C *(see Figure 18)*	-	25 17.5 1.4		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 µs, duty cycle 1.5 %

3 Test circuits

Figure 2. Switching times test circuit for resistive load

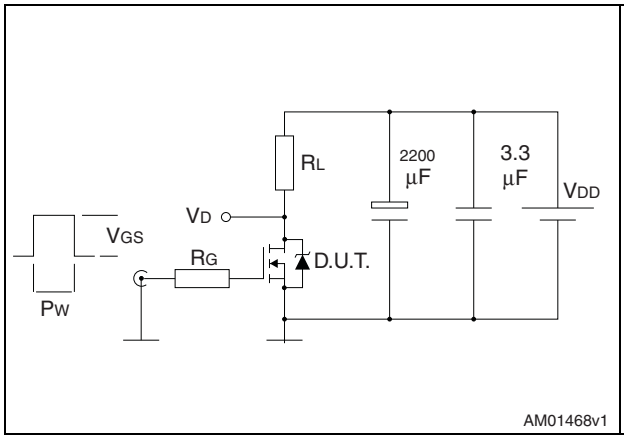


Figure 3. Gate charge test circuit

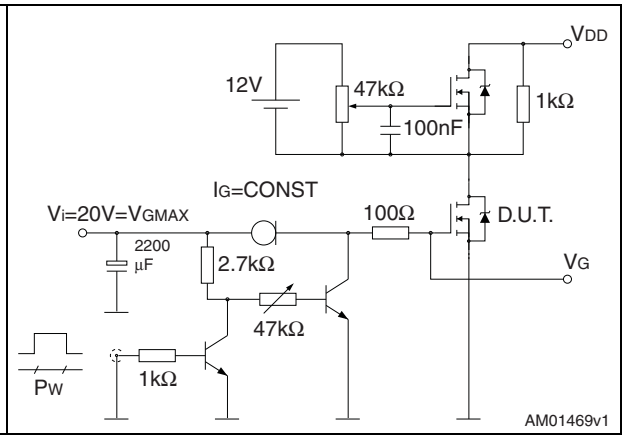


Figure 4. Test circuit for inductive load switching and diode recovery times

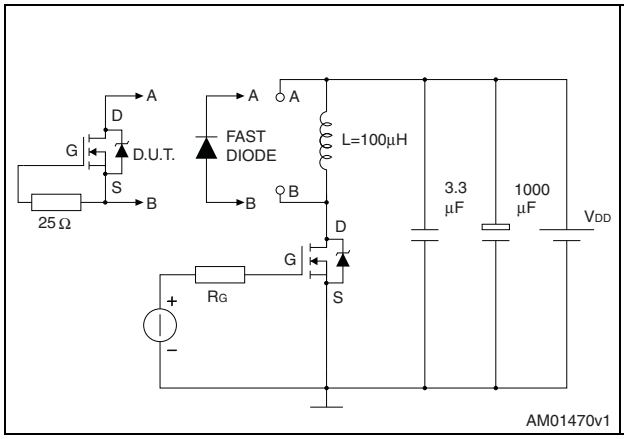


Figure 5. Unclamped inductive load test circuit

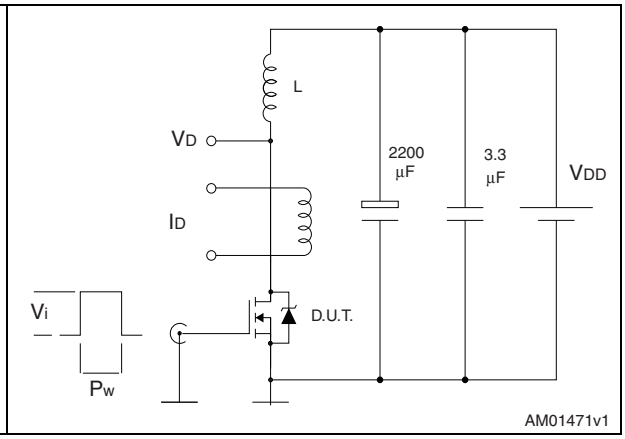


Figure 6. Unclamped inductive waveform

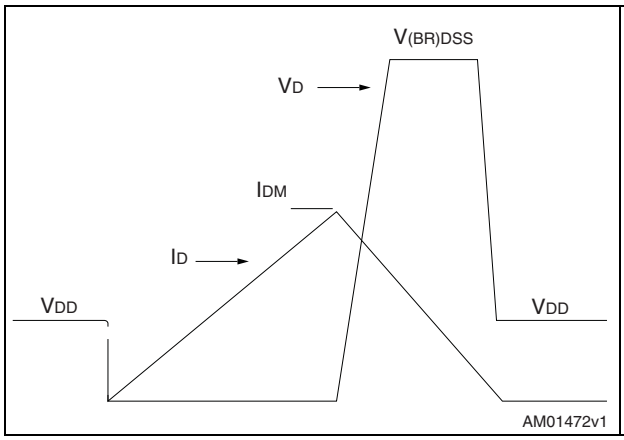
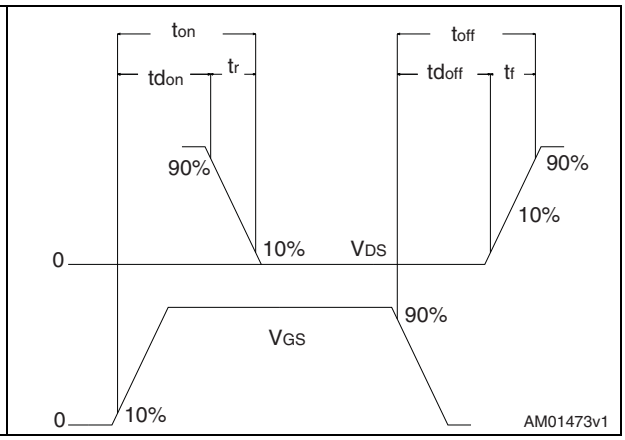


Figure 7. Switching time wave form



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ (3.3 x 3.3) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	
A3		0.20	
b	0.23	0.30	0.38
C		0.328	
C1		0.12	
D		3.30	
D2	2.50	2.65	2.75
E		3.30	
E2	1.25	1.40	1.50
F		1.325	
F1		0.975	
G		0.850	
G1		0.250	

Figure 8. PowerFLAT™ (3.3 x 3.3) drawing

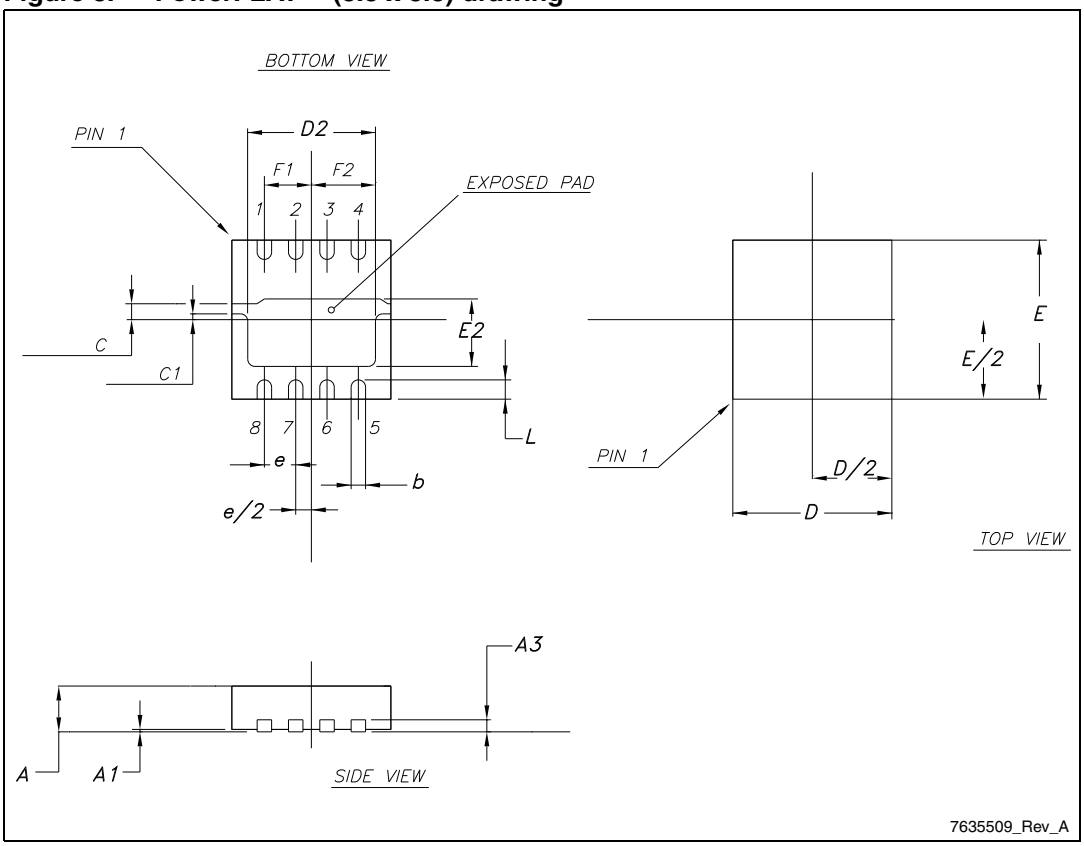
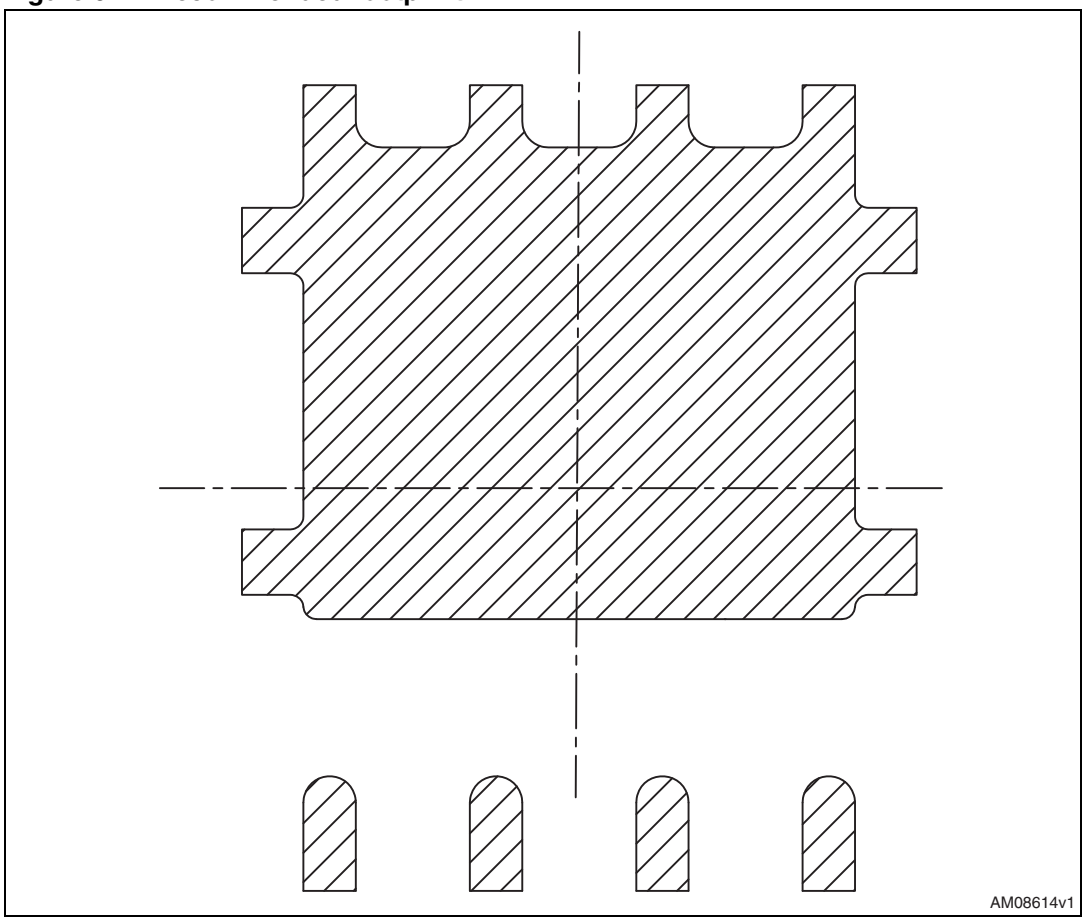


Figure 9. Recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Jun-2011	1	Initial release.

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