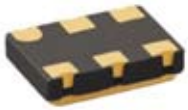
UVV Series
5x7 mm, 3.3 Volt, LVPECL/LVDS, VCXO



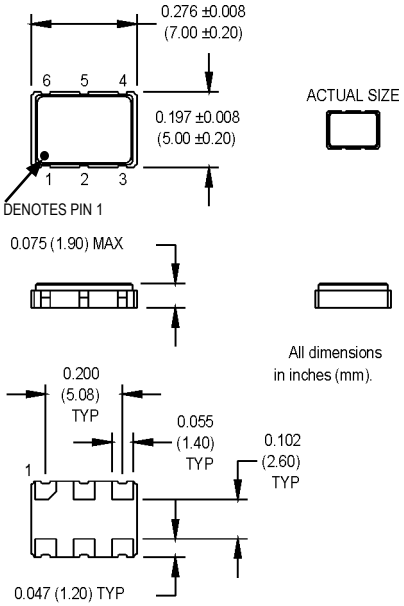
RoHS Compliant

- Versatile VCXO to 800 MHz with good jitter (3 ps typical)
- Used in low jitter clock synthesizers and SONET applications

Ordering Information

UVV 1 0 R 1 L N 00.0000 MHz

- **Product Series**
- **Temperature Range**
  - 1: 0°C to +70°C
  - 2: -40°C to +85°C
  - 6: -20°C to +70°C
  - 8: 0°C to +50°C
- **Stability**
  - 0: Nominal per APR selection
- **Output Type**
  - R: Complementary, Enable
  - Z: Complementary, w/o Enable
- **Absolute Pull Range**
  - 1: ±50 ppm (±35 ppm typ. Stability)
  - 2: ±100 ppm (±20 ppm typ. Stability)
  - 5: ±80 ppm (±25 ppm typ. Stability)
  - 8: ±25 ppm (±50 ppm typ. Stability)
- **Symmetry/Output Logic Type**
  - L: 45/55% LVDS
  - P: 45/55% PECL
  - H: 40/60% LVDS
  - Q: 40/60% PECL
- **Package/Lead Configurations**
  - N: Leadless Ceramic (6 pads)
- **Frequency (customer specified)**



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Enable
3	Ground
4	Output1/ Q
5	Output2/ $\overline{Q}$
6	+Vdd

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Frequency Range	F	0.75		800	MHz	
Operating Temperature	TA	(See ordering information)				
Storage Temperature	TS	-55		+125	°C	
Frequency Stability	ΔF/F	(See ordering information)				See Note 1
Aging						
1st Year		-3/-5		+3/+5	ppm	<52 MHz / ≥52 MHz
Thereafter (per year)		-1/-2		+1/+2	ppm	<52 MHz / ≥52 MHz
Pullability/APR		(See ordering information)				See Note 2
Control Voltage	Vc	0.3	1.65	3	V	Pin 1 Voltage
Linearity			5	15	%	Positive Monotonic Slope
Modulation Bandwidth	fm	10			kHz	-3 dB bandwidth
Input Impedance	Zin	50k			Ohms	
Input Voltage	Vcc	3.135	3.3	3.456	V	
Input Current	Icc					
0.75 MHz to 24 MHz				70/30	mA	PECL/LVDS
24 MHz to 96 MHz				100/60	mA	PELC/LVDS
96 MHz to 800 MHz				110/60	mA	PECL/LVDS
Output Type						PECL/LVDS
Load		50 Ohms to Vcc –2 VDC 100 Ohms differential load				See Note 3 PECL waveform LVDS waveform
Symmetry (Duty Cycle) **(Per Symmetry Code)**		(See ordering Information)				Vcc –1.3 VDC (PECL) 0.5x (Vmax-Vmin) LVDS
Output Skew				200	ps	PECL
Differential Voltage	Vo	250	340	450	mV	LVDS
Logic "1" Level	Voh	Vcc –1.02			V	PECL
Logic "0" Level	Vol			Vcc –1.63	V	PECL
Rise/Fall Time	Tr/Tf		.35 .50	.55 1.0	ns ns	@ 20/80% LVPECL @ 20/80% LVDS
Enable/Disable Logic		80% Vcc min or N/C: output active 20% Vcc max: output disables to high-Z				Output Option R
Start up Time			5		ms	
Phase Jitter	ΦJ		3	5	ps RMS	Integrated 12 kHz – 20 MHz
Phase Noise (Typical)	**10 Hz**	**100 Hz**	**1 kHz**	**20 kHz**	**100 kHz**	**Offset from carrier**
@ 19.44 MHz	-60	-90	-112	-140	-150	dBc/Hz
@ 155.52 MHz	-60	-90	-112	-123	-120	dBc/Hz

1. Stability given for deviation over temperature
2. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.
3. PECL – See load circuit diagram #5 on page 116. LVDS – See load circuit diagram #9 on page 117.