Stereo 2.6W Audio Power Amplifier (With DC_Volume Control)

Features

- **Low Operating Current with 9mA**
- **Improved Depop Circuitry to Eliminate Turn-on and Turn-off Transients in Outputs**
- **High PSRR**
- **32 Steps Volume Adjustable by DC Voltage with Hysteresis**
- **2.6W per Channel Output Power into 4Ω Load at 5V, BTL Mode**
- **Two Output Modes Allowable with BTL and SE Modes Selected by SE/$\overline{\text{BTL}}$ pin**
- **Low Current Consumption in Shutdown Mode (1μA)**
- **Short-Circuit Protection**
- **Thermal Shutdown Protection and Over-Current Protection Circuitry**
- **Maximum Output Swing Clamping Function**
- **The OUT+ Signal and the IN- Signal are Outphase**
- **SOP-16P Packages with Thermal Pad Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

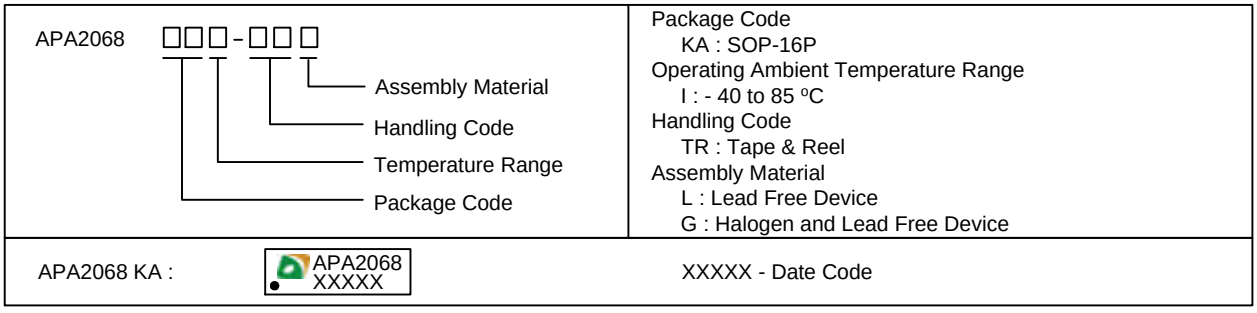
General Description

APA2068 is a monolithic integrated circuit, which provides precise DC volume control, and a stereo bridged audio power amplifiers capable of producing 2.6W (1.8W) into 4Ω with less than 10% (1.0%) THD+N. The attenuator range of the volume control in APA2068 is from 20dB (DC_Vol=0V) to -80dB (DC_Vol=3.54V) with 32 steps. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2068, that reduce pops and clicks noise during power up or shutdown mode operation. It also improves the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design, APA2068 combines a stereo bridge-tied loads ($\overline{\text{BTL}}$) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal.

Applications

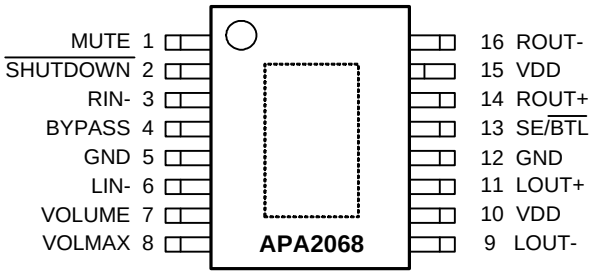
- **NBs**
- **LCD Monitor or TVs**

Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



= Thermal Pad
(Connected to GND for better heat dissipation)

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage Range	-0.3 to 6	V
V_{IN}	Input Voltage Range, SE/$\overline{BTL}$, $\overline{SHUTDOWN}$, MUTE	-0.3 to V_{DD}+0.3	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature,10 Seconds	260	°C
P_D	Power Dissipation	Internal Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance from Junction to Ambient (Note 2) SOP-16P	45	°C/W
θ_{JC}	Thermal Resistance from Junction to Case (Note 3) SOP-16P	10	°C/W

Note 2: The Thermal-Pad on the bottom of the IC should soldered directly to the PCB's Thermal-Pad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Note 3: The case temperature is measured at the center of the Thermal-Pad on the underside of the SOP-16P package.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{DD}	Supply Voltage		4.5	5.5	V
T_A	Operating Ambient Temperature Range		-40	85	°C
T_J	Operating Junction Temperature		-	125	°C
V_{IH}	High Level Threshold Voltage	$\overline{SHUTDOWN}$, MUTE	2	-	V
		SE/$\overline{BTL}$	4	-	

Recommended Operating Conditions (Cont.)

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{IL}	Low Level Threshold Voltage	$\overline{SHUTDOWN}$, MUTE	-	1.0	V
		SE/$\overline{BTL}$	-	1	
V_{ICM}	Common Mode Input Voltage		V_{DD}-1.0	-	V

Electrical Characteristics

V_{DD} = 5V, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2068			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply Current	SE/$\overline{BTL}$=0V	-	9	20	mA
		SE/$\overline{BTL}$=5V	-	4	10	
I_{SD}	Supply Current in Shutdown Mode	SE/$\overline{BTL}$=0V $\overline{SHUTDOWN}$=0V	-	1	-	µA
I_{IH}	High Input Current		-	900	-	nA
I_{IL}	Low Input Current		-	900	-	nA
V_{OS}	Output Differential Voltage		-	5	-	mV
$T_{START-UP}$	Start-Up Time from Shutdown	Bypass Capacitor, C_b=2.2µF	-	1	-	S

Operating Characteristics, BTL mode

V_{DD} = 5V, T_A = 25°C, R_L = 4Ω, Gain = 2V/V (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2068			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD+N=10%, R_L=3Ω, f_{in} = 1kHz	-	2.9	-	W
		THD+N=10%, R_L=4Ω, f_{in} = 1kHz	-	2.6	-	
		THD+N=10%, R_L=8Ω, f_{in} = 1kHz	-	1.6	-	
		THD+N=1%, R_L=3Ω, f_{in} = 1kHz	-	2.4	-	
		THD+N=1%, R_L=4Ω, f_{in} = 1kHz	-	1.8	-	
		THD+N=1%, R_L=8Ω, f_{in} = 1kHz	1	1.3	-	
THD+N	Total Harmonic Distortion Plus Noise	P_O = 1.2W, R_L = 4Ω, f_{in} = 1kHz	-	0.07	-	%
		P_O = 0.9W, R_L = 8Ω, f_{in} = 1kHz	-	0.08	-	
PSRR	Power Ripple Rejection Ratio	V_{rr} = 0.1Vrms, R_L = 8Ω, C_B = 1µF, f_{in} = 120Hz	-	60	-	dB
Crosstalk	Channel Separation	C_B = 1µF, R_L = 8Ω, f_{in} = 1kHz	-	90	-	dB
S/N	Signal to Noise Ratio	P_O = 1.1W, R_L = 8Ω, A_Weighting	-	95	-	dB

Operating Characteristics, SE mode. V_{DD} = 5V,T_A = 25°C, Gain = 1V/V (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2068			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD+N= 10%, R_L = 16Ω, f_{in} = 1kHz	-	220	-	mW
		THD+N= 10%, R_L = 32Ω, f_{in} = 1kHz	-	120	-	
		THD+N = 1%, R_L = 16Ω, f_{in} = 1kHz	-	160	-	
		THD+N = 1%, R_L = 32Ω, f_{in} = 1kHz	-	95	-	

Electrical Characteristics (Cont.)

Operating Characteristics, SE mode. V_{DD} = 5V,T_A = 25°C, Gain = 1V/V (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2068			Unit
			Min.	Typ.	Max.	
THD+N	Total Harmonic Distortion Plus Noise	P_O = 125mW, R_L = 16Ω, f_{in} = 1kHz	-	0.09	-	%
		P_O = 65mW, R_L = 32Ω, f_{in} = 1kHz	-	0.09	-	
PSRR	Power Ripple Rejection Ratio	V_{IN} = 0.1Vrms, R_L = 8Ω, C_B = 1µF, f_{in} = 120Hz	-	60	-	dB
Crosstalk	Channel Separation	C_B = 1µF, R_L = 32Ω, f_{in} = 1kHz	-	60	-	dB
S/N	Signal to Noise Ratio	P_O = 75mW, SE, R_L = 32Ω, A_Weighting	-	100	-	dB

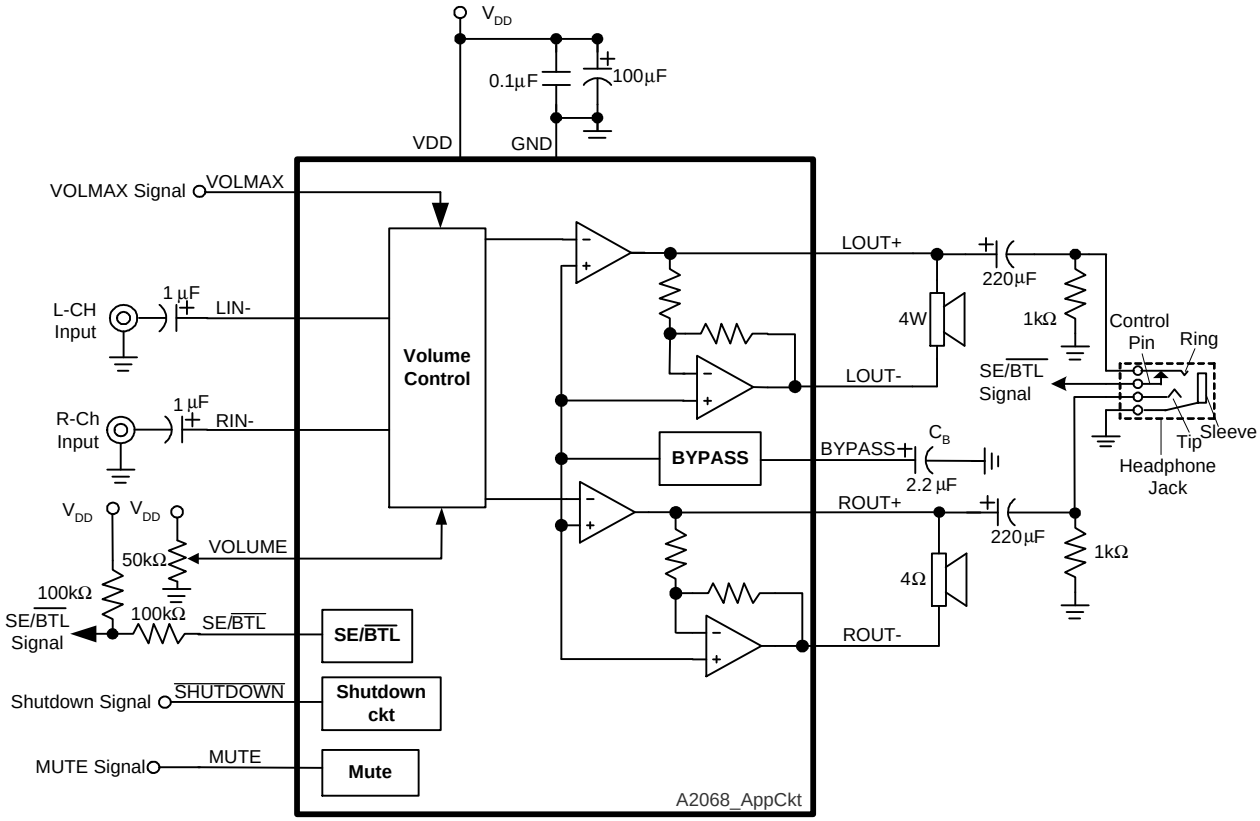
Pin Description

PIN		I/O	FUNCTION
NO.	NAME		
1	MUTE	I	Mute control signal input, hold low for normal operation, hold high to mute.
2	$\overline{\text{SHUTDOWN}}$	I	It will be into shutdown mode when pull low. I_{SD} = 1µA
3	RIN-	I	Right channel input terminal
4	BYPASS	I	Bias voltage generator
5,12	GND	-	Ground connection, Connected to thermal pad.
6	LIN-	I	Left channel input terminal
7	VOLUME	I	Input signal for internal volume gain setting.
8	VOLMAX	I	Setting the maximum output swing. Input a non-zero voltage (V_C) to this pin, the output voltage swing will be clamped between V_{OH} (the maximum positive value) **-** V_C & V_{OL} (the minimum negative value) **+** V_C. Disable this function when tie this pin to GND. Maximum input voltage ≤ 1/2 V_{DD}.
9	LOUT-	O	Left channel negative output in BTL mode and high impedance in SE mode.
10,15	VDD	-	Supply voltage
11	LOUT+	O	Left channel positive output in BTL mode and SE mode.
13	SE/$\overline{\text{BTL}}$	I	Output mode control input, high for SE output mode and low for BTL mode.
14	ROUT+	O	Right channel positive output in BTL mode and SE mode.
16	ROUT-	O	Right channel negative output in BTL mode and high impedance in SE mode.

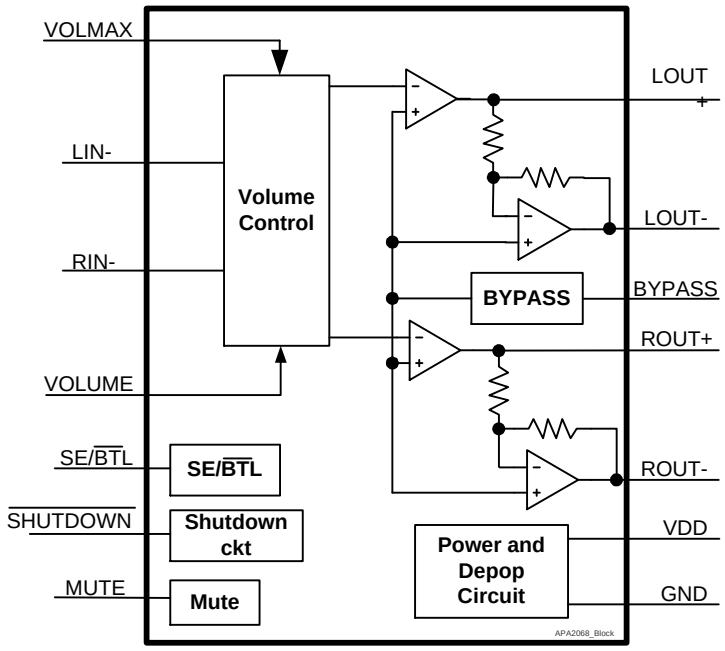
Control Input Table

$\overline{\text{SHUTDOWN}}$	MUTE	SE/$\overline{\text{BTL}}$	Operating Mode
L	X	X	Shutdown mode
H	L	L	BTL out
H	L	H	SE out
H	H	X	Mute

Typical Application Circuit



Block Diagram



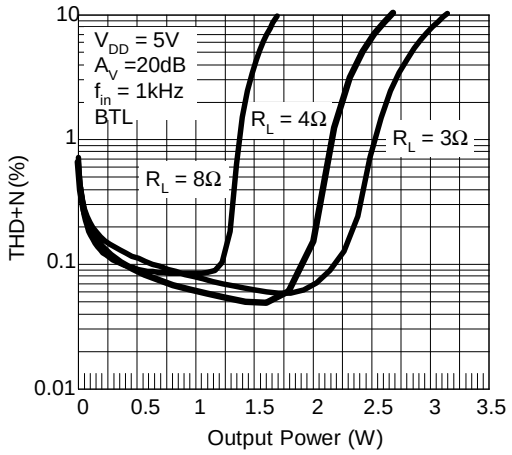
Volume Control Table_BTL Mode

Supply Voltage V_{DD}= 5V

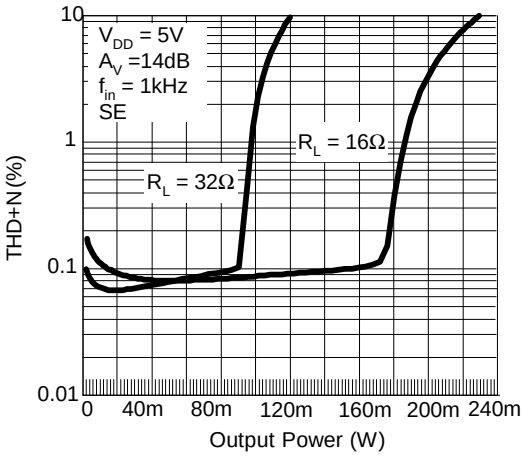
Gain (dB)	High (V)	Low (V)	Hysteresis (mV)	Recommended Voltage (V)
20	0.12	0.00		0
18	0.23	0.17	52	0.20
16	0.34	0.28	51	0.31
14	0.46	0.39	50	0.43
12	0.57	0.51	49	0.54
10	0.69	0.62	47	0.65
8	0.80	0.73	46	0.77
6	0.91	0.84	45	0.88
4	1.03	0.96	44	0.99
2	1.14	1.07	43	1.10
0	1.25	1.18	41	1.22
-2	1.37	1.29	40	1.33
-4	1.48	1.41	39	1.44
-6	1.59	1.52	38	1.56
-8	1.71	1.63	37	1.67
-10	1.82	1.74	35	1.78
-12	1.93	1.85	34	1.89
-14	2.05	1.97	33	2.01
-16	2.16	2.08	32	2.12
-18	2.28	2.19	30	2.23
-20	2.39	2.30	29	2.35
-22	2.50	2.42	28	2.46
-24	2.62	2.53	27	2.57
-26	2.73	2.64	26	2.69
-28	2.84	2.75	24	2.80
-30	2.96	2.87	23	2.91
-32	3.07	2.98	22	3.02
-34	3.18	3.09	21	3.14
-36	3.30	3.20	20	3.25
-38	3.41	3.32	18	3.36
-40	3.52	3.43	17	3.48
-80	5.00	3.54	16	5

Typical Operating Characteristics

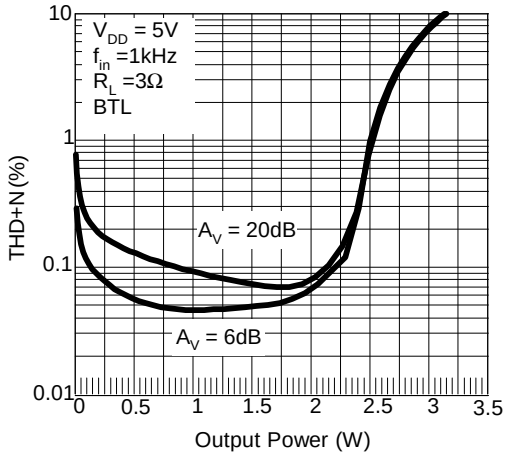
THD+N vs. Output Power



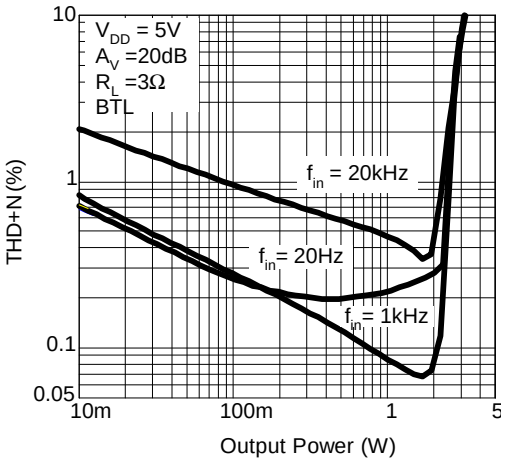
THD+N vs. Output Power



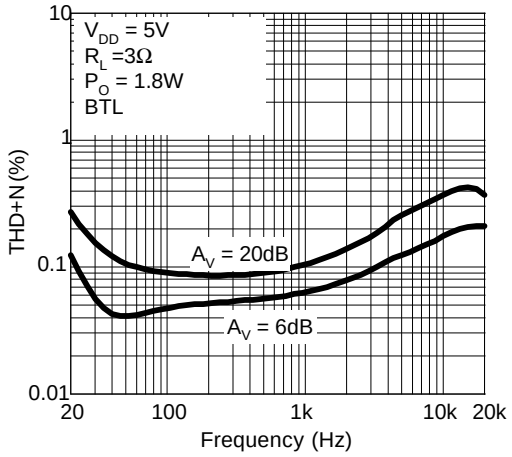
THD+N vs. Output Power



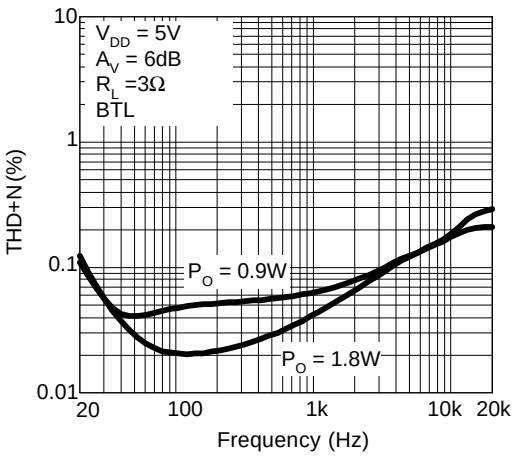
THD+N vs. Output Power



THD+N vs. Frequency

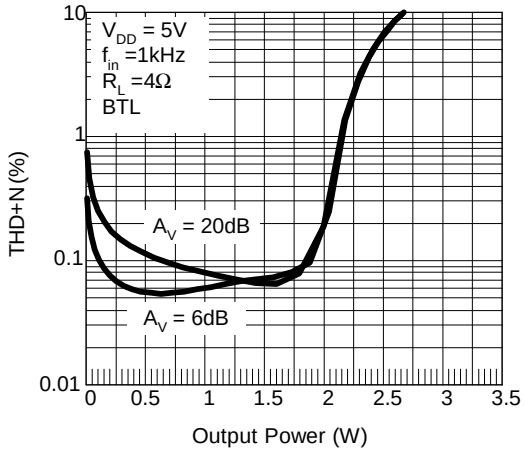


THD+N vs. Frequency

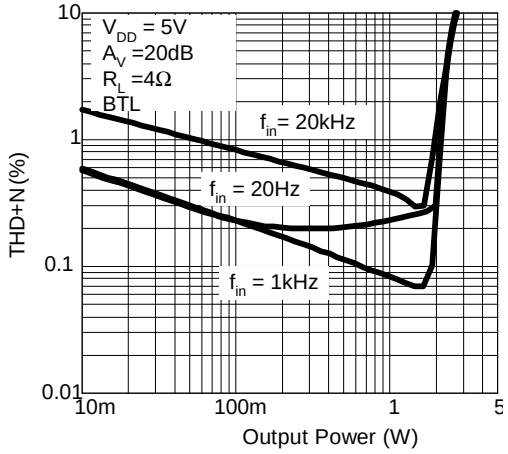


Typical Operating Characteristics (Cont.)

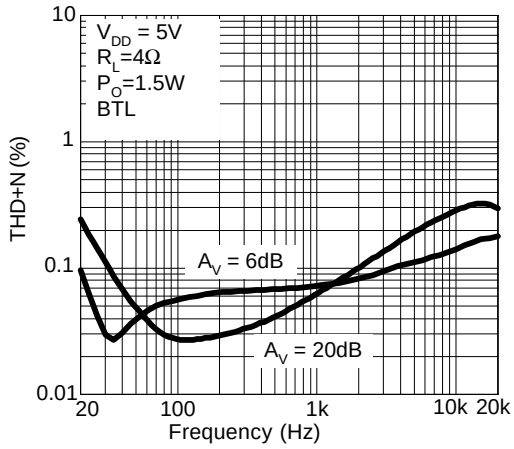
THD+N vs. Output Power



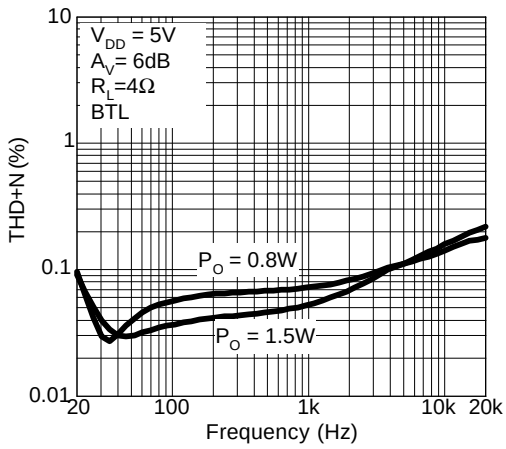
THD+N vs. Output Power



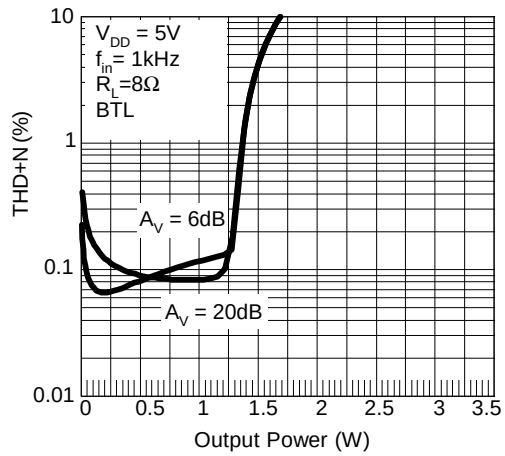
THD+N vs. Frequency



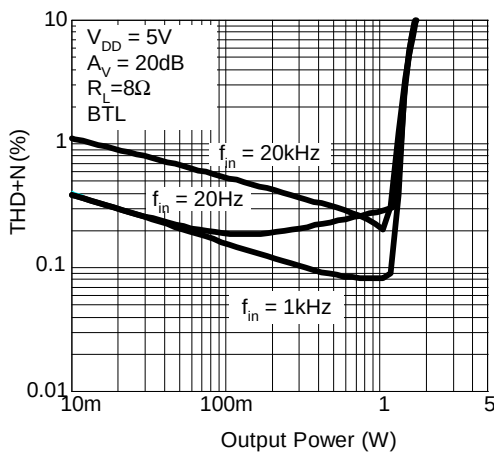
THD+N vs. Frequency



THD+N vs. Output Power

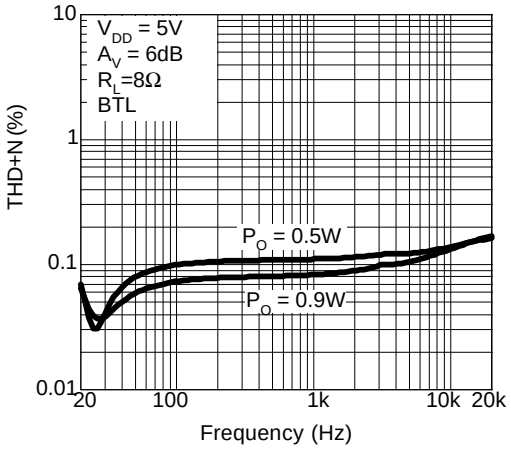


THD+N vs. Output Power

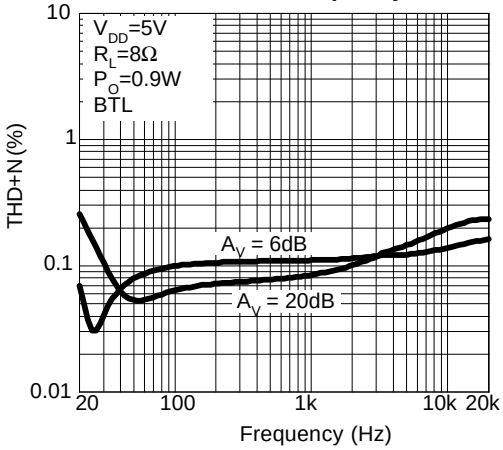


Typical Operating Characteristics (Cont.)

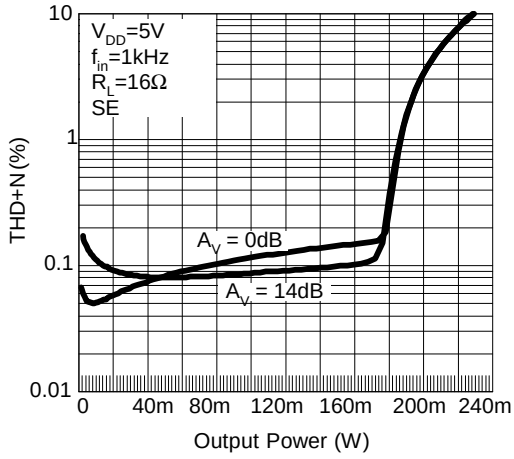
THD+N vs. Frequency



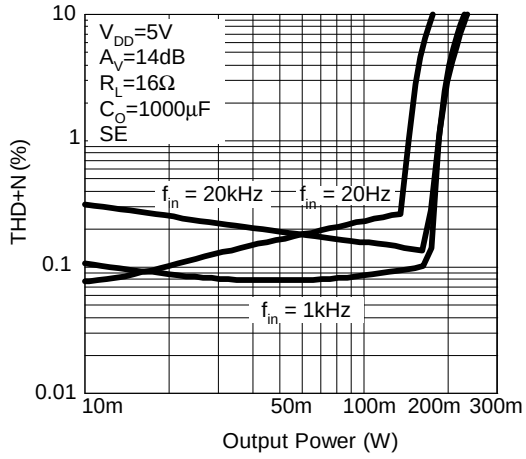
THD+N vs. Frequency



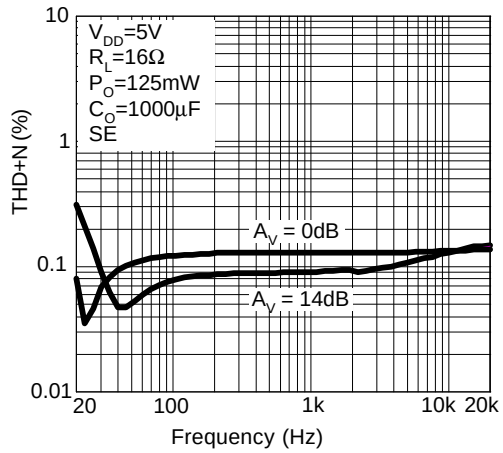
THD+N vs. Output Power



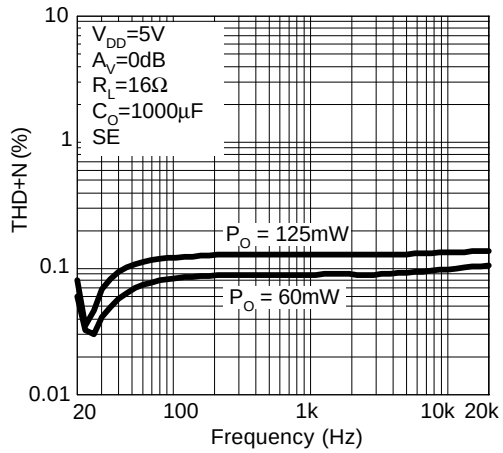
THD+N vs. Output Power



THD+N vs. Frequency

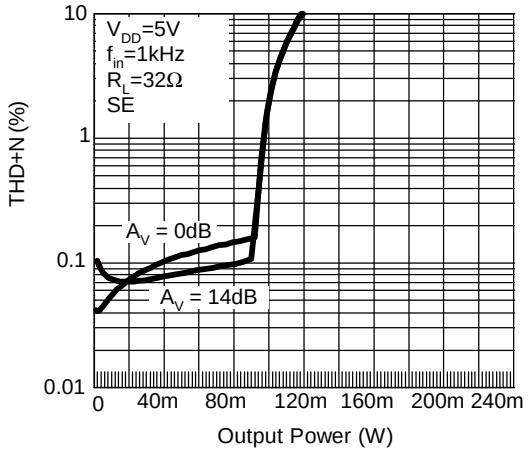


THD+N vs. Frequency

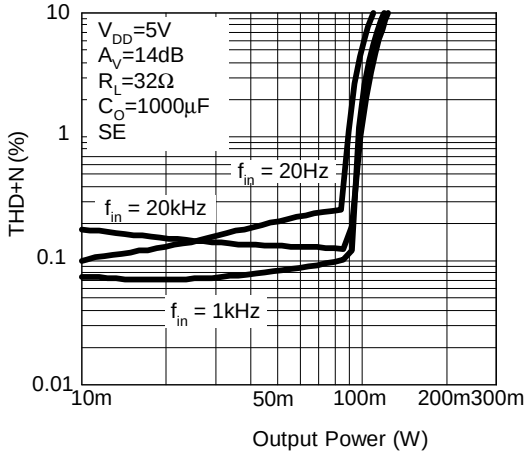


Typical Operating Characteristics (Cont.)

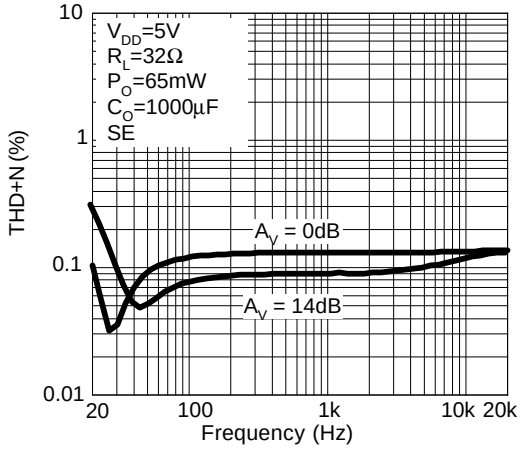
THD+N vs. Output Power



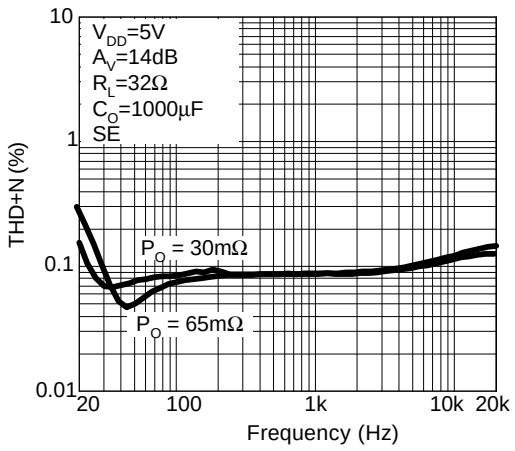
THD+N vs. Output Power



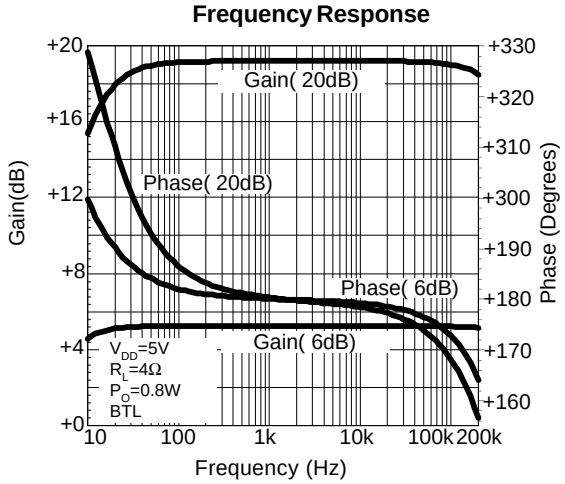
THD+N vs. Frequency



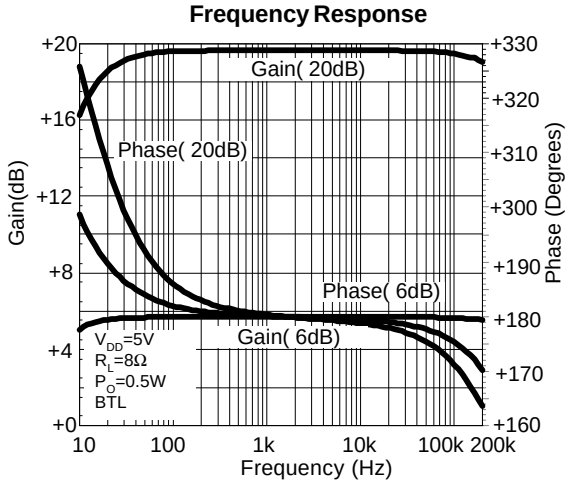
THD+N vs. Frequency



Frequency Response

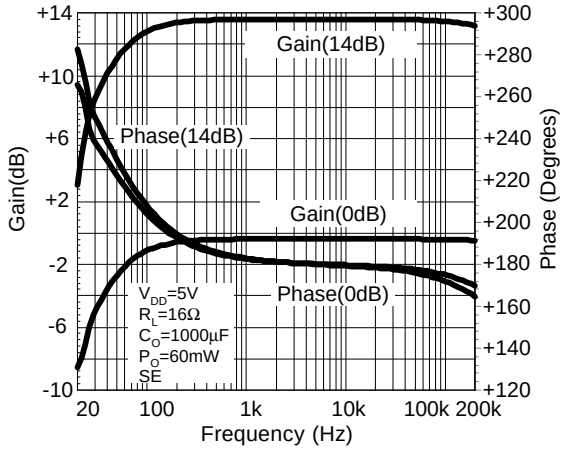


Frequency Response

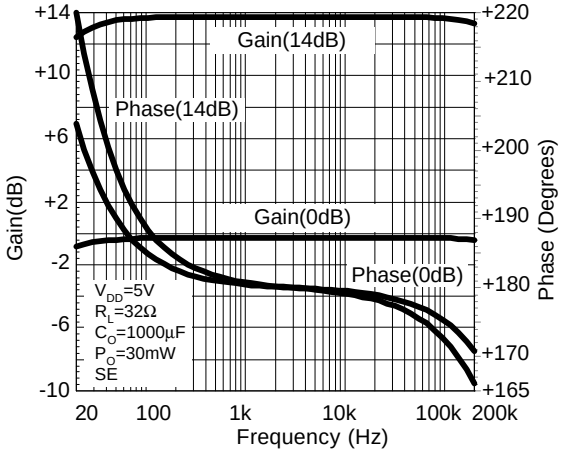


Typical Operating Characteristics (Cont.)

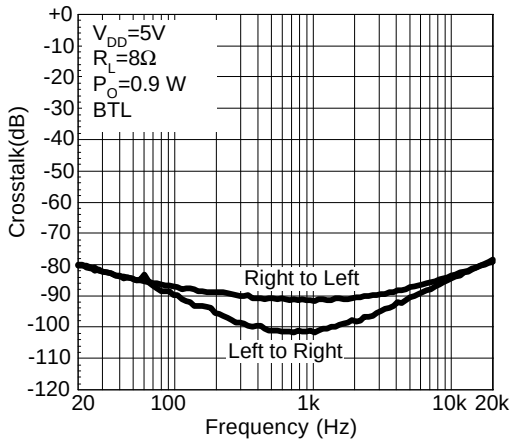
Frequency Response



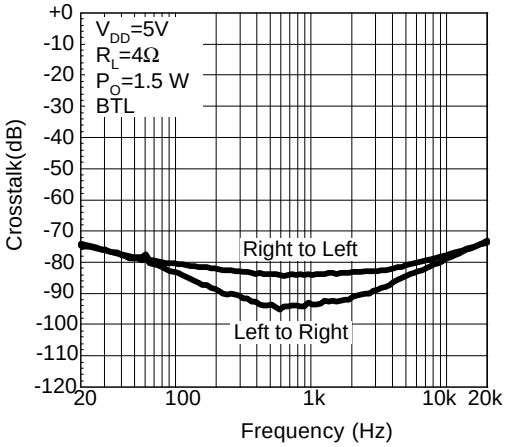
Frequency Response



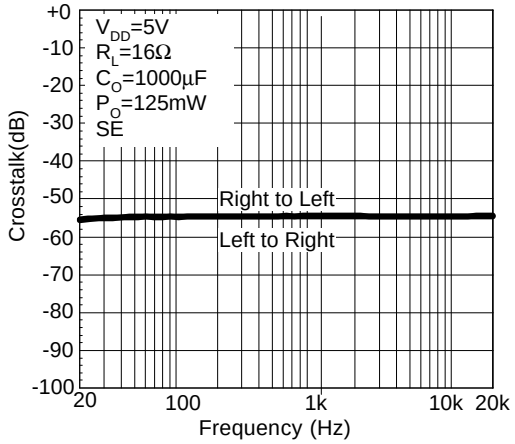
Crosstalk vs. Frequency



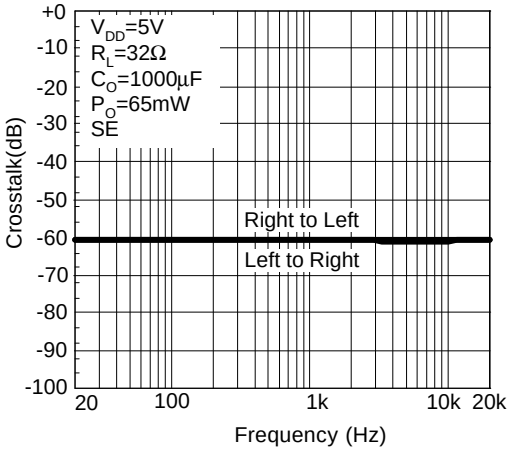
Crosstalk vs. Frequency



Crosstalk vs. Response

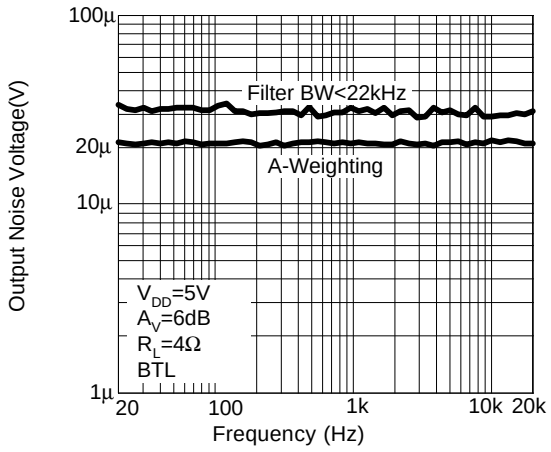


Crosstalk vs. Response

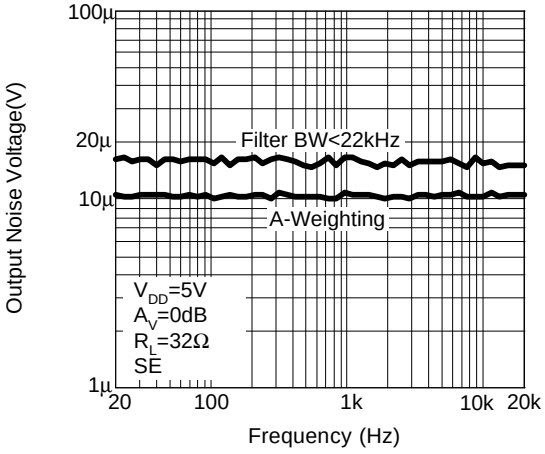


Typical Operating Characteristics (Cont.)

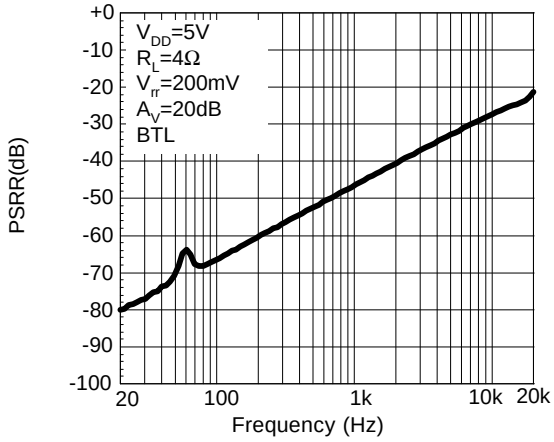
Output Noise Voltage vs. Frequency



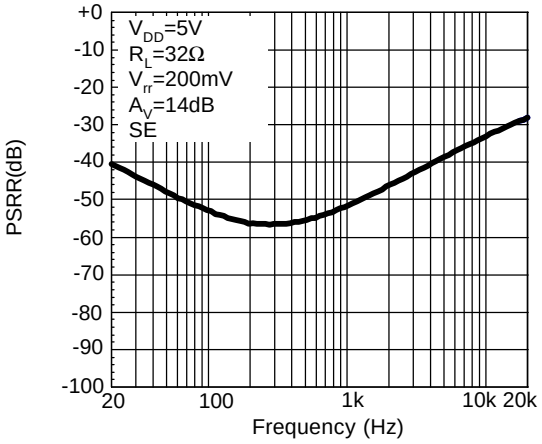
Output Noise Voltage vs. Frequency



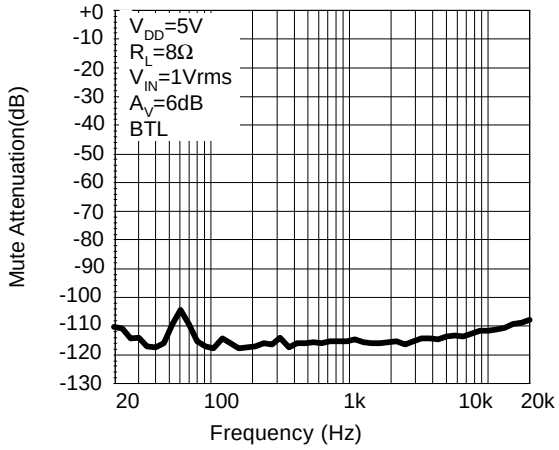
PSRR vs. Frequency



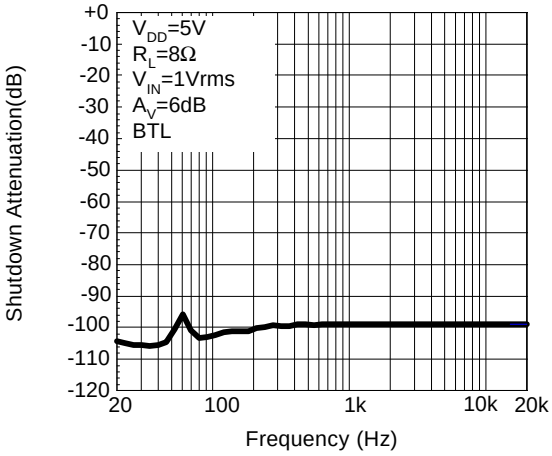
PSRR vs. Frequency



Mute Attenuation vs. Frequency

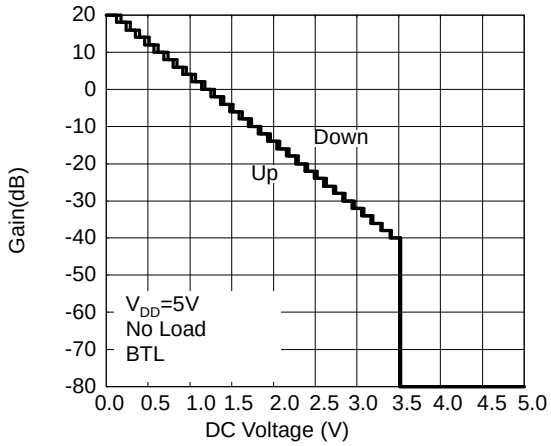


Shutdown Attenuation vs. Frequency

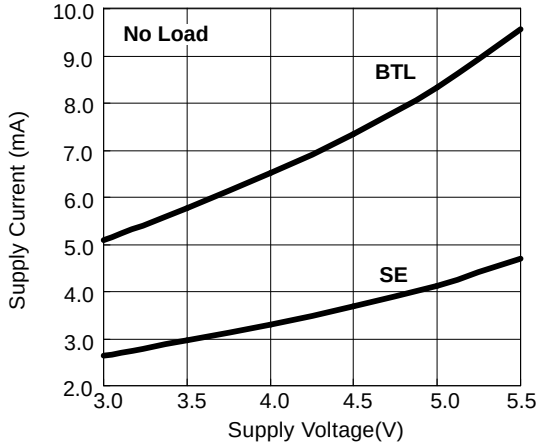


Typical Operating Characteristics (Cont.)

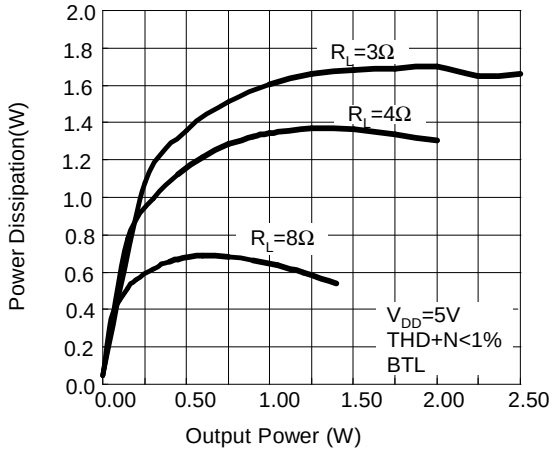
Gain vs. Volume Voltage



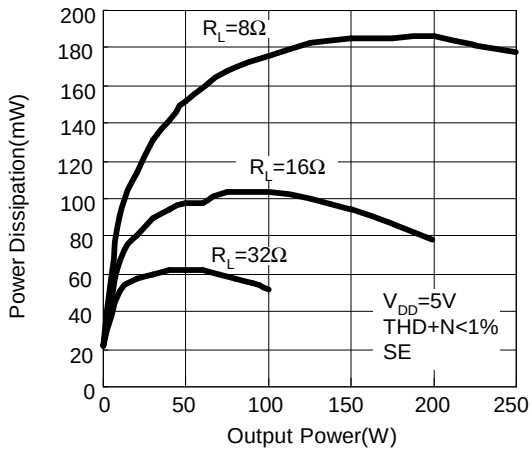
Supply Current vs. Supply Voltage



Power Dissipation vs.Output Power



Power Dissipation vs. Output Power



Application Information

BTL Operation

The APA2068 output stage (power amplifier) has two pairs of operational amplifiers internally, which allows different amplifier configurations.

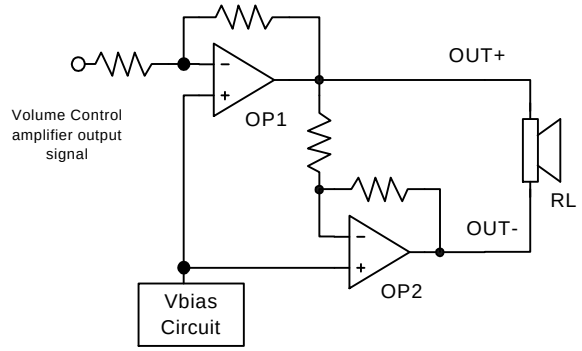


Figure 1: APA2068 Internal Configuration

(each channel)

The power amplifier's OP1 gain is set by internal unity-gain and input audio signal comes from internal volume control amplifier while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude but out of phase 180°. Consequently, the differential gain for each channel is 2 x (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration is commonly referred to bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to the ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus, doubles the output swing for aspecified supply voltage.

When placed under the same conditions, a BTL amplifier has four times the output power of a SE amplifier. A BTL configuration, such as the one used in APA2068, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, it's not necessary for DC voltage to be across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation

To consider the single-supply SE configuration shown Application Circuit, a coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF), so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).The rules described still hold with the addition of the following relationship:

$$\frac{1}{C_B \times 150k\Omega} \leq \frac{1}{R_i C_i} << \frac{1}{R_L C_C} \qquad (1)$$

Output SE/$\overline{\text{BTL}}$ Operation

The best cost saving feature of APA2068 is that it can be switched easily between BTL and SE modes. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Inside of the APA2068, two separate amplifiers drive OUT+ and OUT- (see Figure 1). The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT- and ROUT-.

- When SE/$\overline{\text{BTL}}$ keeps low, the OP2 turns on and the APA2068 is in the BTL mode.
- When SE/$\overline{\text{BTL}}$ keeps high, the OP2 is in a high output impedance state, which configures the APA2068 as SE driver from OUT+. I_{DD} is reduced by approximately one-half in SE mode.

Control of the SE/$\overline{\text{BTL}}$ input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in the Application Circuit.

Application Information (Cont.)

Output SE/$\overline{BTL}$ Operation (Cont.)

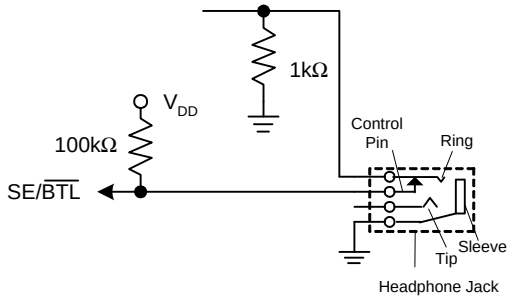


Figure 2: SE/$\overline{BTL}$ Input Selection by Phonejack Plug

In Figure 2, input SE/$\overline{BTL}$ operates as below :
When the phonejack plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{BTL}$ input is pulled high and enables the SE mode. When the input goes high, the OUT- amplifier is shutdown causing the speaker to mute. The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack. When there is no headphone plugged into the system, the contact pin of the headphone jack is connnected from the signal pin, the voltage divider set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/$\overline{BTL}$ pin, enabling the BTL function.

Volume Control Function

The APA2068 has an internal stereo volume control that setting is the function of the DC voltage applied to the VOLUME input pin. The APA2068 volume control consists of 32 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps, controlled by the DC voltage, are from 20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in the volume control graph.

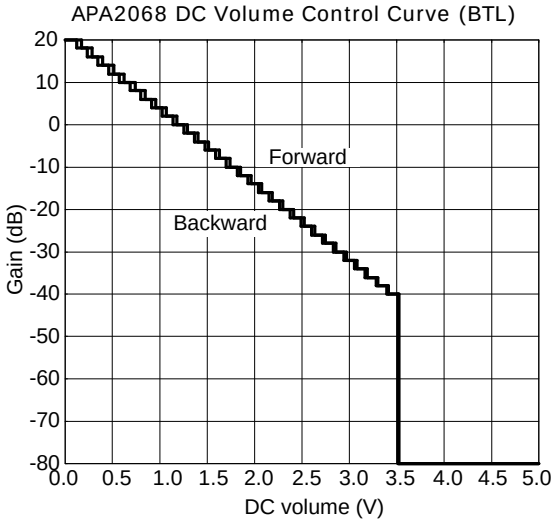


Figure 3: Gain Setting vs. VOLUME Pin Voltage

For the highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gain levels are 2dB/step from 20dB to -40dB in BTL mode, and the last step at -80dB as mute mode.

Input Resistance, R_i

The gain for each audio input of the APA2068 is set by the internal resistors (R_i and R_F) of volume control amplifier in inverting configuration.

$$\text{SE Gain} = A_V = -\frac{R_F}{R_i} \qquad (2)$$

$$\text{BTL Gain} = -2\times\frac{R_F}{R_i} \qquad (3)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. For varying gain settings, the APA2068 generates each input resistance on figure 4. The input resistance will affect the low frequency performance of audio signal. The minmum input resistance is 10kΩ when gain setting is 20dB and the resistance will ramp up when close loop gain below 20dB. The input resistance has wide variation (+/-10%) caused by process variation.

Application Information (Cont.)

Input Resistance, R_i (Cont.)

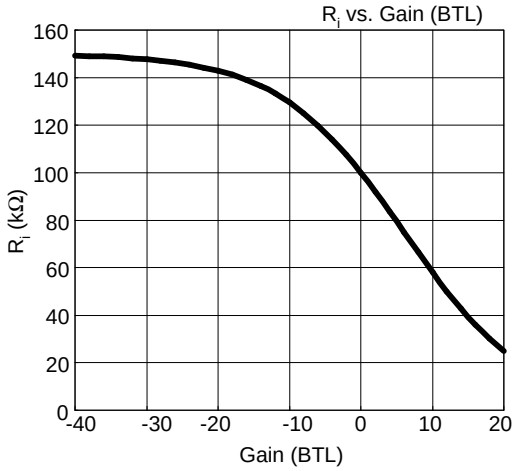


Figure 4: Input Resistance vs. Gain Setting

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i (25kΩ) form a high-pass filter with the corner frequency determined in the following equation :

$$Fc(highpass) = \frac{1}{2\pi \times 25k\Omega \times Ci} \qquad (4)$$

The value of C_i is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where R_i is 25kΩ and the specification calls for a flat bass response down to 50Hz. Equation is reconfigured as below :

$$Ci = \frac{1}{2\pi \times 25k\Omega \times Fc} \qquad (5)$$

When the input resistance variation is considered, the C_i is 0.13μF, therefore, a value in the range of 0.33μF to 1.0μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i+R_F, C_i) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level of the amplifiers' input is held at V_{DD}/2. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

A power amplifier, proper supply bypassing, is critical for low noise performance and high power supply rejection. The capacitor location on the BYPASS pin should be as close to the device as possible. The effect of a larger supply bypass capacitor is to improve PSRR due to increased half-supply stability. Two critical criteria of bypass capacitor (C_B): 1st, it depends upon desired PSRR requirements and click-and-pop performance; 2nd, the leakage current of C_B will induce the voltage drop of V_{BYPASS} (voltage of BYPASS pin), and if the V_{BYPASS} is less than 0.49V_{DD}, APA2068 will enter mute condition. The value of V_{BYPASS} can be calculated as below:

$$V_{BYPASS} = 0.5V_{DD} - I_{Leakage} \times 150k\Omega \qquad (6)$$

Where

$I_{Leakage}$ =Leakage current of C_B

Therefore, it is recommended that C_B's leakage current should be no more then 0.4μA for properly work of APA2068.

To avoid the start-up pop noise, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation should be maintained.

$$\frac{1}{(C_B \ X150k\Omega)} << \frac{1}{C_i X150k\Omega} \qquad (7)$$

The capacitor is fed from a 150kΩ resistor inside of the amplifier and the 150kΩ is the maximum input resistance of (R_i+R_F). Bypass capacitor, C_B, values of 2.2μF to 10μF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N and noise performance. The bypass capacitance also affects the start up time. It is determined in the following equation:

$$Tstart\ up = 5X(C_{BYPASS} X150k\Omega) \qquad (8)$$

Output Coupling Capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by the equation.

$$Fc(highpass) = \frac{1}{2\pi R_L C_C} \qquad (9)$$

Application Information (Cont.)

Output Coupling Capacitor, C_C (Cont.)

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage, from a performance standpoint, is the load impedance and is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load.

Power Supply Decoupling, C_S

The APA2068 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, it is recommended to place a large aluminum electrolytic capacitor of 10µF or greater near the audio power amplifier.

Optimizing Depop Circuitry

Circuitry has been included in the APA2068 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry.

The value of C_i will also affect turn-on pops (Refer to Effective Bypass Capacitance). The bypass voltage ramp up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of C_{BYPASS} can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_{BYPASS}, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_{BYPASS} and the turn-on time. In a SE configuration, the output coupling capacitor, C_C, is of particular concern.

This capacitor discharges through the internal 10KΩ resistors. Depending on the size of C_C, the time constant can be relatively large. To reduce transients in SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current. In most cases, choosing a small value of C_i in the range of 0.33µF to 1µF, Cb being equal to 4.7µF and an external 1kΩ resistor should be placed in parallel with the internal 10kΩ resistor should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain, so it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption when not in use, the APA2068 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the $\overline{\text{SHUTDOWN}}$ pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between the ground and the supply V_{DD} to provide maximum device performance.

By switching the $\overline{\text{SHUTDOWN}}$ pin to low, the amplifier enters a low-current state, I_{DD}<1µA. APA2068 is in shutdown mode. On normal operating, $\overline{\text{SHUTDOWN}}$ pin pull to high level to keep the IC out of the shutdown mode. The $\overline{\text{SHUTDOWN}}$ pin should be tied to a definite voltage to avoid unwanted state changing.

Mute Function

The APA2068 mutes the amplifier outputs when logic high is applied to the MUTE pin. Applying logic low to the MUTE pin returns the APA2068 to normal operation. Prevent unanticipated mute behavior by connecting the Mute pin to logic high or low. Do not let the Mute pin float.

Application Information (Cont.)

Maximum Output Swing Clamping Function (VolMax)

The APA2068 provides the maximum output swing clamping function to protect the speaker.

When input a non-zero voltage (V_X) to VolMax pin, BTL mode output amplitude (V_{OP}) is be limited at $V_{OP}=V_{DD}-2V_X$. SE mode output amplitude (V_{OP}) is be limited at $V_{OP}=1/2V_{DD}-2V_X$. This function can effectively limite the output power across the speaker and avoid damaging the speaker.

The maximum setting voltage of VolMax is Vdd/2, and when this function is not used, connect the VolMax to the GND.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load.

The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{1}{P_{SUP}} \quad (10)$$

Where

$$P_O = \frac{V_{orms} \times V_{orms}}{R_L} = \frac{(V_P \times V_P)}{2R_L}$$

$$V_{orms} = \frac{V_P}{\sqrt{2}} \quad (11)$$

$$P_{SUP} = V_{DD} \times L_{DDSVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (12)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \frac{(\frac{V_P \times V_P}{2R_L})}{(V_{DD} \times \frac{2V_P}{\pi R_L})} = \frac{\pi V_P}{4V_{DD}} \quad (13)$$

Table 1 calculates efficiencies for four different output power levels.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range.

Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Table 1: Efficiency vs. Output Power in 5-V/8Ω BTL Systems.

Po (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

**High peak voltages cause the THD+N to increase.

Power Dissipation

Whether the power amplifier is operated in BTL or SE mode, power dissipation is the major concern. Equation14 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode: } P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \quad (14)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus, the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \quad (15)$$

Since the APA2068 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depend on the mode of operation. Even with this substantial increase in power dissipation, the APA2068 does not require extra heatsink. The power dissipation from equation14, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation16:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (16)$$

Application Information (Cont.)

Power Dissipation (Cont.)

For SOP16-P package with thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of APA2068 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation16.

Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Consideration

The thermal pad must be connected to the ground. The package with thermal pad of the APA2068 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA2068 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the APA2068 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA2068 junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions.

To calculate maximum ambient temperatures, first consideration is that the numbers from the **Power Dissipation vs. Output Power** graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature (T_{JMAX}), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2068 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs.

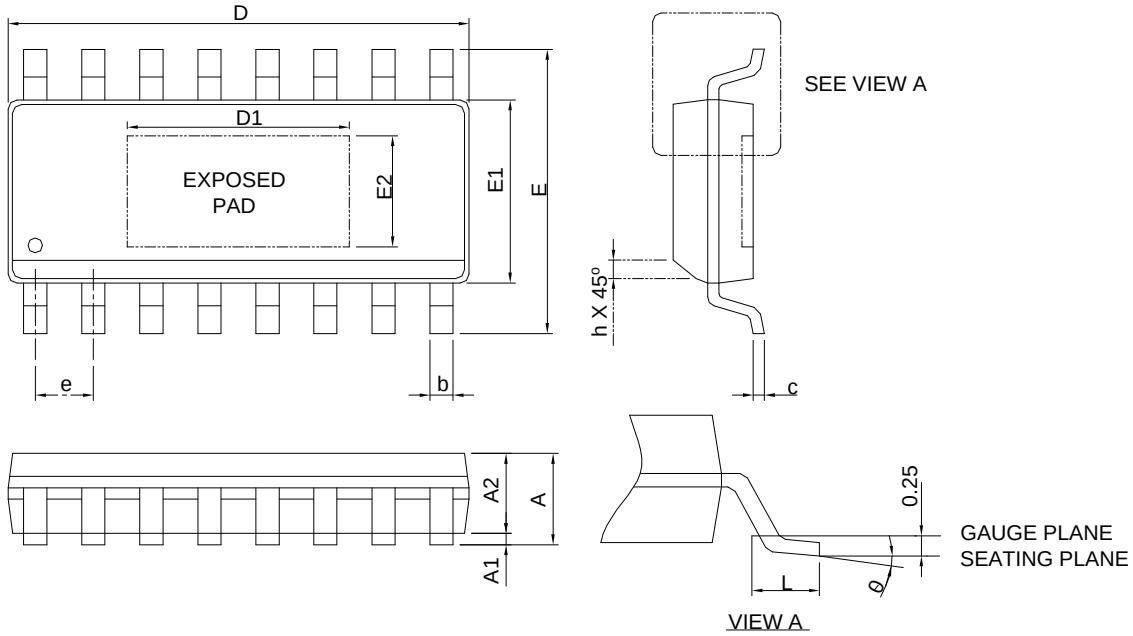
$$T_{AMax} = T_{JMax} - \theta_{JA} P_D \quad (16)$$

150 - 45(0.8*2) = 78°C

The APA2068 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

Package Information

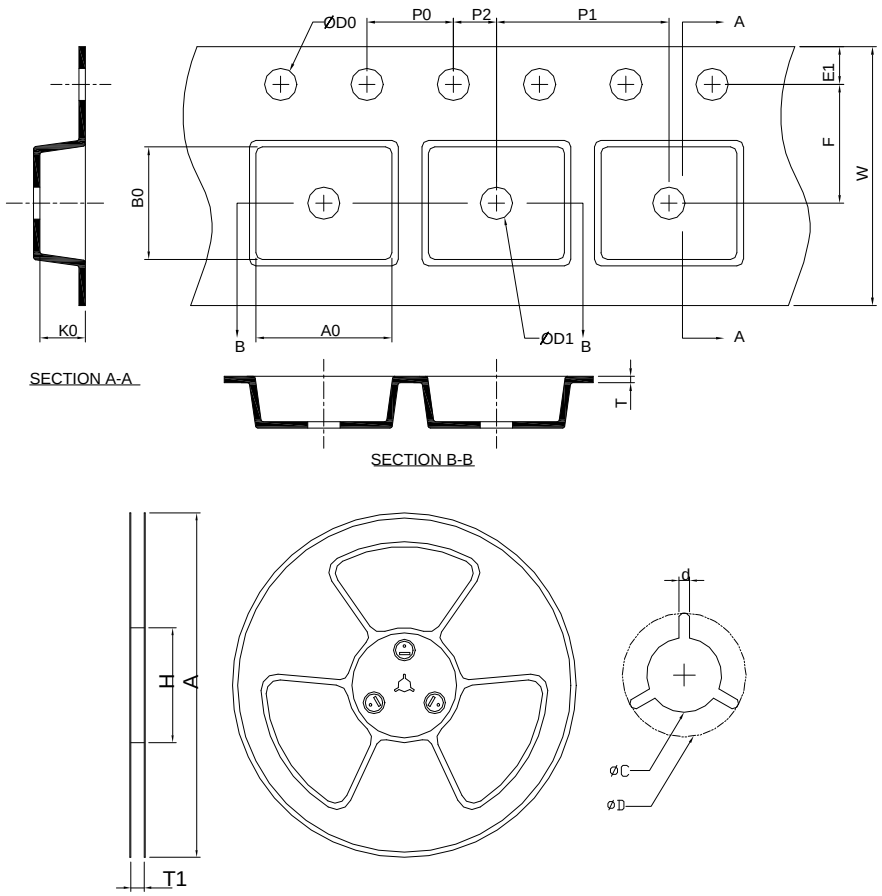
SOP-16P



SYMBOL	SOP-16P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	9.80	10.00	0.386	0.394
D1	3.50	4.50	0.138	0.177
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow from JEDEC MS-012 BC.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-16P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	10.30±0.20	2.10±0.20

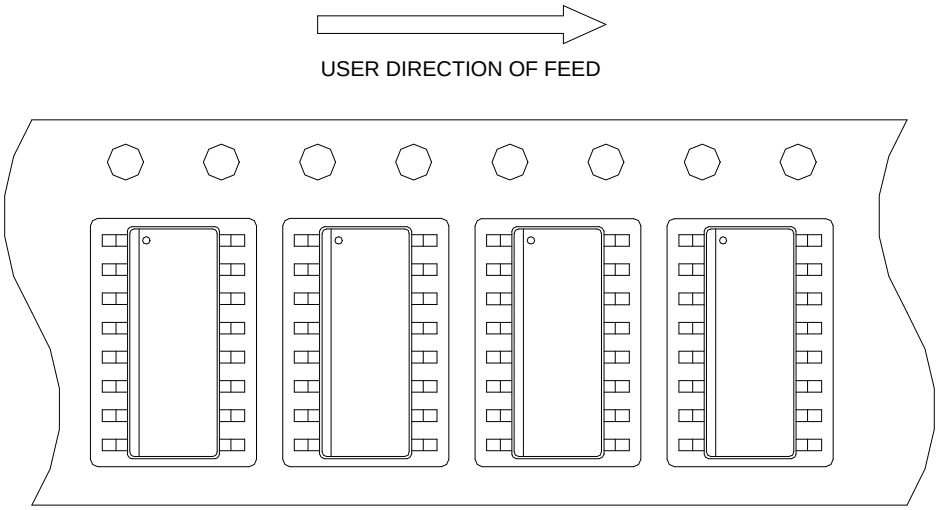
(mm)

Devices Per Unit

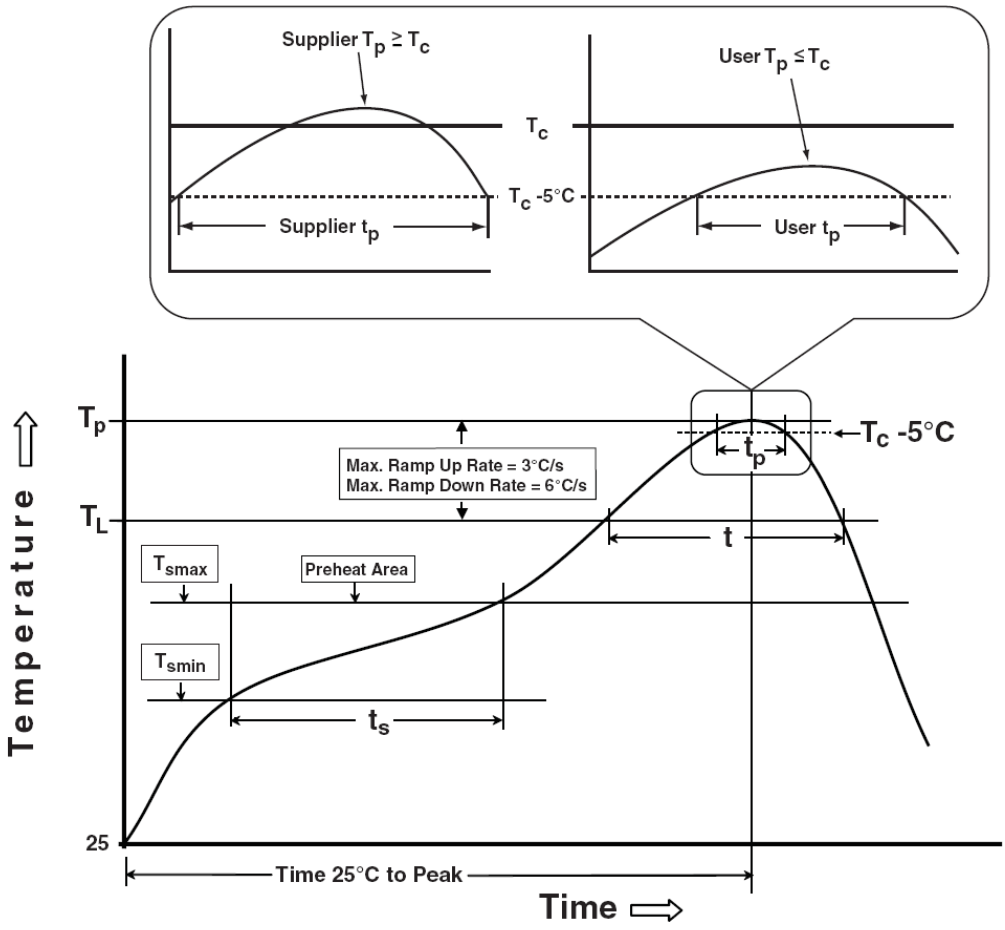
Package Type	Unit	Quantity
SOP-16P	Tape & Reel	2500

Taping Direction Information

SOP-16P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838