

μ PA2738GR

P-channel MOSFET

-30 V, -10 A, $15 \text{ m}\Omega$

R07DS1321EJ0100 Rev.1.00 Jan 25, 2016

Description

The μ PA2738GR is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- $V_{DSS} = -30 \text{ V } (T_A = 25^{\circ}\text{C})$
- Low on-state resistance
 - --- R_{DS(on)} = 15 mΩ MAX. (V_{GS} = -10 V, I_D = -10 A)
- 4.5 V Gate-drive available
- Small and surface mount package (SOP-8)
- Pb-free and Halogen free



SOP-8

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μ PA2738GR-E1-AX	Ni / Pd / Au	Tono 2500 n/rool	SOP-8
μ PA2738GR-E2-AX	INI/Pu/Au	Tape 2500 p/reel	0.085 g TYP.

Absolute Maximum Ratings ($T_A = 25$ °C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	-30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	∓20	V
Drain Current (DC)	I _{D(DC)}	∓10	Α
Drain Current (pulse) *1	I _{D(pulse)}	∓100	Α
Total Power Dissipation *2	P _{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P _{T2}	2.5	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	−55 to +150	°C
Single Avalanche Current *3	I _{AS}	10	Α
Single Avalanche Energy *3	E _{AS}	10	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2 R_{th(ch-A)} 114 °C/W

Notes: *1. PW \leq 10 μ s, Duty Cycle \leq 1%

*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

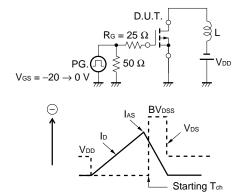
*3. Starting T_{ch} = 25°C, V_{DD} = -15 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C)

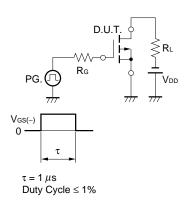
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			-1	μΑ	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			∓100	nA	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate Cut-off Voltage	$V_{GS(off)}$	-1.0		-2.5	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Forward Transfer Admittance *1	y _{fs}	4			S	$V_{DS} = -10 \text{ V}, I_{D} = -5.0 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		12	15	mΩ	$V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$
Resistance *1	R _{DS(on)2}		19	29	mΩ	$V_{GS} = -4.5 \text{ V}, I_D = -10 \text{ A}$
Input Capacitance	C _{iss}		1450		pF	$V_{DS} = -10 \text{ V},$
Output Capacitance	Coss		710		pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		650		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		14		ns	$V_{DD} = -15 \text{ V}, I_D = -5.0 \text{ A},$
Rise Time	t _r		30		ns	$V_{GS} = -10 \text{ V},$
Turn-off Delay Time	t _{d(off)}		60		ns	$R_G = 10 \Omega$
Fall Time	t _f		50		ns	
Total Gate Charge	Q_{G}		37		nC	$V_{DD} = -24 \text{ V},$
Gate to Source Charge	Q_{GS}		2.5		nC	$V_{GS} = -10 \text{ V},$
Gate to Drain Charge	Q_{GD}		20		nC	$I_D = -10 \text{ A}$
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.86		V	I _F = 10 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		47		ns	$I_F = 10 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		43		nC	di/dt = 100 A/μs

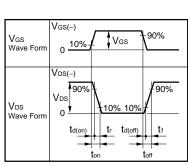
Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME





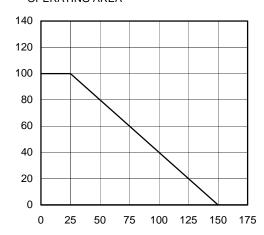
TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. \\ \hline \\ IG = -2 \text{ mA} \\ \hline \\ \hline \\ PG. \\ \hline \\ \end{array}$$

dT - Percentage of Rated Power - %

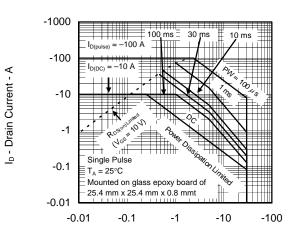
TYPICAL CHARACTERISTICS (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



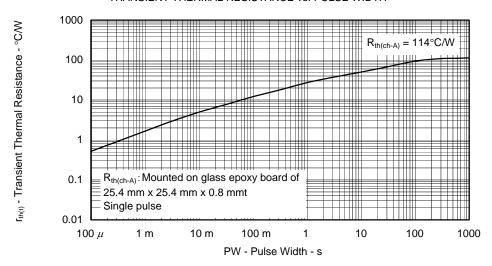
T_A - Ambient Temperature - °C

FORWARD BIAS SAFE OPERATING AREA

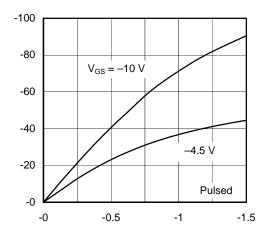


V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

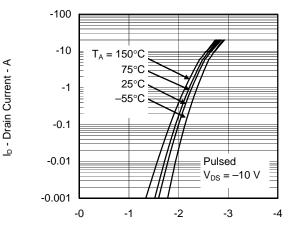


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS



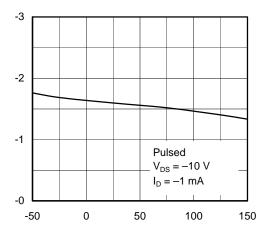
V_{GS} - Gate to Source Voltage - V

I_D - Drain Current - A

V_{GS(off)} - Gate to Source Cut-off Voltage - V

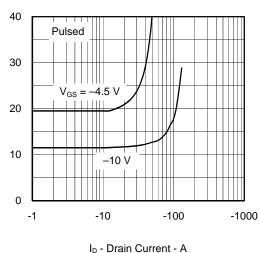
 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$

GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

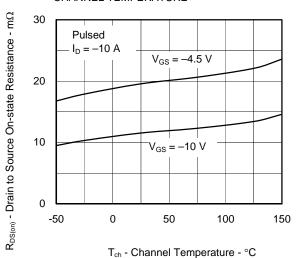


T_{ch} - Channel Temperature - °C

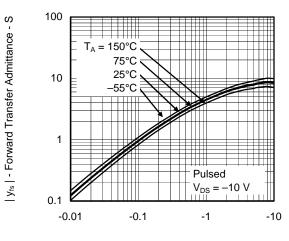
DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

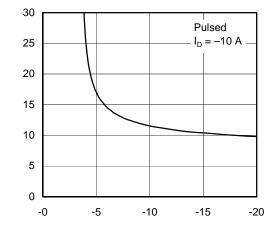


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



ID - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

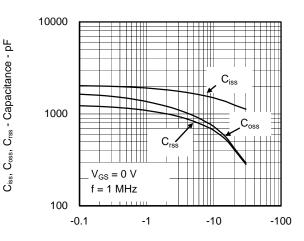


R_{DS(on)} - Drain to Source On-state Resistance - mΩ

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V_{GS} - Gate to Source Voltage - V

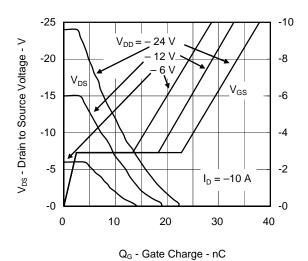
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



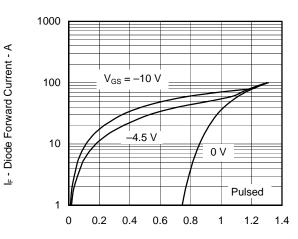
V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



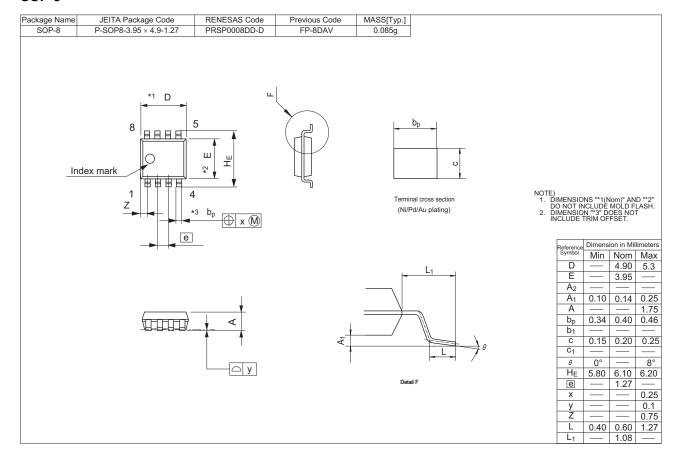




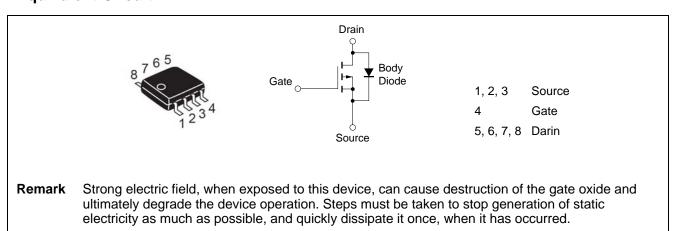
 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

Package Drawings (Unit: mm)

SOP-8



Equivalent Circuit



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