CISCO ONLY

Description

The 8T49N234 has one fractional-feedback PLL that can be used as a jitter attenuator and frequency translator. It is equipped with one integer and one fractional output divider, allowing the generation of up to two different output frequencies, ranging from 8kHz to 1GHz. These frequencies are completely independent of each other, the input reference frequencies and the crystal reference frequency. The device places virtually no constraints on input to output frequency conversion, supporting all FEC rates, including the new revision of ITU-T Recommendation G.709 (2009), most with 0ppm conversion error. The outputs may select among LVPECL, LVDS, HCSL or LVCMOS output levels.

This makes it ideal to be used in any frequency synthesis application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates.

The 8T49N234 accepts one differential or single-ended input clock and a fundamental-mode crystal input. The internal PLL can lock to the input reference clock or just to the crystal to behave as a frequency synthesizer. A second input reference (FBIN) is used as the external feedback input for zero delay buffer functionality.

The device monitors both input references for Loss-of-Signal (LOS), and generates an alarm when an input reference failure is detected.

The PLL has a register-selectable loop bandwidth from 0.2Hz to 6.4kHz. The device starts up with output Q0 set to 12MHz, and output Q1 set to 6MHz. Loop bandwidth is set to 25Hz. Input clock, CLK is set to 6MHz.

The device supports output enable, inputs and Lock and LOS status outputs.

The device is programmable through an I^2C interface.

Typical Applications

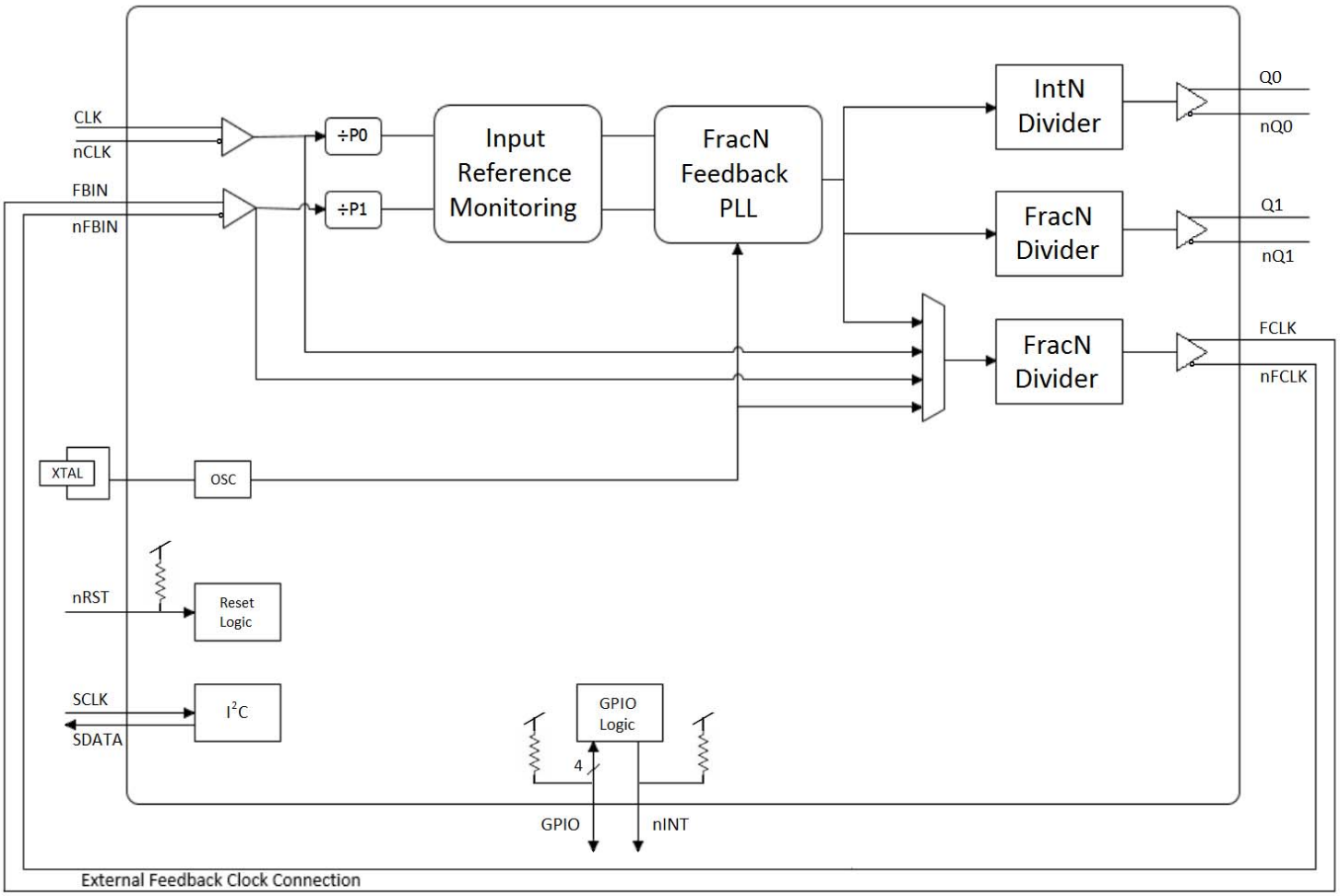
- OTN or SONET / SDH equipment
- Gigabit and Terabit IP switches / routers including Synchronous Ethernet
- Video broadcast

Features

- Supports SDH/SONET and Synchronous Ethernet clocks including all FEC rate conversions
- 480fs RMS typical jitter (including spurs): 12kHz to 5MHz
- Operating modes: synthesizer, jitter attenuator
- Operates from a 10MHz to 50MHz fundamental-mode crystal or a 10MHz to 125MHz external oscillator
- Accepts one LVPECL, LVDS, LVHSTL or LVCMOS input clock
  - Accepts frequencies ranging from 8kHz to 875MHz
  - Clock input monitoring
- Generates two LVPECL / LVDS / HCSL or four LVCMOS device outputs
  - Output frequencies ranging from 8kHz up to 1.0GHz (differential)
  - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
  - One integer divider ranging from ÷4 to ÷786,420
  - Three fractional output dividers (see Output Dividers)
- Programmable loop bandwidth settings from 0.2Hz to 6.4kHz
  - Optional fast-lock function
- Four general purpose I/O pins with optional support for status & control:
  - Two output enable control inputs provide control over the device outputs
  - Lock and Loss-of-Signal alarm outputs
- Open-drain Interrupt pin
- Register programmable through I^2C
- Full 2.5V or 3.3V supply modes, 1.8V support for LVCMOS outputs, GPIO and control pins
- -40°C to 85°C ambient operating temperature
- Package: 40QFN, lead-free (RoHS 6)

Block Diagram

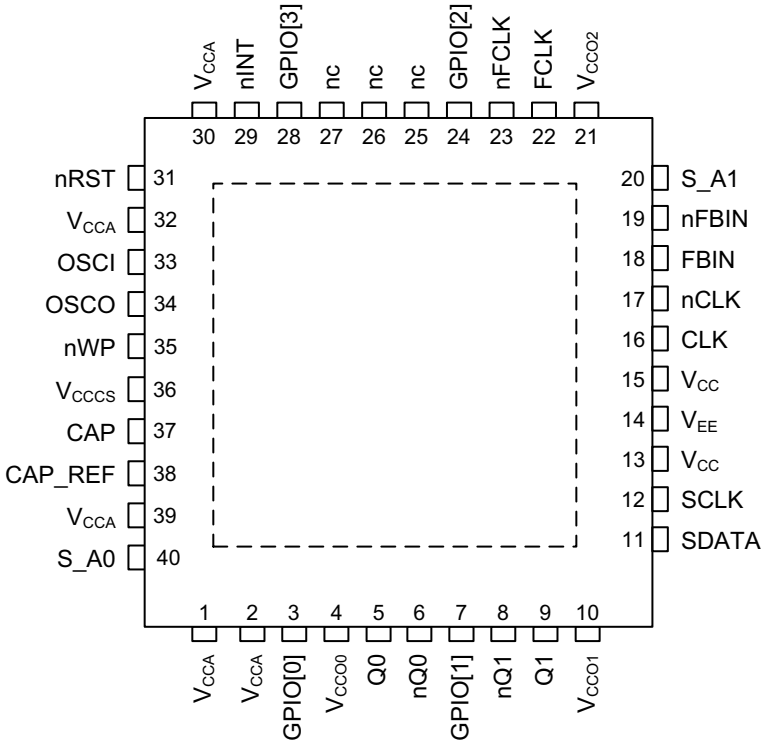
Figure 1: Block Diagram



8T49N234 transistor count: 454,200

Pin Assignments

Figure 2: Pin Assignments for 6mm x 6mm 40-Lead Package



Pin Description Tables

Table 1: Pin Descriptions

Number	Name	Type[a]	Description
1	V_{CCA}	Power	Analog function supply for core analog functions. 2.5V or 3.3V supported.
2	V_{CCA}	Power	Analog function supply for analog functions associated with the PLL. 2.5V or 3.3V supported.
3	GPIO[0]	I/O (PU)	General-purpose input-output. LVTTL / LVCMOS input levels.
4	V_{CCO0}	Power	High-speed output supply for output pair Q0, nQ0. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
5	Q0	O (Universal)	Clock output. Please refer to the Output Drivers for additional details.
6	nQ0	O (Universal)	Clock output. Please refer to the Output Drivers for additional details.
7	GPIO[1]	I/O (PU)	General-purpose input-output. LVTTL / LVCMOS input levels.
8	nQ1	O (Universal)	Clock output. Please refer to the Output Drivers for additional details.
9	Q1	O (Universal)	Clock output. Please refer to the Output Drivers for additional details.

Table 1: Pin Descriptions

Number	Name	Type[a]	Description
10	V_{CCO1}	Power	High-speed output supply for output pair Q1, nQ1. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
11	SDATA	I/O (PU)	I^2C interface bi-directional data.
12	SCLK	I/O (PU)	I^2C interface bi-directional clock.
13	V_{CC}	Power	Core digital function supply. 2.5V or 3.3V supported.
14	V_{EE}	Power	Negative supply voltage. All V_{EE} pins and EPAD must be connected before any positive supply voltage is applied.
15	V_{CC}	Power	Core digital function supply. 2.5V or 3.3V supported.
16	CLK	I (PD)	Non-inverting differential clock input.
17	nCLK	I (PU/ PD)	Inverting differential clock input. V_{CC} / 2 when left floating (set by internal pullup / pulldown resistors).
18	FBIN	I (PD)	Non-inverting differential feedback clock input. Connect to FCLK, or the output of an external feedback divider, depending on application.
19	nFBIN	I (PU/ PD)	Inverting differential feedback clock input. Connect to nFCLK, or the output of an external feedback divider, depending on application. V_{CC} / 2 when left floating (set by internal pullup / pulldown resistors).
20	S_A1	I (PD)	I^2C Address Bit A1.
21	V_{CCO2}	Power	High-speed output supply voltage for output pair FCLK, nFCLK. 2.5V or 3.3V supported.
22	FCLK	O	Differential clock output pair. LVPECL levels. Connect to FBIN for the pre-configured frequency.
23	nFCLK	O	Differential clock output pair. LVPECL levels. Connect to nFBIN for the pre-configured frequency.
24	GPIO[2]	I/O (PU)	General-purpose input-output. LVTTL / LVCMOS Input levels.
25	nc	Unused	Do not connect.
26	nc	Unused	Do not connect.
27	nc	Unused	Do not connect.
28	GPIO[3]	I/O (PU)	General-purpose input-output. LVTTL / LVCMOS Input levels.
29	nINT	O	Interrupt output.
30	V_{CCA}	Power (Open-drain with pullup)	Analog function supply for analog functions associated with PLL. 2.5V or 3.3V supported.
31	nRST	I	Master Reset input. LVTTL / LVCMOS interface levels: 0 = All registers and state machines are reset to their default values.
32	V_{CCA}	Power	Analog function supply for core analog functions. 2.5V or 3.3V supported.

Table 1: Pin Descriptions

Number	Name	Type[a]	Description
33	OSCI	I	Crystal input. Accepts a 10MHz – 50MHz reference from a clock oscillator or a 12pF fundamental mode, parallel-resonant crystal. For proper device functionality, a crystal or external oscillator must be connected to this pin.
34	OSCO	O	Crystal output. This pin must be connected to a crystal. If an oscillator is connected to OSCI, then this pin must be left unconnected.
35	nWP	I	Write protect input. LVTTL / LVCMOS interface levels. 0 = Write operations on the serial port will complete normally, but will have no effect except on interrupt registers. 1 = Serial port writes may change any register.
36	V_{CCCS}	Power	Output supply for control & status pins: GPIO[3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST 1.8V, 2.5V or 3.3V supported
37	CAP	Analog	PLL external capacitance. A 0.1µF capacitance value across CAP and CAP_REF pins is recommended.
38	CAP_REF	Analog	PLL external capacitance. A 0.1µF capacitance value across CAP and CAP_REF pins is recommended.
39	V_{CCA}	Power	Analog function supply for analog functions associated with PLL. 2.5V or 3.3V supported.
40	S_A0	I	I^2C Address bit A0.
ePAD	Exposed Pad	Power	Negative supply voltage. All V_{EE} pins and ePAD must be connected before any positive supply voltage is applied.

a. Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. *Pullup* and *Pulldown* refer to internal input resistors. See Table 26, *DC Input/ Output Characteristics,* for typical values.

Principles of Operation

The 8T49N234 can be locked to the input clock and generate a wide range of synchronized output clocks.

It could be used for example in either the transmit or receive path of Synchronous Ethernet equipment.

The 8T49N234 accepts one differential or single-ended input clock ranging from 8kHz up to 875MHz. It generates up to two output clocks ranging from 8kHz up to 1.0GHz.

The PLL path within the 8T49N234 supports two states: Lock and Free-run. The Lock status may be monitored on register bits and pins. In the locked state, the PLL locks to a valid clock input and its output clocks have a frequency accuracy equal to the frequency accuracy of the input clock. In the Free-run state, the PLL outputs a clock with the same frequency accuracy as the external crystal.

Upon power up, the PLL will enter Free-run state, in this state it generates output clocks with the same frequency accuracy as the external crystal. The 8T49N234 continuously monitors the clock input for activity (signal transitions). If no input reference is provided, the device will remain locked to the crystal in Free-run state and will generate output frequencies as a synthesizer.

When an input clock has been validated, the PLL will transition to the Lock state.

The device supports conversion of any input frequencies to two different independent output frequencies.

The 8T49N234 has a programmable loop bandwidth from 0.2Hz to 6.4kHz.

In default configuration, the device looks for a 6MHz input clock. The device starts up with output Q0 set to 12MHz and output Q1 set to 6MHz. Loop bandwidth is set to 25Hz.

The device monitors both input references and generates an alarm when an input clock failure is detected on either CLK or FBIN inputs.

The device is programmable through an I^2C interface and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory.

Crystal Input

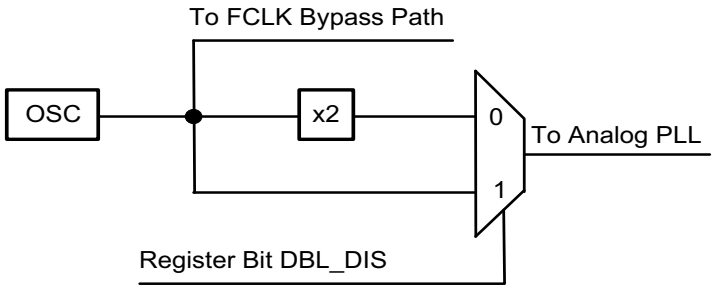
The crystal input on the 8T49N234 is capable of being driven by a parallel-resonant, fundamental mode crystal with a frequency range of 10MHz – 50MHz.

The oscillator input also supports being driven by a single-ended crystal oscillator or reference clock.

The long term drift will depend on the quality of the crystal or oscillator attached to this port.

This device provides the ability to double the crystal frequency input into the PLL for improved close-in phase noise performance. Refer to Figure 3.

Figure 3: Doubler Block Diagram



Bypass Path

The crystal input or either reference input (CLK or FBIN) may be used directly as a clock source for the FCLK output dividers. This may only be done for input frequencies of 250MHz or less.

Input Clock Selection

The 8T49N234 accepts the input clock with frequencies ranging from 8kHz up to 875MHz. The input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ±100ppm or better, except where gapped clock inputs are used.

Input Clock Monitor

The clock input is monitored for Loss-of-Signal (LOS). If no activity has been detected on the clock input within a user-selectable time period then the clock input is considered to be failed and an internal Loss-of-Signal status flag is set. The user-selectable time period has sufficient range to allow a gapped clock missing many consecutive edges to be considered a valid input.

User-selection of the clock monitor time-period is based on a counter driven by a monitor clock. The monitor clock is fixed at the frequency of the PLL's VCO divided by 8. With a VCO range of 3GHz – 4GHz, the monitor clock has a frequency range of 375MHz to 500MHz.

The monitor logic for the input reference will count the number of monitor clock edges indicated in the appropriate Monitor Control register. If an edge is received on the input reference being monitored, then the count resets and begins again. If the target edge count is reached before an input reference edge is received, then an internal soft alarm is raised and the count re-starts. During the soft alarm period, the PLL tracking will not be adjusted. If an input reference edge is received before the count expires for the second time, then the soft alarm status is cleared and the PLL will resume adjustments. If the count expires again without any input reference edge being received, then a Loss-of-Signal alarm is declared.

It is expected that for normal (non-gapped) clock operation, users will set the monitor clock count for each input reference to be slightly longer than the nominal period of that input reference. A margin of 2 – 3 monitor clock periods should give a reasonably quick reaction time and yet prevent false alarms.

For gapped clock operation, the user will set the monitor clock count to a few monitor clock periods longer than the longest expected clock gap period. The monitor count registers support 17-bit count values, which will support at least a gap length of two clock periods for any supported input reference frequency, with longer gaps being supported for faster input reference frequencies. Since gapped clocks usually occur on input reference frequencies above 100MHz, gap lengths of thousands of periods can be supported.

Using this configuration for a gapped clock, the PLL will continue to adjust while the normally expected gap is present, but will freeze once the expected gap length has been exceeded and alarm after twice the normal gap length has passed.

Once a LOS on either CLK or FBIN is detected, the appropriate internal LOS alarm will be asserted and it will remain asserted until that input clock returns and is validated. Validation occurs once 8 rising edges have been received on that input reference. If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation period starts over.

Each LOS flag may also be reflected on one of the GPIO[3:0] outputs. Changes in status of any reference can also generate an interrupt if not masked.

Input to Output Clock Frequency

The 8T49N234 is designed to accept any frequency within its input range and generate two different output frequencies that are independent from the input frequencies and from each other. The internal architecture of the device ensures that most translations will result in the exact output frequency specified. Please contact IDT for configuration software or other assistance in determining if a desired configuration will be supported exactly.

Synthesizer Mode Operation

The device may act as a frequency synthesizer with the PLL generating its operating frequency from just the crystal input. By setting the SYN_MODE register bit and setting the STATE[1:0] field to Free-run, no input clock references are required to generate the desired output frequencies.

When operating as a synthesizer, the precision of the output frequency will be <1ppb for any supported configuration.

Loop Filter and Bandwidth

The 8T49N234 uses one external capacitor of fixed value to support its loop bandwidth. When operating in Synthesizer mode a fixed loop bandwidth of approximately 200kHz is provided.

When not operating as a synthesizer, the 8T49N234 will support a range of loop bandwidths: 0.2Hz, 0.4Hz, 0.8Hz, 1.6Hz, 3.2Hz, 6.4Hz, 12Hz, 25Hz, 50Hz, 100Hz, 200Hz, 400Hz, 800Hz, 1.6kHz or 6.4kHz.

The device supports two different loop bandwidth settings: acquisition and locked. These loop bandwidths are selected from the list of options described above. If enabled, the acquisition bandwidth is used while lock is being acquired to allow the PLL to “fast-lock”. Once locked the PLL will use the locked bandwidth setting. If the acquisition bandwidth setting is not used, the PLL will use the locked bandwidth setting at all times.

Output Dividers

The 8T49N234 supports one integer output divider and one fractional output divider. The integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in Table 2.

An output synchronization via the PLL_SYN bit is necessary after programming the output dividers to ensure that the outputs are synchronized.

Table 2: Output Divide Ratios

1st-Stage Divide	2nd-Stage Divide	Total Divide	Minimum F_{OUT} (MHz)	Maximum F_{OUT} (MHz)
4	1	4	750	1000
5	1	5	600	800
6	1	6	500	666.7
4	2	8	375	500
5	2	10	300	400
6	2	12	250	333.3
4	4	16	187.5	250
5	4	20	150	200
6	4	24	125	166.7
...				
4	131,070	524,280	0.0057	0.0076
5	131,070	655,350	0.0046	0.0061
6	131,070	786,420	0.0038	0.0051

Fractional Output Divider Programming (Q1 and FCLK)

For the FracN output divider Q1 the output divide ratio is given by:

- Output divide ratio = (N.F)x2
- N = Integer part: 4, 5, ...(2^{18}–1)
- F = Fractional part: [0, 1, 2, ...(2^{28}–1)]/(2^{28})

For integer operation of these output dividers, N = 3 is also supported for the full output frequency range.

The minimum output divide ratio defined above is valid for all CLK_SEL modes.

Output Divider Frequency Sources

Output dividers associated with the Q[1:0] outputs take their input frequency directly from the PLL.

Output dividers associated with the FCLK outputs can take their input frequencies from the PLL, CLK or FBIN input reference frequency or the crystal frequency.

Output Drivers

The Q[1:0] clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, either output can support LVCMOS, LVPECL, HCSL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V V_{CCO}.

Each output may be enabled or disabled by register bits and/or GPIO pins.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q & nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions can be disabled via register programming:

- Any unused output, including all output divider logic, can be individually powered-off.
- Any unused input, including the clock monitoring logic can be individually powered-off.
- The digital PLL can be powered-off when running in synthesizer mode.
- Clock gating on logic that is not being used.

Status / Control Signals and Interrupts

The status and control signals for the device, may be operated at 1.8V, 2.5V or 3.3V as determined by the voltage applied to the V_{CCCS} pins. All signals will share the same voltage levels.

Signals involved include: nWP, nINT, nRST, GPIO[3:0], S_A0, S_A1, SCLK and SDATA. The voltage used here is independent of the voltage chosen for the digital and analog core voltages and the output voltages selected for the clock outputs.

General-Purpose I/Os & Interrupts

The 8T49N234 provides four General Purpose Input / Output (GPIO) pins for miscellaneous status & control functions. Each GPIO may be configured as either an input or an output. Each GPIO may be directly controlled from register bits or be used as a predefined function as shown in Table 3. Note that the default state prior to configuration being loaded from internal OTP will be to set each GPIO to input direction to function as an output enable.

Table 3: GPIO Configuration[a]

GPIO Pin	Configured as Input		Configured as Output	
	Fixed Function	General Purpose	Fixed Function	General Purpose
3	–	GPI[3] (default)	LOL	GPO[3]
2	–	GPI[2]	LOS[0] (default)	GPO[2]
1	OSEL[1] (default)	GPI[1]	LOS[1]	GPO[1]
0	OSEL[0] (default)	GPI[0]	–	GPO[0]

a. GPI[x]: General purpose input. Logic state on GPIO[x] pin is directly reflected in GPI[x] register.
LOL: Loss-of-Lock status flag for digital PLL. Logic-high indicates digital PLL not locked.
GPO[x]: General purpose output. Logic state is determined by value written in register GPO[x].
OSEL[n]: Output enable control signals for outputs Qx, nQx. Refer to Output Enable Operation section.
LOS[x]: Loss-of-Signal status flag for input reference (0 = CLK, 1 = FBIN). Logic-high indicates input reference failure.

If used in the fixed-function mode of operation, the GPIO bits will reflect the real-time status of their respective status bits as shown in Table 3.

The LOL alarm will support two modes of operation:

- De-asserts once PLL is locked, or
- De-asserts after PLL is locked and all internal synchronization operations that may destabilize output clocks are completed.

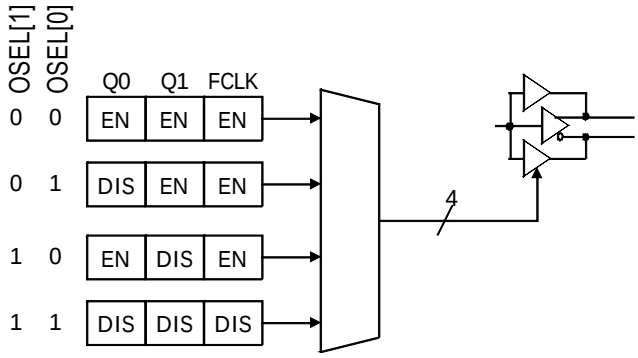
Interrupt Functionality

Interrupt functionality includes an interrupt status flag for each of PLL Loss-of-Lock status (LOL) and Loss-of-Signal status for each input (LOS[1:0]). Those status flags are set whenever there is an alarm on their respective functions. The status flag will remain set until the alarm has been cleared and a ‘1’ has been written to the Status Flag’s register location or if a reset occurs. Each status flag will also have an Interrupt Enable bit that will determine if that Status Flag is allowed to cause the device interrupt status to be affected (enabled) or not (disabled). All interrupt enable bits will be in the disabled state after reset. The device interrupt status flag and nINT output pin are asserted if any of the enabled interrupt status flags are set.

Output Enable Operation

When GPIO[1:0] are used as output enable control signals, the function of the pins is to select one of four register-based maps that indicate which outputs should be enabled or disabled.

Figure 4: Output Enable Map Operation



Device Hardware Configuration

The8T49N234 supports an internal One-Time Programmable (OTP) memory that is pre-programmed at the factory with one complete device configuration. This pre-programmed configuration will be loaded into the device's registers on power-up or reset.

These default register settings can be over-written using the serial programming interface once reset is complete. Any configuration written via the serial programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a different factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The 8T49N234 has an internal power-up reset (POR) circuit and a master reset input pin nRST. If either is asserted, the device will be in the Reset State.

For highly programmable devices, it's common practice to reset the device immediately after the initial power-on sequence. IDT recommends connecting the nRST input pin to a programmable logic source for optimal functionality. It is recommended that a minimum pulse width of 10ns be used to drive the nRST input.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- The GPIO signals will be configured as output enable inputs.
- All clock outputs will be disabled.
- All interrupt status and interrupt enable bits will be cleared, negating the nINT signal.

Upon the later of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load its configuration using the data stored in the internal One-Time Programmable (OTP) memory.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the crystal and begin operation. Once the PLL is locked, all the outputs derived from it will be synchronized and output phase adjustments can then be applied if desired.

Serial Control Port Description

Serial Control Port Configuration Description

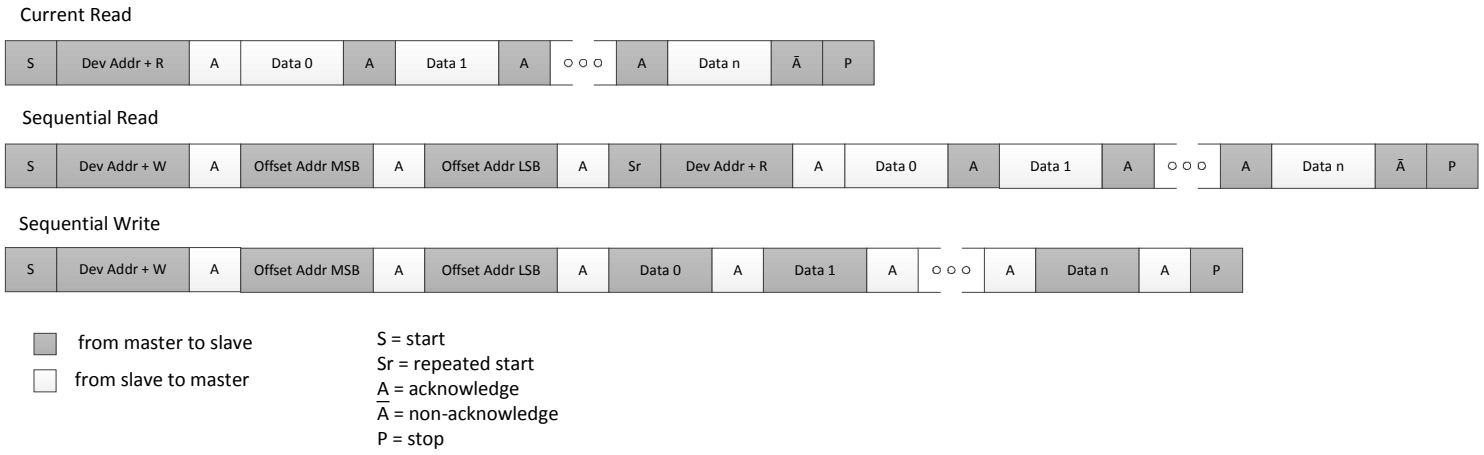
The device has a serial control port capable of responding as a slave in an I²C compatible configuration, to allow access to any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details.

I²C Mode Operation

The I²C interface is designed to fully support v1.2 of the I²C specification for normal and fast mode operation. The device acts as a slave device on the I²C bus at 100kHz or 400kHz using the address defined in the Serial interface control register (0006h), as modified by the S_A0 & S_A1 input pin settings. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

Figure 5: I²C Slave Read and Write Cycle Sequencing



The8T49N234 will not support the following functions:

- I²C general call
- Slave clock stretching
- I²C start byte protocol
- CBUS compatibility

Register Descriptions

Table 4: Register Blocks

Register Ranges Offset (Hex)	Register Block Description
0000 – 0001	Startup Control Registers
0002 – 0005	Device ID Control Registers
0006 – 0007	Serial Interface Control Registers
0008 – 002F	Digital PLL Control Registers
0030 – 0038	GPIO Control Registers
0039 – 003E	Output Driver Control Registers
003F – 004A	Output Divider Control Registers (Integer Portion)
004B – 0056	Reserved
0057 – 0062	Output Divider Control Registers (Fractional Portion)
0063 – 0067	Output Divider Source Control Registers
0068 – 006B	Analog PLL Control Registers
006C – 0070	Power-Down & Lock Alarm Control Registers
0071 – 0078	Input Monitor Control Registers
0079	Interrupt Enable Register
007A – 007B	Factory Setting Registers
007C – 01FF	Reserved
0200 – 0201	Interrupt Status Registers
0202 – 020B	Reserved
020C	General-Purpose Input Status Register
020D – 0212	Global Interrupt and Boot Status Register
0213 – 03FF	Reserved

Table 5: Device ID Control Register Bit Field Locations and Descriptions

Device ID Register Control Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0002	REV_ID[3:0]				DEV_ID[15:12]			
0003	DEV_ID[11:4]							
0004	DEV_ID[3:0]				DASH_CODE [10:7]			
0005	DASH_CODE [6:0]							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
REV_ID[3:0]	R/W	0h	Device revision.
DEV_ID[15:0]	R/W	0606h	Device ID code.
DASH CODE [10:0]	R/W	0b	Device dash code. Decimal value assigned by IDT to identify the configuration loaded at the factory. May be over-written by users at any time.

Table 6: Serial Interface Control Register Bit Field Locations and Descriptions

Serial Interface Control Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0006	0	UFTADD[6:2]					UFTADD[1]	UFTADD[0]
0007	Rsvd							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
UFTADD[6:2]	R/W	11011b	Configurable portion of I^2C base (bits 6:2) address for this device.
UFTADD[1]	R/O	0b	I^2C base address bit 1. This address bit reflects the status of the S_A1 external input pin. See Table 1.
UFTADD[0]	R/O	0b	I^2C base address bit 0. This address bit reflects the status of the S_A0 external input pin. See Table 1.
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7: Digital PLL Input Control Register Bit Field Locations and Descriptions

Digital PLL Input Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0008	REFSEL[2:0]			1	0	1	1	1
0009	Rsvd							Rsvd
000A	Rsvd		1	Rsvd	Rsvd	Rsvd	STATE[1:0]	
000B	Rsvd			PRE0[20:16]				
000C	PRE0[15:8]							
000D	PRE0[7:0]							
000E	Rsvd			PRE1[20:16]				
000F	PRE1[15:8]							
0010	PRE1[7:0]							

Digital PLL Input Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
REFSEL[2:0]	R/W	000b	Input reference selection for digital PLL: 000 = automatic selection 001 through 111 = Reserved, do not use
STATE[1:0]	R/W	00b	Digital PLL state machine control: 00 = run automatically 01 = force FREERUN state – set this if in Synthesizer mode 10 = force NORMAL state 11 = Reserved
PRE0[20:0]	R/W	00002Fh	Pre-divider ratio for input reference 0 (CLK) when used by digital PLL.
PRE1[20:0]	R/W	00002Fh	Pre-divider ratio for input reference 1 (FBIN) when used by digital PLL.
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 8: Digital PLL Feedback Control Register Bit Field Locations and Descriptions

Digital PLL Feedback Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0011	M1_0[23:16]							
0012	M1_0[15:8]							
0013	M1_0[7:0]							
0014	M1_1[23:16]							
0015	M1_1[15:8]							
0016	M1_1[7:0]							
0017	LCKBW[3:0]				ACQBW[3:0]			
0018	LCKDAMP[2:0]			ACQDAMP[2:0]			PLLGAIN[1:0]	
0019	Rsvd			Rsvd	Rsvd			Rsvd
001A	Rsvd							
001B	Rsvd							
001C	Rsvd							Rsvd
001D	Rsvd							
001E	Rsvd							
001F	FFh							
0020	FFh							
0021	FFh							
0022	FFh							
0023	Rsvd		Rsvd	Rsvd		Rsvd	Rsvd	FASTLCK
0024	LOCK[7:0]							
0025	Rsvd							DSM_INT[8]
0026	DSM_INT[7:0]							
0027	Rsvd							
0028	Rsvd			DSMFRAC[20:16]				
0029	DSMFRAC[15:8]							
002A	DSMFRAC[7:0]							
002B	Rsvd							
002C	01h							
002D	Rsvd							
002E	Rsvd							
002F	DSM_ORD[1:0]		DCXOGAIN[1:0]		Rsvd	DITHGAIN[2:0]		

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
M1_0[23:0]	R/W	00002Fh	M1 feedback divider ratio for input reference 0 (CLK) when used by digital PLL.
M1_1[23:0]	R/W	00002Fh	M1 feedback divider ratio for input reference 1 (FBIN) when used by digital PLL.
LCKBW[3:0]	R/W	0111b	Digital PLL loop bandwidth while locked: 0000 = 0.2Hz 0001 = 0.4Hz 0010 = 0.8Hz 0011 = 1.6Hz 0100 = 3.2Hz 0101 = 6.4Hz 0110 = 12Hz 0111 = 25Hz 1000 = 50Hz 1001 = 100Hz 1010 = 200Hz 1011 = 400Hz 1100 = 800Hz 1101 = 1.6kHz 1110 = 6.4kHz 1111 = Reserved
ACQBW[3:0]	R/W	0111b	Digital PLL loop bandwidth while in acquisition (not-locked): 0000 = 0.2Hz 0001 = 0.4Hz 0010 = 0.8Hz 0011 = 1.6Hz 0100 = 3.2Hz 0101 = 6.4Hz 0110 = 12Hz 0111 = 25Hz 1000 = 50Hz 1001 = 100Hz 1010 = 200Hz 1011 = 400Hz 1100 = 800Hz 1101 = 1.6kHz 1110 = 6.4kHz 1111 = Reserved

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
LCKDAMP[2:0]	R/W	011b	Damping factor for digital PLL while locked: 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved
ACQDAMP[2:0]	R/W	011b	Damping factor for digital PLL while in acquisition (not locked): 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved
PLLGAIN[1:0]	R/W	01b	Digital loop filter gain settings for digital PLL: 00 = 0.5 01 = 1 10 = 1.5 11 = 2
FASTLCK	R/W	1b	Enables fast lock operation for digital PLL: 0 = normal locking using LCKBW & LCKDAMP fields in all cases 1 = fast lock mode using ACQBW & ACQDAMP when not phase locked and LCKBW & LCKDAMP once phase locked
LOCK[7:0]	R/W	3Fh	Lock window size for digital PLL. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0.
DSM_INT[8:0]	R/W	02Ch	Integer portion of the Delta-Sigma modulator value.
DSMFRAC[20:0]	R/W	181949h	Fractional portion of Delta-Sigma modulator value. Divide this number by 2^{21} to determine the actual fraction.

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
DSM_ORD[1:0]	R/W	11b	Delta-Sigma modulator order for digital PLL: 00 = Delta-Sigma modulator disabled 01 = 1st order modulation 10 = 2nd order modulation 11 = 3rd order modulation
DCXOGAIN[1:0]	R/W	01b	Multiplier applied to instantaneous frequency error before it is applied to the digitally controlled oscillator in digital PLL: 00 = 0.5 01 = 1 10 = 2 11 = 4
DITHGAIN[2:0]	R/W	000b	Dither gain setting for digital PLL: 000 = no dither 001 = Least Significant Bit (LSB) only 010 = 2 LSBs 011 = 4 LSBs 100 = 8 LSBs 101 = 16 LSBs 110 = 32 LSBs 111 = 64 LSBs
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 9: GPIO Control Register Bit Field Locations and Descriptions

The values observed on any GPIO pins that are used as general purpose inputs are visible in the GPI[3:0] register that is located at location 0x020C near a number of other read-only registers.

GPIO Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0030	Rsvd				GPIO_DIR[3:0]			
0031	Rsvd				GPI3SEL[2]	GPI2SEL[2]	GPI1SEL[2]	GPI0SEL[2]
0032	Rsvd				GPI3SEL[1]	GPI2SEL[1]	GPI1SEL[1]	GPI0SEL[1]
0033	Rsvd				GPI3SEL[0]	GPI2SEL[0]	GPI1SEL[0]	GPI0SEL[0]
0034	Rsvd				GPO3SEL[2]	GPO2SEL[2]	GPO1SEL[2]	GPO0SEL[2]
0035	Rsvd				GPO3SEL[1]	GPO2SEL[1]	GPO1SEL[1]	GPO0SEL[1]
0036	Rsvd				GPO3SEL[0]	GPO2SEL[0]	GPO1SEL[0]	GPO0SEL[0]
0037	Rsvd							
0038	Rsvd				GPO[3:0]			

GPIO Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
GPIO_DIR[3:0]	R/W	0100b	Direction control for general-purpose I/O pins GPIO[3:0]: 0 = input mode 1 = output mode
GPI0SEL[2:0]	R/W	001b	Function of GPIO[0] pin when set to input mode by GPIO_DIR[0] register bit: 000 = general purpose input (value on GPIO[0] pin directly reflected in GPI[0] register bit) 001 = output enable control bit 0: OSEL[0], (Refer to Figure 4 for more details.) 010 = Reserved 011 = Reserved 100 through 111 = Reserved
GPI1SEL[2:0]	R/W	001b	Function of GPIO[1] pin when set to input mode by GPIO_DIR[1] register bit: 000 = general purpose input (value on GPIO[1] pin directly reflected in GPI[1] register bit) 001 = output enable control bit 1: OSEL[1], (Refer to Figure 4 for more details.) 010 through 111 = reserved
GPI2SEL[2:0]	R/W	000b	Function of GPIO[2] pin when set to input mode by GPIO_DIR[2] register bit: 000 = general purpose Input (value on GPIO[2] pin directly reflected in GPI[2] register bit) 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 through 111 = Reserved

GPIO Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
GPI3SEL[2:0]	R/W	000b	Function of GPIO[3] pin when set to input mode by GPIO_DIR[3] register bit: 000 = general purpose input (value on GPIO[3] pin directly reflected in GPI[3] register bit) 001 = Reserved 010 = Reserved 011 = Reserved 100 through 111 = Reserved
GPO0SEL[2:0]	R/W	000b	Function of GPIO[0] pin when set to output mode by GPIO_DIR[0] register bit: 000 = general purpose output (value in GPO[0] register bit driven on GPIO[0] pin 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 through 111 = Reserved
GPO1SEL[2:0]	R/W	000b	Function of GPIO[1] pin when set to output mode by GPIO_DIR[1] register bit: 000 = general purpose output (value in GPO[1] register bit driven on GPIO[1] pin 001 = Loss-of-Signal status flag for input reference 1 (FBIN) reflected on GPIO[1] pin 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

GPIO Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
GPO2SEL[2:0]	R/W	001b	Function of GPIO[2] pin when set to output mode by GPIO_DIR[2] register bit: 000 = general purpose output (value in GPO[2] register bit driven on GPIO[2] pin 001 = Loss-of-Signal status flag for input reference 0 (CLK) reflected on GPIO[2] pin 010 = Reserved 011 = Reserved 100 = Reserved 101 through 111 = Reserved
GPO3SEL[2:0]	R/W	000b	Function of GPIO[3] pin when set to output mode by GPIO_DIR[3] register bit: 000 = general purpose output (value in GPO[3] register bit driven on GPIO[3] pin 001 = Loss-of-Lock status flag for digital PLL reflected on GPIO[3] pin 010 = Reserved 011 = Reserved 100 through 111 = Reserved
GPO[3:0]	R/W	0000b	Output values reflect on pin GPIO[3:0] when general purpose output mode selected.
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 10: Output Driver Control Register Bit Field Locations and Descriptions

Output Driver Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0039	Rsvd				Rsvd	1	OUTEN[1:0]	
003A	Rsvd				Rsvd		POL_Q[1:0]	
003B	Rsvd							
003C	Rsvd							
003D	Rsvd		1	Rsvd	Rsvd	Rsvd	1	Rsvd
003E	OUTMODE1[2:0]			SE_MODE1	OUTMODE0[2:0]			SE_MODE0

Output Driver Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
OUTEN[1:0]	R/W	11b	Output enable control for clock outputs Q[1:0], nQ[1:0]: 0 = Qn is in a high-impedance state 1 = Qn is enabled as indicated in appropriate OUTMODEn[2:0] register field
POL_Q[1:0]	R/W	00b	Polarity of clock outputs Q[1:0], nQ[1:0]: 0 = Qn is normal polarity 1 = Qn is inverted polarity
OUTMODE0[2:0]	R/W	001b	Output driver mode of operation for clock outputs Q[1:0], nQ[1:0]: 000 = High-impedance 001 = LVPECL 010 = LVDS 011 = LVCMOS 100 = HCSL 101 – 111 = Reserved
OUTMODE1[2:0]	R/W	011b	
SE_MODE0	R/W	0b	Behavior of output pair Qm, nQm when LVCMOS operation is selected: (Must be 0 if LVDS or LVPECL output style is selected) 0 = Qm and nQm are both the same frequency but inverted in phase 1 = Qm and nQm are both the same frequency and phase
SE_MODE1	R/W	1b	
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 11: Output Divider Control Register (Integer Portion) Bit Field Locations and Descriptions

Output Divider Control Register (Integer Portion) Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
003F	Rsvd						NS1_Q0[1:0]	
0040	NS2_Q0[15:8]							
0041	NS2_Q0[7:0]							
0042	Rsvd						N_Q1[17:16]	
0043	N_Q1[15:8]							
0044	N_Q1[7:0]							
0045	Rsvd						N_FCLK[17:16]	
0046	N_FCLK[15:8]							
0047	N_FCLK[7:0]							
0048	Rsvd							
0049	Rsvd							
004A	Rsvd							

Output Divider Control Register (Integer Portion) Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
NS1_Q0[1:0]	R/W	00b	1st stage output divider ratio for output clock Q0, nQ0: 00 = /5 01 = /6 10 = /4 11 = Reserved
NS2_Q0[15:0]	R/W	001Dh	2nd stage output divider ratio for output clock Q0, nQ0. Actual divider ratio is 2x the value written here. A value of 0 in this register will bypass the second stage of the divider.
N_Q1[17:0]	R/W	00122h	Integer portion of output divider ratio for output clock Q1, nQ1: Values of 0, 1 or 2 cannot be written to this register. Actual divider ratio is 2x the value written here.
N_FCLK[17:0]	R/W	00122h	Integer portion of output divider ratio for output clock FCLK, nFCLK: Values of 0, 1 or 2 cannot be written to this register. Actual divider ratio is 2x the value written here.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 12: Output Divider Control Register (Fractional Portion) Bit Field Locations and Descriptions

Output Divider Control Register (Fractional Portion) Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0057	Rsvd				NFRAC_Q1[27:24]			
0058	NFRAC_Q1[23:16]							
0059	NFRAC_Q1[15:8]							
005A	NFRAC_Q1[7:0]							
005B	Rsvd				NFRAC_FCLK[27:24]			
005C	NFRAC_FCLK[23:16]							
005D	NFRAC_FCLK[15:8]							
005E	NFRAC_FCLK[7:0]							
005F	Rsvd							
0060	Rsvd							
0061	Rsvd							
0062	Rsvd							

Output Divider Control Register (Fractional Portion) Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
NFRAC_Q1[27:0]	R/W	0000000h	Fractional portion of output divider ratio for output Q1, nQ1. Actual fractional portion is 2x the value written here. Fraction = (NFRAC_Q1 * 2) * 2^{-28}
NFRAC_FCLK[27:0]	R/W	0000000h	Fractional portion of output divider ratio for output FCLK, nFCLK. Actual fractional portion is 2x the value written here. Fraction = (NFRAC_FCLK * 2) * 2^{-28}
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 13: Output Clock Source Control Register Bit Field Locations and Descriptions

Output Clock Source Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0063	PLL_SYN	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	CLK_SELFCLK[1:0]	
0064	Rsvd							
0065	Rsvd							
0066	Rsvd		Rsvd		Rsvd		Rsvd	
0067	Rsvd		Rsvd		Rsvd		Rsvd	

Output Clock Source Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
PLL_SYN	R/W	0b	Output synchronization control for outputs derived from PLL. Setting this bit from 0->1 will cause the output divider(s) for the affected outputs to be held in reset. Setting this bit from 1->0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0.
CLK_SELFCLK[1:0]	R/W	00b	Clock source selection for output pair FCLK, nFCLK: Do not select input reference 0 or 1 if that input is faster than 250MHz: 00 = PLL 01 = input reference 0 (CLK) 10 = input reference 1 (FBIN) 11 = crystal input
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Please contact IDT through one of the methods listed on the last page of this datasheet for details on how to set these fields for a particular user configuration.

Table 14: Analog PLL Control Register Bit Field Locations and Descriptions

Analog PLL Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0068	CPSET[2:0]			RS[1:0]		CP[1:0]		WPOST
0069	Rsvd		1	TDC_DIS	SYN_MODE	Rsvd	DLCNT	DBITM
006A	VCOMAN[2:0]			DBIT[4:0]				
006B	001b			Rsvd				

Analog PLL Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
CPSET[2:0]	R/W	111b	Charge pump current setting for analog PLL: 000 = 110µA 001 = 220µA 010 = 330µA 011 = 440µA 100 = 550µA 101 = 660µA 110 = 770µA 111 = 880µA
RS[1:0]	R/W	00b	Internal loop filter series resistor setting for analog PLL: 00 = 330Ω 01 = 640Ω 10 = 1.2kΩ 11 = 1.79kΩ
CP[1:0]	R/W	10b	Internal loop filter parallel capacitor setting for analog PLL: 00 = 40pF 01 = 80pF 10 = 140pF 11 = 200pF
WPOST	R/W	0b	Internal loop filter 2nd-pole setting for analog PLL: 0 = Rpost = 497Ω, Cpost = 40pF 1 = Rpost = 1.58kΩ, Cpost = 40pF
TDC_DIS	R/W	0b	TDC disable control for PLL: 0 = TDC enabled 1 = TDC disabled

Analog PLL Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
SYN_MODE	R/W	0b	Frequency synthesizer mode control for PLL: 0 = PLL jitter attenuates and translates one or more input references 1 = PLL synthesizes output frequencies using only the crystal as a reference Note that the STATE[1:0] field in the digital PLL control register must be set to force free-run state.
DLCNT	R/W	1b	Digital lock count setting for analog PLL: 0 = counter is a 20-bit accumulator 1 = counter is a 16-bit accumulator
DBITM	R/W	0b	Digital lock manual override setting for analog PLL: 0 = automatic mode 1 = manual mode
VCOMAN[2:0]	R/W	001b	Manual lock mode VCO selection setting for analog PLL: 000 = VCO0 001 = VCO1 010 – 111 = Reserved
DBIT[4:0]	R/W	01011b	Manual mode digital lock control setting for VCO in analog PLL.
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 15: Power Down Control Register Bit Field Locations and Descriptions

Power Down Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
006C	Rsvd						LCKMODE	DBL_DIS
006D	Rsvd						Rsvd	CLK_DIS
006E	Rsvd							
006F	Rsvd				1	Rsvd	Q1_DIS	Q0_DIS
0070	Rsvd					DPLL_DIS	DSM_DIS	CALRST

Power Down Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
LCKMODE	R/W	0b	Controls the behavior of the LOL alarm deassertion: 0 = LOL alarm deasserts once PLL is locked 1 = LOL alarm deasserts once PLL is locked and output clocks are stable
DBL_DIS	R/W	0b	Controls whether crystal input frequency is doubled before being used in PLL: 0 = 2x actual crystal frequency used 1 = actual crystal frequency used
CLK_DIS	R/W	0b	Disable control for differential clock input: 0 = input is enabled 1 = input is disabled
Qm_DIS	R/W	0b	Disable control for output Qm, nQm (m = 0, 1): 0 = output Qm, nQm functions normally 1 = All logic associated with Output Qm, nQm is disabled & driver in High-impedance state
DPLL_DIS	R/W	0b	Disable control for digital PLL: 0 = digital PLL enabled 1 = digital PLL disabled
DSM_DIS	R/W	0b	Disable control for Delta-sigma modulator for analog PLL: 0 = DSM enabled 1 = DSM disabled
CALRST	R/W	0b	Reset calibration Logic for analog PLL: 0 = calibration logic for analog PLL enabled 1 = calibration logic for analog PLL disabled
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 16: Input Monitor Control Register Bit Field Locations and Descriptions

Input Monitor Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0071	Rsvd							LOS_0[16]
0072	LOS_0[15:8]							
0073	LOS_0[7:0]							
0074	Rsvd							LOS_1[16]
0075	LOS_1[15:8]							
0076	LOS_1[7:0]							
0077	Rsvd							
0078	Rsvd							

Input Monitor Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
LOS_m[16:0]	R/W	0004Ch	Number of input monitoring clock periods before input reference m (m = 0 (CLK), 1 (FBIN)) is considered to be missed (soft alarm). Minimum setting is 3.
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 17: Interrupt Enable Control Register Bit Field Locations and Descriptions

Interrupt Enable Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0079	Rsvd	LOL_EN	Rsvd	Rsvd	Rsvd		LOS1_EN	LOS0_EN

Interrupt Enable Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
LOL_EN	R/W	0b	Interrupt enable control for Loss-of-Lock interrupt status bit: 0 = LOL_INT register bit will not affect status of nINT output signal 1 = LOL_INT register bit will affect status of nINT output signal
LOSm_EN	R/W	0b	Interrupt enable control for Loss-of-Signal interrupt status bit for input reference (m = 0 (CLK), 1 (FBIN)): 0 = LOSm_INT register bit will not affect status of nINT output signal 1 = LOSm_INT register bit will affect status of nINT output signal
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 18: Factory Setting Register Bit Field Locations

Factory Setting Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
007A	27h							
007B	Rsvd			Rsvd	Rsvd	Rsvd	Rsvd	Rsvd

This register contains “sticky” bits for tracking the status of the various alarms. Whenever an alarm occurs, the appropriate Interrupt Status bit will be set. The Interrupt Status bit will remain asserted even after the original alarm goes away. The Interrupt Status bits remain asserted until explicitly cleared by a write of a ‘1’ to the bit over the serial port. This type of functionality is referred to as Read / Write-1-to-Clear (R/W1C).

Table 19: Interrupt Status Register Bit Field Locations and Descriptions

Interrupt Status Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0200	Rsvd	LOL_INT	Rsvd	Rsvd	Rsvd		LOS1_INT	LOS0_INT
0201	Rsvd							

Interrupt Status Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
LOL_INT	R/W1C	0b	Interrupt status bit for Loss-of-Lock: 0 = no Loss-of-lock alarm flag on PLL has occurred since the last time this register bit was cleared 1 = at least one Loss-of-Lock alarm flag on PLL has occurred since the last time this register bit was cleared
LOSm_INT	R/W1C	0b	Interrupt status bit for Loss-of-Signal on input reference (m = 0 (CLK), 1 (FBIN)): 0 = no Loss-of-Signal alarm flag on input reference m has occurred since the last time this register bit was cleared 1 = at least one Loss-of-Signal alarm flag on input reference m has occurred since the last time this register bit was cleared
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 20: General Purpose Input Status Register Bit Field Locations and Descriptions

Global Interrupt Status Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
020C	Rsvd				GPI[3]	GPI[2]	GPI[1]	GPI[0]

General Purpose Input Status Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
GPI[3:0]	R/O	–	Shows current values on GPIO[3:0] pins that are configured as general purpose inputs.
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 21: Global Interrupt Status Register Bit Field Locations and Descriptions

Global Interrupt Status Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
020D	Rsvd		Rsvd		Rsvd			INT
020E	Rsvd				Rsvd			
020F	Rsvd			Rsvd				
0210	Rsvd					Rsvd	Rsvd	Rsvd
0211	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
0212	Rsvd							

Global Interrupt Status Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
INT	R/O	–	Device interrupt status: 0 = no interrupt status bits that are enabled are asserted (nINT pin released) 1 = at least one interrupt status bit that is enabled is asserted (nINT pin asserted low)
Rsvd	R/W	–	Reserved. Always write 0 to this bit location. Read values are not defined.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 22: Absolute Ratings

Item	Rating
Supply voltage, V_{CC}	3.63V
Inputs, V_I OSCI Other input	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, V_O (Q[1:0], nQ[1:0], FCLK, nFCLK)	-0.5V to V_{CCOX}[a] + 0.5V
Outputs, V_O (GPIO, SCLK, SDATA, nINT)	-0.5V to V_{CCCS} + 0.5V
Outputs, I_O (Q[1:0], nQ[1:0], FCLK, nFCLK) Continuous current Surge current	 40mA 65mA
Outputs, I_O (GPIO[3:0], SCLK, SDATA, nINT) Continuous current Surge current	 8mA 13mA
Junction temperature, T_J	125°C
Storage temperature, T_{STG}	-65°C to 150°C

a. V_{CCOX} denotes: V_{CCO0}, V_{CCO1}, V_{CCO2}.

Supply Voltage Characteristics

Table 23: Power Supply DC Characteristics, V_{CC} = 3.3V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core supply voltage		3.135	3.3	3.465	V
V_{CCA}	Analog supply voltage		3.135	3.3	V_{CC}	V
V_{CCCS}	Control and status supply voltage		1.71		V_{CC}	V
I_{CC}	Core supply current[a]			39	50	mA
I_{CCCS}	Control and status supply current[b]			3	6	mA
I_{CCA}	Analog supply current[a]			91	121	mA
I_{EE}	Power supply current[c]	Q[1:0], nQ[1:0] configured for LVPECL logic levels; outputs unloaded[d]		281	340	mA

a. I_{CC}, I_{CCA} and I_{CCCS} are included in I_{EE} when output clocks configured for LVPECL logic levels.

b. GPIO [3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST pins are floating.

c. Internal dynamic switching current at maximum f_{OUT} is included.

d. Outputs enabled.

Table 24: Power Supply DC Characteristics, V_{CC} = 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core supply voltage		2.375	2.5	2.625	V
V_{CCA}	Analog supply voltage		2.375	2.5	V_{CC}	V
V_{CCCS}	Control and status supply voltage		1.71		V_{CC}	V
I_{CC}	Core supply current[a]			39	50	mA
I_{CCCS}	Control and status supply current[b]			3	5	mA
I_{CCA}	Analog supply current[a]			87	118	mA
I_{EE}	Power supply current[c]	Q[1:0], nQ[1:0] configured for LVPECL logic levels; outputs unloaded[d]		264	325	mA

a. I_{CC}, I_{CCA} and I_{CCCS} are included in I_{EE} when output clocks configured for LVPECL logic levels.

b. GPIO [3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST pins are floating.

c. Internal dynamic switching current at maximum f_{OUT} is included.

d. Outputs enabled.

Table 25: Maximum Output Supply Current, V_{CC} = V_{CCCS} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[a] = 3.3V ±5%				V_{CCOx}[a] = 2.5V ±5%				V_{CCOx}[a] = 1.8V±5%	Units
			LVPECL	LVDS	HCSL	LVCMOS	LVPECL	LVDS	HCSL	LVCMOS	LVCMOS	
I_{CCO0}[b]	Q0, nQ0 Output supply current	Outputs unloaded[c]	41	50	41	44	35	42	36	35	30	mA
I_{CCO1}[b]	Q1, nQ1 Output supply current	Outputs unloaded[c]	55	64	55	55	48	57	47	52	43	mA
I_{CCO2}[b]	FCLK, nFCLK Output supply current	Outputs unloaded[c]	56	N/A	N/A	N/A	49	N/A	N/A	N/A	N/A	mA

a. V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}.

b. Internal dynamic switching current at maximum f_{OUT} is included.

c. Outputs enabled.

DC Electrical Characteristics

Table 26: DC Input/ Output Characteristics, V_{CC} = V_{CCOX} = 3.3V±5% or 2.5V±5%

Symbol	Parameter		Test Conditions[a]	Minimum	Typical	Maximum	Units
C_{IN}	Input capacitance[b]				3.5		pF
R_{PULLUP}	Input pull-up resistor	GPIO[3:0], nRST, nWP, SDATA, SCLK			51		kΩ
$R_{PULLDOWN}$	Input pull-down resistor	S_A0, S_A1			51		kΩ
C_{PD}	Power dissipation capacitance (per output pair)	LVCMOS Q0	V_{CCOX} = 3.465V		11.5		pF
		LVCMOS Q1	V_{CCOX} = 3.465V		13		pF
		LVCMOS Q0	V_{CCOX} = 2.625V		10.5		pF
		LVCMOS Q1	V_{CCOX} = 2.625V		16		pF
		LVCMOS Q0	V_{CCOX} = 1.89V		11		pF
		LVCMOS Q1	V_{CCOX} = 1.89V		13		pF
		LVDS, HCSL or LVPECL Q0	V_{CCOX} = 3.465V or 2.625V		2.5		pF
		LVDS, HCSL or LVPECL Q1, FCLK	V_{CCOX} = 3.465V or 2.625V		4.5		pF
R_{OUT}	Output impedance	GPIO[3:0]	V_{CCCS} = 3.3V		26		Ω
			V_{CCCS} = 2.5V		30		
			V_{CCCS} = 1.8V		42		
		LVCMOS Q[1:0], nQ[1:0]	V_{CCOX} = 3.3V		18		Ω
			V_{CCOX} = 2.5V		22		
			V_{CCOX} = 1.8V		30		

a. V_{CCOX} denotes: V_{CCO0}, V_{CCO1}, V_{CCO2}.

b. This specification does not apply to the OSCI or OSCO pins.

Table 27: LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input high voltage	nWP, nRST, GPIO[3:0], SDATA, SCLK, S_A1, S_A0	V_{CCCS} = 3.3V	2.1		V_{CCCS} +0.3	V
			V_{CCCS} = 2.5V	1.7		V_{CCCS} +0.3	V
			V_{CCCS} = 1.8V	1.4		V_{CCCS} +0.3	V
V_{IL}	Input low voltage	nWP, nRST, GPIO[3:0], SDATA, SCLK, S_A1, S_A0	V_{CCCS} = 3.3V	-0.3		0.8	V
			V_{CCCS} = 2.5V	-0.3		0.6	V
			V_{CCCS} = 1.8V	-0.3		0.4	V
I_{IH}	Input high current	S_A1, S_A0	$V_{CCCS} = V_{IN}$ = 3.465V, 2.625V, 1.89V			150	µA
		nRST, nWP, SDATA, SCLK	$V_{CCCS} = V_{IN}$ = 3.465V, 2.625V, 1.89V			5	µA
		GPIO[3:0]	$V_{CCCS} = V_{IN}$ = 3.465V, 2.625V, 1.89V			1	mA
I_{IL}	Input low current	S_A1, S_A0	V_{CCCS} = 3.465V, 2.625V, 1.89V, V_{IN} = 0V	-5			µA
		nRST, nWP, SDATA, SCLK	V_{CCCS} = 3.465V, 2.625V, 1.89V, V_{IN} = 0V	-150			µA
		GPIO[3:0]	V_{CCCS} = 3.465V, 2.625V, 1.89V, V_{IN} = 0V	-1			mA
V_{OH}	Output high voltage	SDATA,[a] SCLK,[a] nINT[a]	V_{CCCS} = 3.3V ±5%, I_{OH} = -5µA	2.6			V
		GPIO[3:0]	V_{CCCS} = 3.3V ±5%, I_{OH} = -50µA	2.6			V
		SDATA,[a] SCLK,[a] nINT[a]	V_{CCCS} = 2.5V ±5%, I_{OH} = -5µA	1.8			V
		GPIO[3:0]	V_{CCCS} = 2.5V ±5%, I_{OH} = -50µA	1.8			V
		SDATA,[a] SCLK,[a] nINT[a]	V_{CCCS} = 1.8V ±5%, I_{OH} = -5µA	1.3			V
		GPIO[3:0]	V_{CCCS} = 1.8V ±5%, I_{OH} = -50µA	1.3			V
V_{OL}	Output low voltage	SDATA,[a] SCLK,[a] nINT[a]	V_{CCCS} = 3.3V ±5%, 2.5V±5%, or 1.8V±5% I_{OL} = 5mA			0.5	V
		GPIO[3:0]	V_{CCCS} = 3.3V ±5%, 2.5V±5%, or 1.8V±5% I_{OL} = 5mA			0.5	V

a. Use of external pull-up resistors is recommended.

Table 28: Differential Input DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input high current	CLK, nCLK; FBIN, nFBIN	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input low current	CLK, FBIN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nCLK, nFBIN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-peak voltage[a]			0.15		1.3	V
V_{CMR}	Common mode input voltage[a, b]			V_{EE}		V_{CC} -1.2	V

a. V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.

b. Common mode voltage is defined as the cross-point.

Table 29: LVPECL DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[a] = 3.3V±5%			V_{CCOx}[a] = 2.5V±5%			Units
			Minimum	Typical	Maximum	Minimum	Typical	Maximum	
V_{OH}	Output high voltage[b]		V_{CCOX} - 1.3		V_{CCOX} - 0.8	V_{CCOX} - 1.4		V_{CCOX} - 0.9	V
V_{OL}	Output low voltage[b]		V_{CCOX} - 1.95		V_{CCOX} - 1.75	V_{CCOX} - 1.95		V_{CCOX} - 1.75	V

a. V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}.

b. Outputs terminated with 50Ω to V_{CCOx} – 2V.

Table 30: LVDS DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOX} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C[a, b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential output voltage		200		400	mV
ΔV_{OD}	V_{OD} magnitude change				50	mV
V_{OS}	Offset voltage		1.1		1.375	V
ΔV_{OS}	V_{OS} magnitude change				50	mV

a. V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}.

b. Terminated with 100Ω across Qx and nQx.

Table 31: LVCMOS DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[a] = 3.3V±5%			V_{CCOx}[a] = 2.5V±5%			V_{CCOx}[a] = 1.8V ±5%			Units
			Minimum	Typical	Maximum	Minimum	Typical	Maximum	Minimum	Typical	Maximum	
V_{OH}	Output high voltage	I_{OH} = -8mA	2.6			1.8			1.1			V
V_{OL}	Output low voltage	I_{OL} = 8mA			0.5			0.5			0.5	V

a. V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}.

Table 32: Input Frequency Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input frequency[a]	OSCI, OSCO	Using a crystal (See Table 33 for crystal characteristics)	10		50	MHz
			Over-driving crystal input doubler logic enabled[b]	10		62.5	MHz
			Over-driving crystal input doubler logic disabled[b]	10		125	MHz
		CLK, nCLK; FBIN, nFBIN		0.008		875	MHz
f_{PD}	Phase detector frequency[c]			0.008		8	MHz
f_{SCLK}	Serial port clock SCLK (slave mode)	I^2C operation		100		400	kHz

a. For the input reference frequency, the divider values must be set for the VCO to operate within its supported range.

b. For optimal noise performance, the use of a quartz crystal is recommended. Refer to Overdriving the XTAL Interface in the Applications Information section.

c. Pre-dividers must be used to divide the input reference frequency down to a f_{PD} valid frequency range.

Table 33: Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of oscillation			Fundamental		
Frequency		10		50	MHz
Equivalent Series Resistance (ESR)			15	30	Ω
Load capacitance (C_L)			12		pF
Frequency stability (total)		-100		100	ppm

AC Electrical Characteristics

Table 34: AC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[a], [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO operating frequency			3000		4000	MHz
f_{OUT}	Output frequency	LVPECL, LVDS, HCSL	Integer divide ratio	0.008		1000	MHz
			Q0, Q1, FCLK outputs Non-integer divide	0.008		400	MHz
		LVCMOS		0.008		250	MHz
t_R / t_F	Output rise and fall times	LVPECL	20% to 80%		320	520	ps
		LVDS	20% to 80%, V_{CCOx} = 3.3V		160	320	ps
			20% to 80%, V_{CCOx} = 2.5V		200	400	ps
		HCSL	20% to 80%		280	470	ps
		LVCMOS[c], [d]	20% to 80%, V_{CCOx} = 3.3V		240	310	ps
			20% to 80%, V_{CCOx} = 2.5V		260	330	ps
			20% to 80%, V_{CCOx} = 1.8V		350	550	ps
SR	Output slew rate	LVPECL	Differential waveform, measured ±150mV from center	1		5	V/ns
		LVDS	Differential waveform, measured ±150mV from center, V_{CCOx} = 2.5V	0.5		4	V/ns
			Differential waveform, measured ±150mV from center, V_{CCOx} = 3.3V	0.5		5	V/ns
		HCSL	Measured on differential waveform, ±150mV from center, V_{CCOx} = 2.5V, $f_{OUT} \leq$ 156.25MHz	1.5		5	V/ns
			Measured on differential waveform, ±150mV from center, V_{CCOx} = 3.3V, $f_{OUT} \leq$ 156.25MHz	2.5		6.5	V/ns
odc	Output duty cycle[e]	LVPECL, LVDS, HCSL	$f_{OUT} \leq$ 666.667MHz	45	50	55	%
		LVPECL, LVDS, HCSL	f_{OUT} > 666.667MHz	40	50	60	%
		LVCMOS		40	50	60	%

Table 34: AC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[a], [b] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
SPO	Static phase offset[f]		Default configuration, V_{CC} = V_{CCOx} = 3.3V or 2.5V		480		ps
ΔSPO	Static phase offset variation[f]		Default configuration, V_{CC} = V_{CCOx} = 3.3V or 2.5V	-200		200	ps
	Spurious limit at offset [f]	≥800kHz	Default configuration		-67		dBc
$t_{startup}$	Startup time[g]	Internal OTP startup	From V_{CC} >80% to First output clock edge		110	150	ms

a. V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}.

b. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

c. Appropriate SE_MODE bit must be configured to select phase-aligned or phase-inverted operation.

d. All Q and nQ outputs in phase-inverted operation.

e. Characterized in PLL mode. Duty cycle of bypassed signals (input reference clocks or crystal input) is not adjusted by the device.

f. Characterized with default configuration.

g. This parameter is guaranteed by design.

Table 35: HCSL AC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to 85°C[a], [b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{RB}	Ring-back voltage margin[c], [d]		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed[c], [d]		500			ps
V_{MAX}	Absolute max. output voltage[e], [f]				1150	mV
V_{MIN}	Absolute min. output voltage[e], [g]		-300			mV
V_{CROSS}	Absolute crossing voltage[h], [i]		200		500	mV
ΔV_{CROSS}	Total variation of V_{CROSS} over all edges[h], [j]				140	mV

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}.

c. Measurement taken from differential waveform.

d. T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.

e. Measurement taken from single ended waveform.

f. Defined as the maximum instantaneous voltage including overshoot.

g. Defined as the minimum instantaneous voltage including undershoot.

h. Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

i. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

j. Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in V_{CROSS} for any particular system.

Table 36: Typical RMS Phase Jitter, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[a]

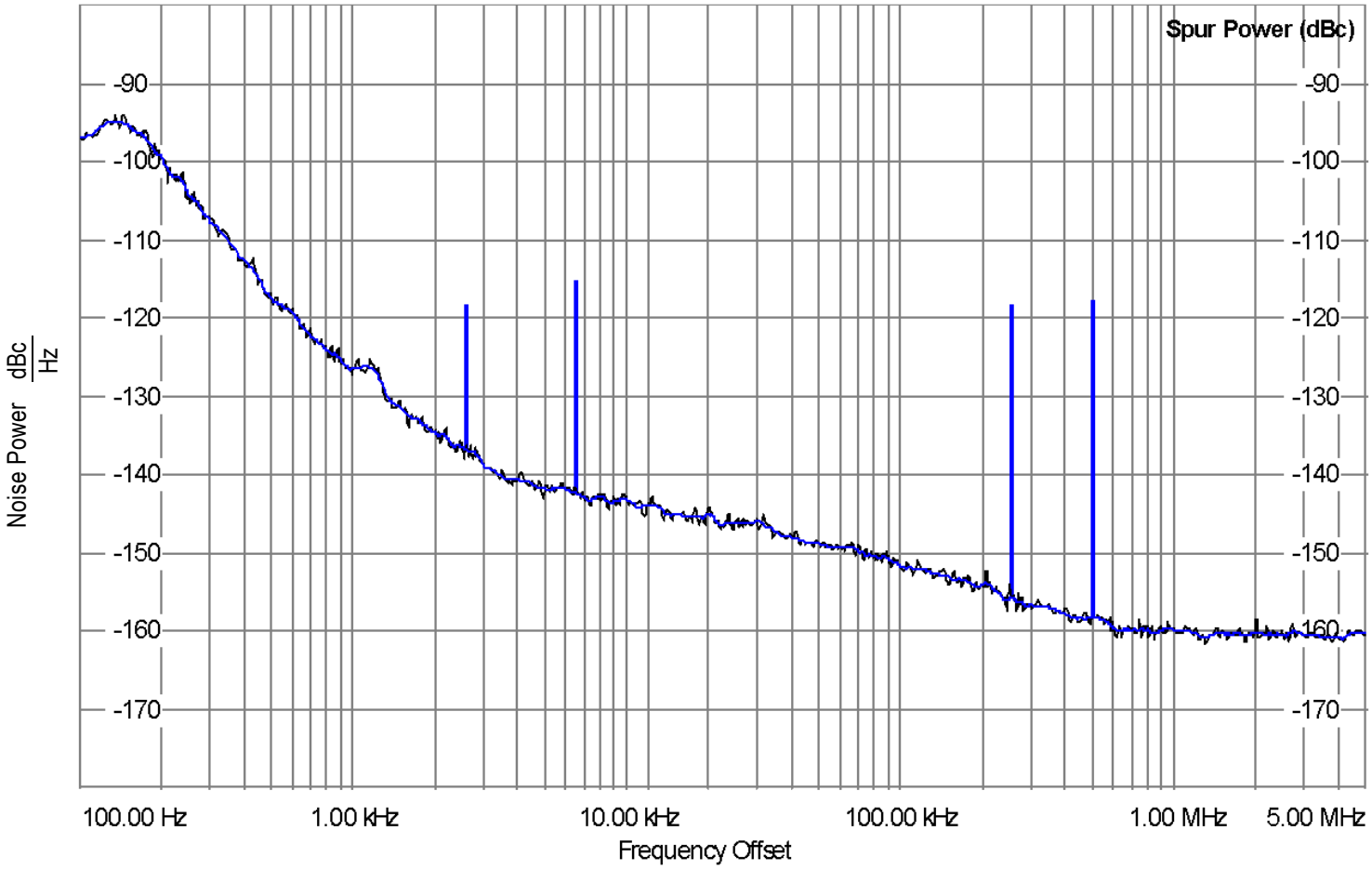
Symbol	Parameter		Test Conditions	Typical	Units
tjit(φ)	RMS phase jitter[b] (random)	Q0	Default Configuration, f_{OUT} = 12MHz, Integration range: 12kHz – 5MHz	480	fs
		Q1	Default Configuration, f_{OUT} = 6MHz, Integration range: 12kHz – 500kHz	291	fs

a. V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}.

b. It is recommended to use IDT's *Timing Commander* software to program the device for optimal jitter performance.

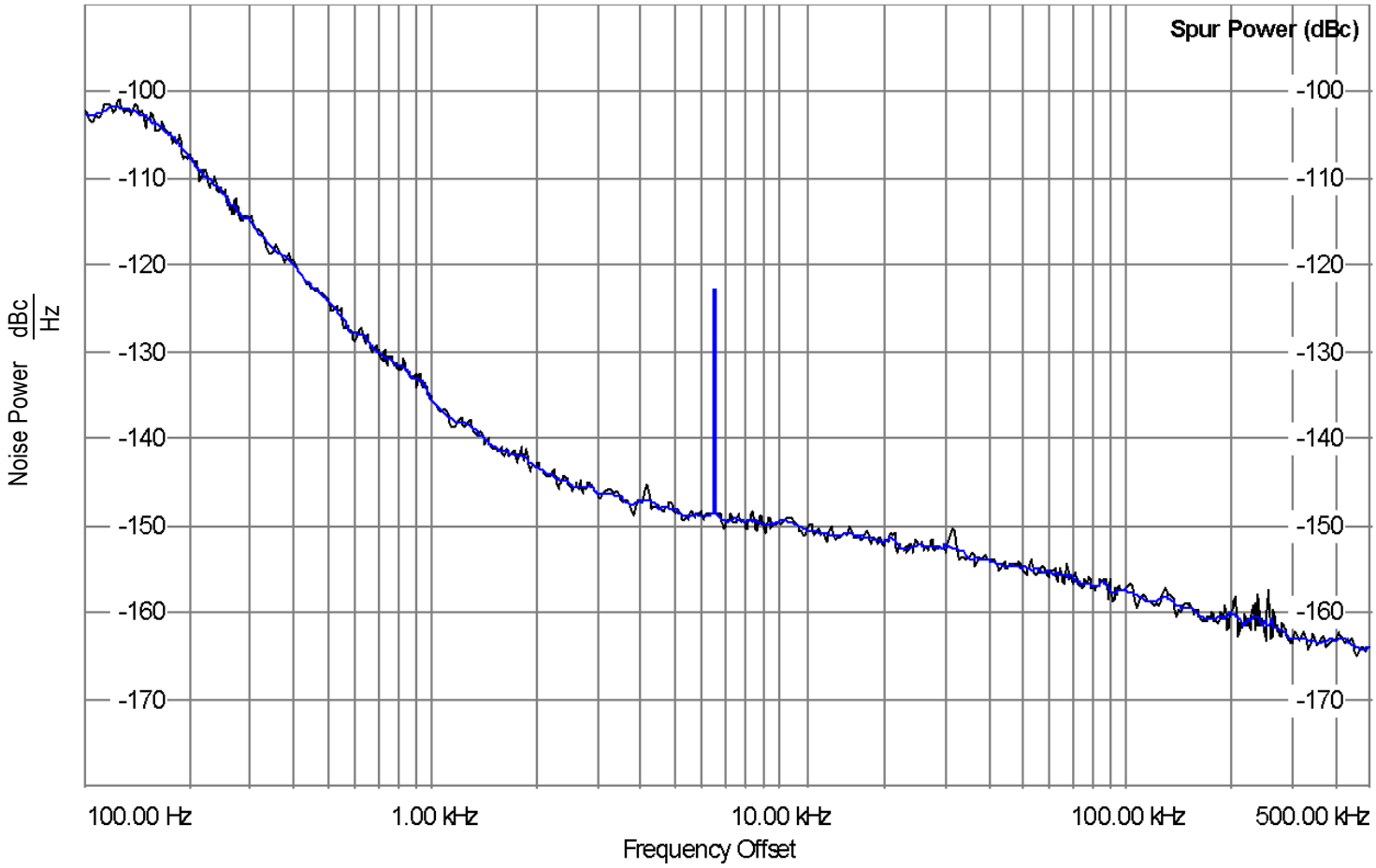
Typical Phase Noise (Q0, default configuration)

Figure 6: Typical Phase Noise Plot



Typical Phase Noise (Q1, default configuration)

Figure 7: Typical Phase Noise Plot



Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Input

For applications not requiring the use of one or more reference clock inputs, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground. It is recommended that CLK, nCLK not be driven with active signals when not selected.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both OSCI and OSCO can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from OSCI to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

Any unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

Any unused LVDS output pair can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

LVCMOS Outputs

Any LVCMOS output can be left floating if unused. There should be no trace attached.

HCSL Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 8* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 9* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSCI input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

Figure 8: General Diagram for LVCMOS Driver to XTAL Input Interface

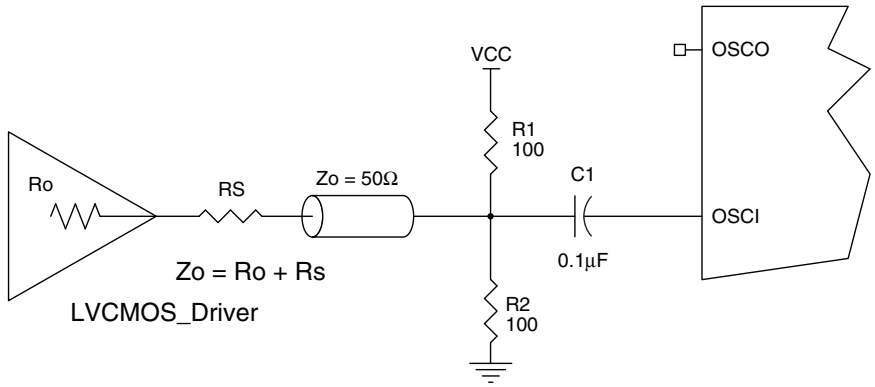
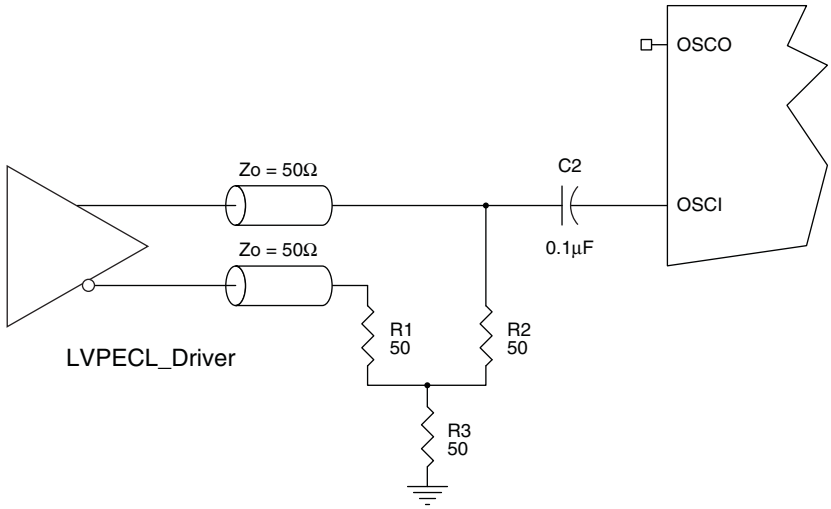


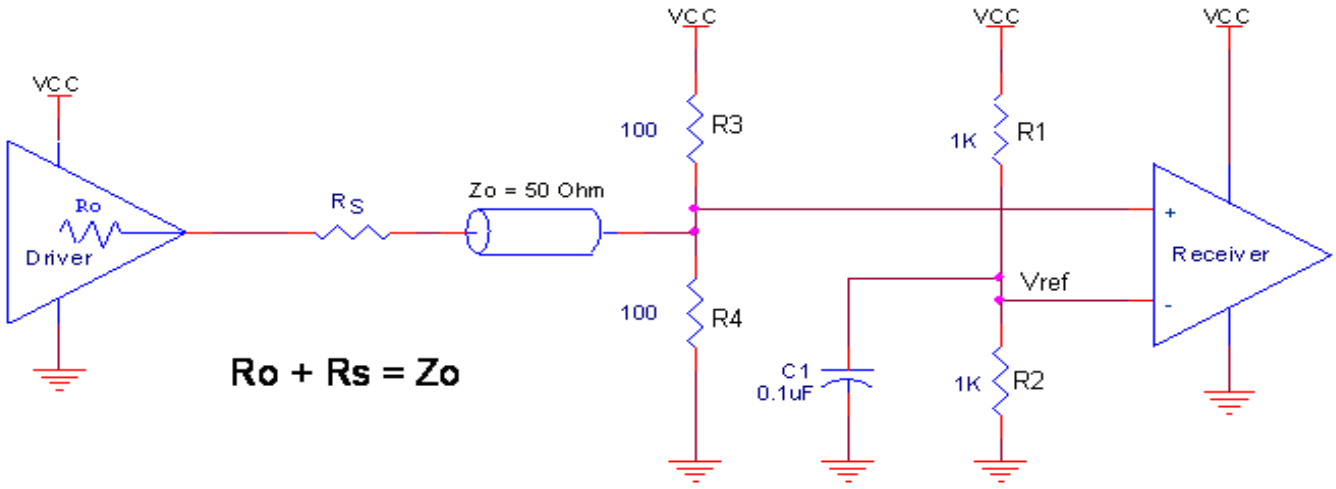
Figure 9: General Diagram for LVPECL Driver to XTAL Input Interface



Wiring the Differential Input to Accept Single-Ended Levels

Figure 10 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 10: Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



3.3V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 11* to *Figure 15* show interface examples for the CLK, nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 11*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 11: CLK/ nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

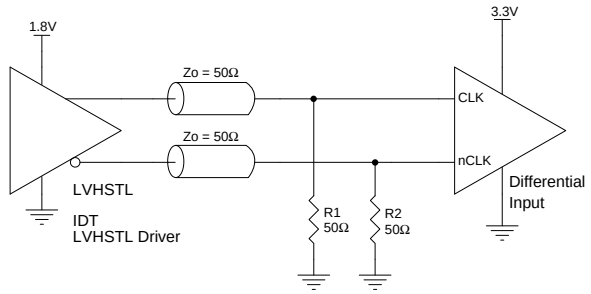


Figure 12: CLK/ nCLK Input Driven by a 3.3V LVPECL Driver

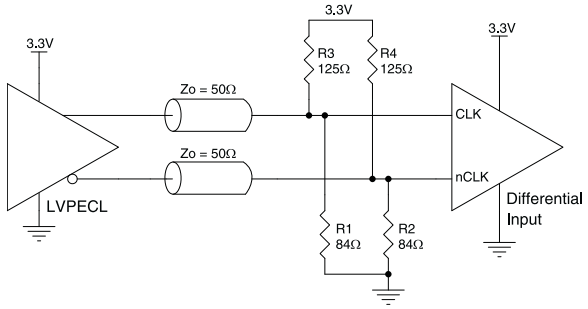


Figure 13: CLK/ nCLK Input Driven by a 3.3V HCSL Driver

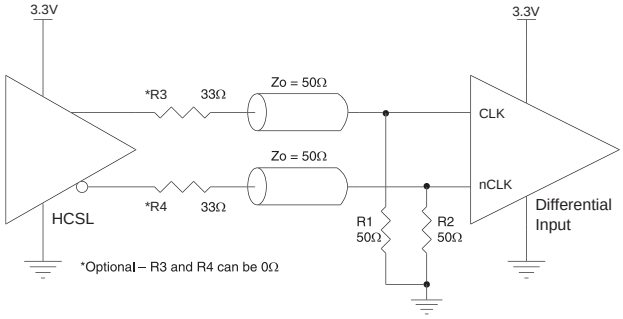


Figure 14: CLK/ nCLK Input Driven by a 3.3V LVPECL Driver

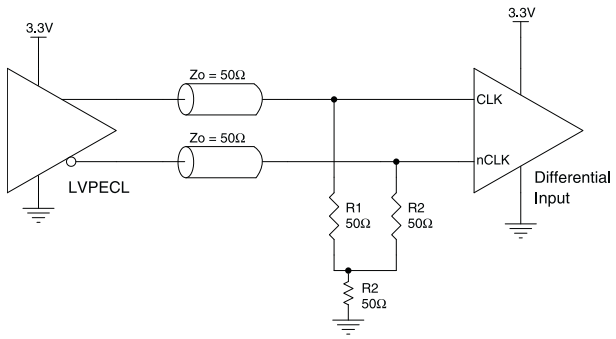
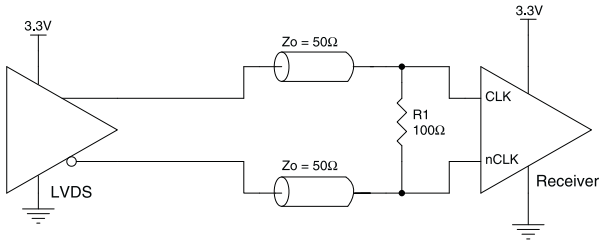


Figure 15: CLK/ nCLK Input Driven by a 3.3V LVDS Driver



2.5V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 16 to Figure 20* show interface examples for the CLK/nCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 16*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 16: CLK/ nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

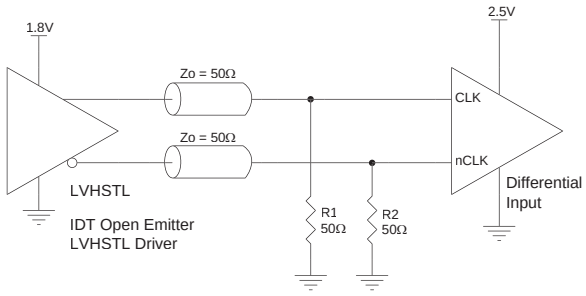


Figure 17: CLK/ nCLK Input Driven by a 2.5V LVPECL Driver

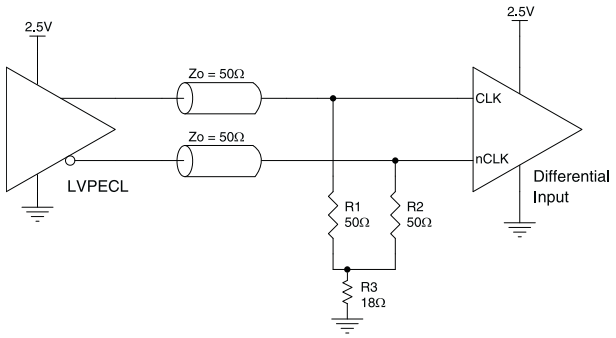


Figure 18: CLK/ nCLK Input Driven by a 2.5V HCSL Driver

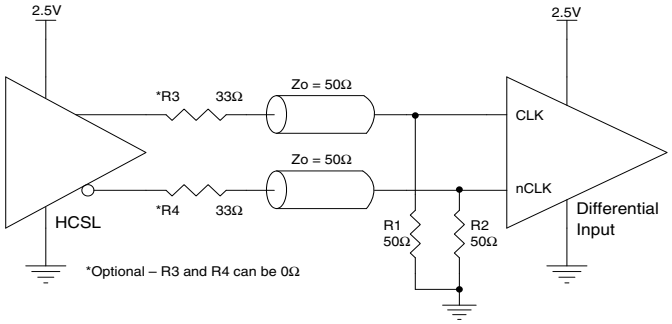


Figure 19: CLK/ nCLK Input Driven by a 2.5V LVPECL Driver

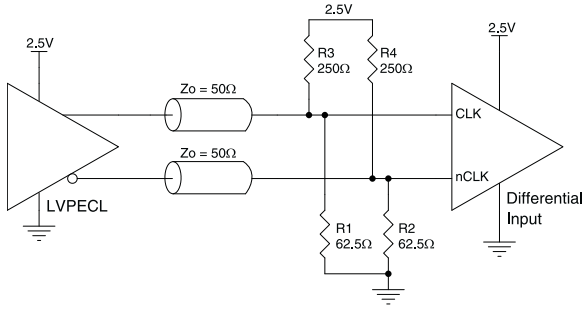
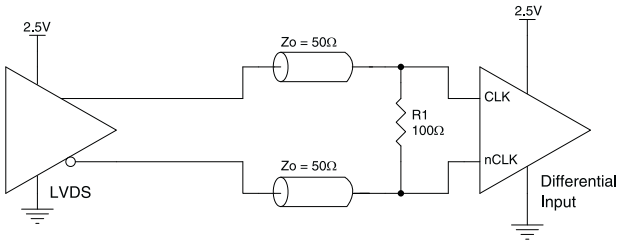


Figure 20: CLK/ nCLK Input Driven by a 2.5V LVDS Driver



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 21* can be used with either type of output structure. *Figure 22*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 21: Standard LVDS Termination

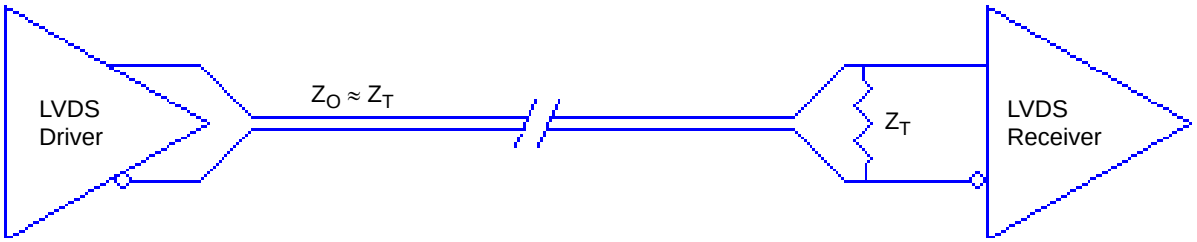
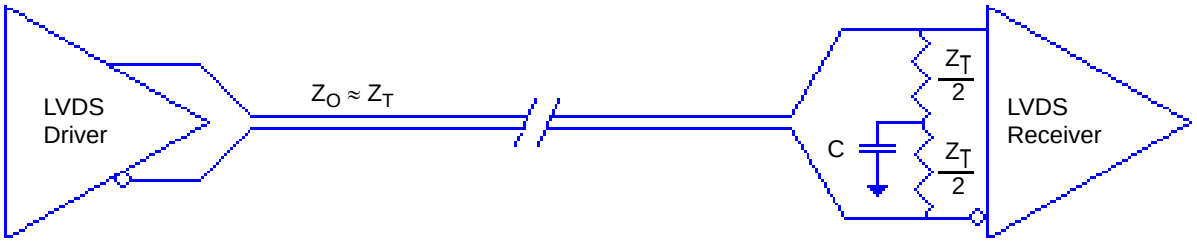


Figure 22: Optional LVDS Termination



Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 23 and Figure 24* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 23: 3.3V LVPECL Output Termination

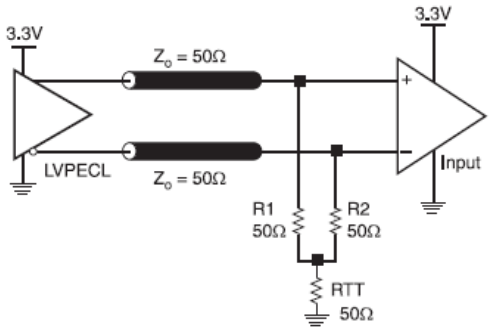
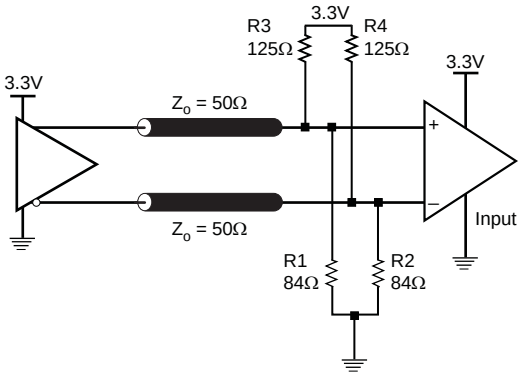


Figure 24: 3.3V LVPECL Output Termination



Termination for 2.5V LVPECL Outputs

Figure 25 and *Figure 27* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in *Figure 27* can be eliminated and the termination is shown in *Figure 26*.

Figure 25: 2.5V LVPECL Driver Termination Example

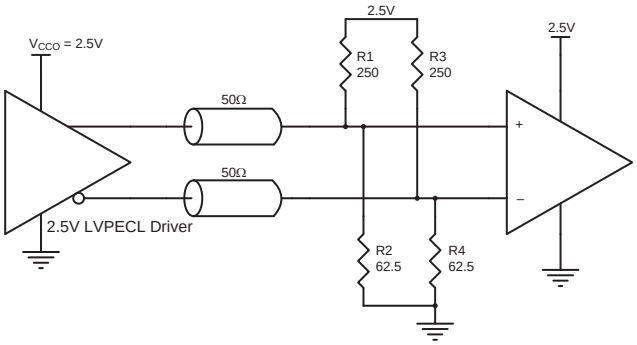


Figure 26: 2.5V LVPECL Driver Termination Example

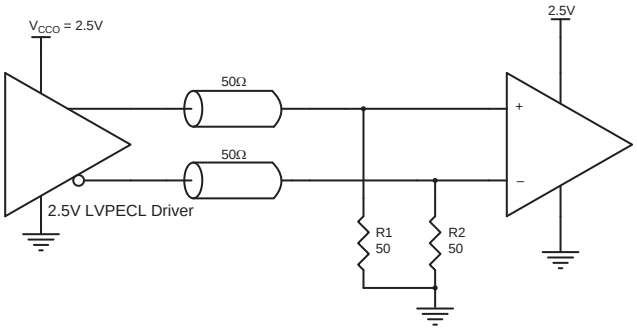
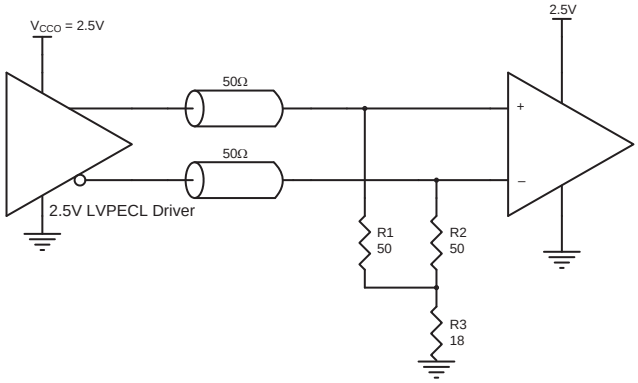


Figure 27: 2.5V LVPECL Driver Termination Example



HCSL Recommended Termination

Figure 28 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 28: Recommended Source Termination (where the driver and receiver will be on separate PCBs)

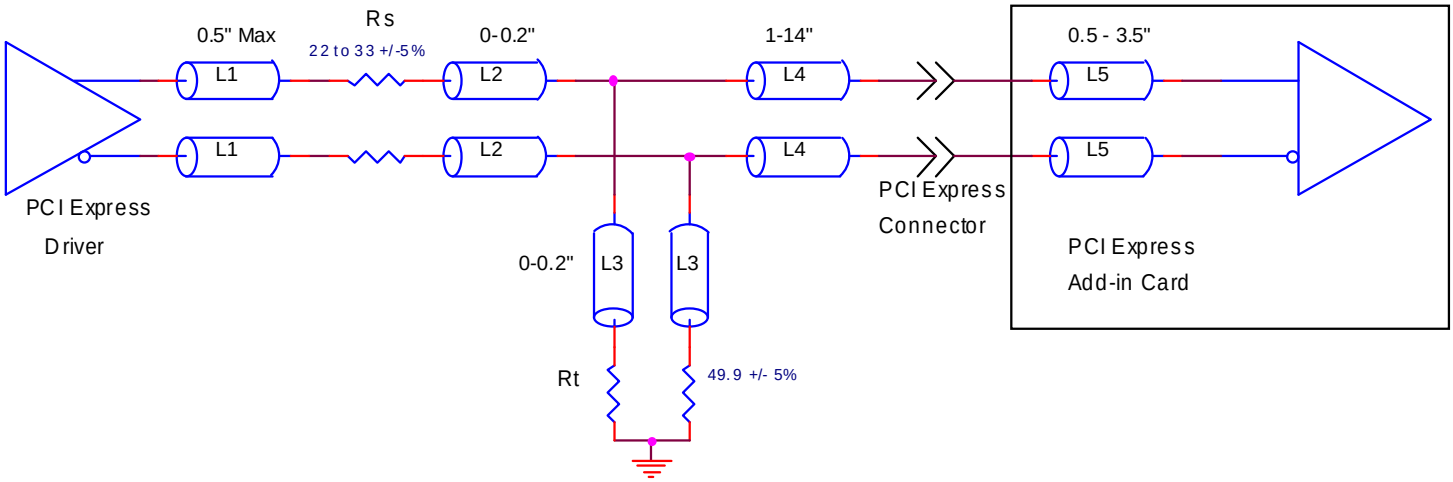
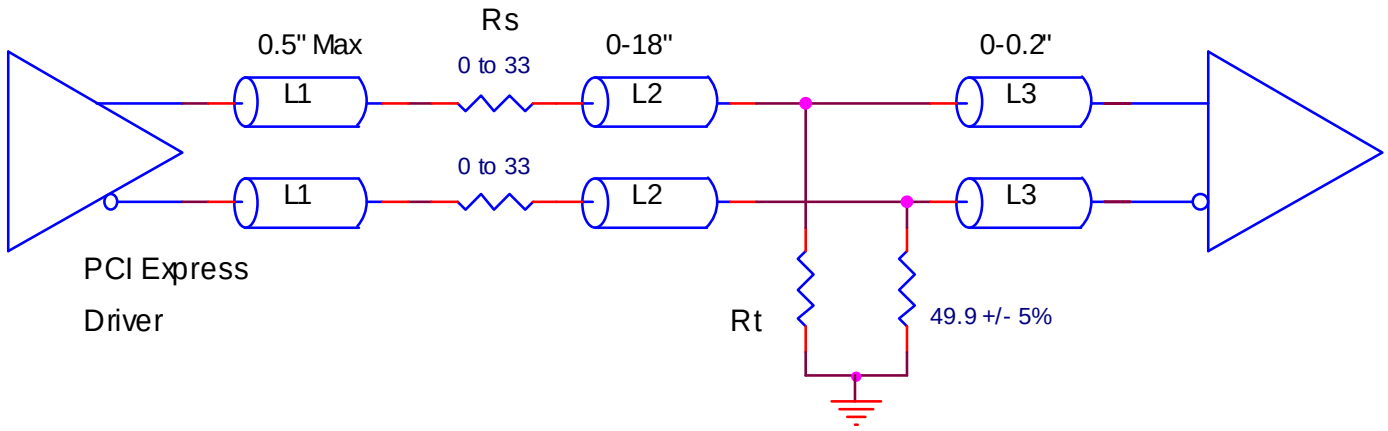


Figure 29 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 29: Recommended Termination (where a point-to-point connection can be used)

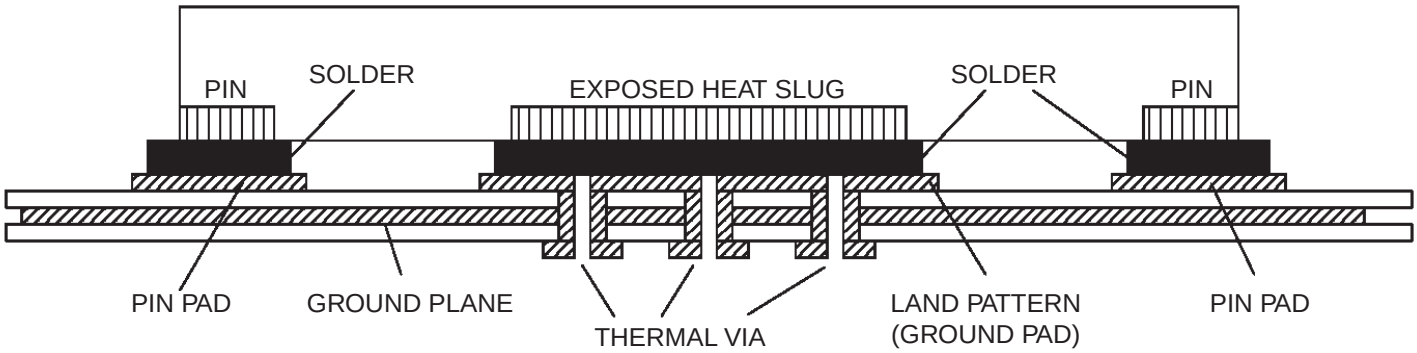


VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 30*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the *Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead-frame Base Package, Amkor Technology.*

Figure 30: P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



Schematic and Layout Information

Contact IDT for schematic and layout support.

Crystal Recommendation

This device was validated using FOX 277LF series through-hole crystals including Part # 277LF-40-18 (40MHz). If a surface mount crystal is desired, we recommend FOX Part #603-40-48 (40MHz).

Power Dissipation and Thermal Considerations

The 8T49N234 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as these features and functions are enabled.

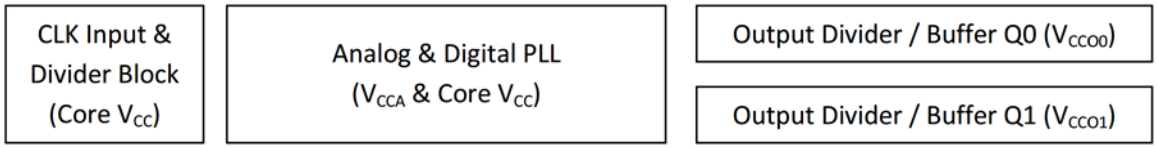
The 8T49N234 device is designed and characterized to operate within the ambient industrial temperature range of -40°C to 85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below are generated using maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

Power Domains

The 8T49N234 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). *Figure 31* below indicates the individual domains and the associated power pins.

Figure 31: Power Domains



Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core and analog voltage supplies from *Table 23* and *Table 24*.
2. Determine the nominal power consumption of each enabled output path which consists of:
   a. A base amount of power that is independent of operating frequency, as shown in *Table 38* through *Table 46* (depending on the chosen output protocol).
   b. A variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in *Table 38* through *Table 46*.
3. All of the above totals are summed.

Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heatsink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in *Table 37* below. Please contact IDT for assistance in calculating results under other scenarios.

Table 37: Thermal Resistance θ_{JA} for 40-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	26.3°C/W	23.2°C/W	21.7°C/W

Current Consumption Data and Equations

Table 38: 3.3V LVPECL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00660	32.9
Q1	0.01088	44.4
FCLK		

Table 39: 3.3V HCSL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00647	33.5
Q1	0.01050	44.7

Table 40: 3.3V LVDS Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00716	41.9
Q1	0.01145	52.8

Table 41: 3.3V LVCMOS Output Calculation Table

Output	Base_Current (mA)
Q0	31.3
Q1	42.1

Table 42: 2.5V LVPECL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00483	27.6
Q1	0.00865	38.3
FCLK		

Table 43: 2.5V HCSL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00425	27.7
Q1	0.00827	38.5

Table 44: 2.5V LVDS Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00483	36.0
Q1	0.00906	46.3

Table 45: 2.5V LVCMOS Output Calculation Table

Output	Base_Current (mA)
Q0	25.8
Q1	36.0

Table 46: 1.8V LVCMOS Output Calculation Table

Output	Base_Current (mA)
Q0	22.8
Q1	33.1

Applying the values to the following equation will yield output current by frequency:

Qx Current (mA) = FQ_Factor * Frequency (MHz) + Base_Current

where:

Qx Current is the specific output current according to output type and frequency

FQ_Factor is used for calculating current increase due to output frequency

Base_Current is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$T_J = T_A + (\theta_{JA} * Pd_{total})$

where:

T_J is the junction temperature (°C)

T_A is the ambient temperature (°C)

θ_{JA} is the thermal resistance value from Table 48, dependent on ambient airflow (°C/W)

Pd_{total} is the total power dissipation of the 8T49N234 under usage conditions, including power dissipated due to loading (W).

Note that the power dissipation per output pair due to loading is assumed to be 27.95mW for LVPECL outputs and 44.5mW for HCSL outputs. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using C_{PD} (found in Table 26) and output frequency:

$Pd_{OUT} = C_{PD} * F_{OUT} * V_{CCO}^2$

where:

Pd_{OUT} is the power dissipation of the output (W)

C_{PD} is the power dissipation capacitance (F)

F_{OUT} is the output frequency of the selected output (MHz)

V_{CCO} is the voltage supplied to the appropriate output (V)

Power Calculations Example

Table 47: Default Configuration (3.3V Core Voltage)

Output	Output Type	Frequency (MHz)	V_{CCO}
Q0	LVPECL	12	3.3V
Q1	LVCMOS	6	3.3V
FCLK	LVPECL	6	3.3V

- Core supply current + control and status supply current = $I_{CC} + I_{CCCS}$ = 56mA (max)
- Analog supply current, I_{CCA} = 121mA (max)
- Output supply current:
  Q0 current = 12MHz * 0.00660mA/MHz + 32.9mA = 32.98mA
  Q1 current = 42.1mA
  FCLK current = 6MHz * 0.01088mA/MHz + 44.4mA = 44.47mA
- Total output supply current = 119.6mA
- Total device current: 56mA + 121mA + 119.6mA = 296.6mA
- Total device power = 3.465V * 296.6mA = 1027.7mW
- Power dissipated through output loading:
  LVPECL = 27.95mW * 2 = 55.9mW
  LVCMOS = 0.94mW
  13pF * 6MHz * $(3.465V)^2$ * 1 output pair = 0.94mW
  Total power = 1027.7mW + 55.9mW + 0.94mW = 1084.54mW= 1.08W

With an ambient temperature of 85°C, and no air flow, the junction temperature is:

T_J = 85°C + 26.3°C/W * 1.08W = 113.4°C

This is below the limit of 125°C.

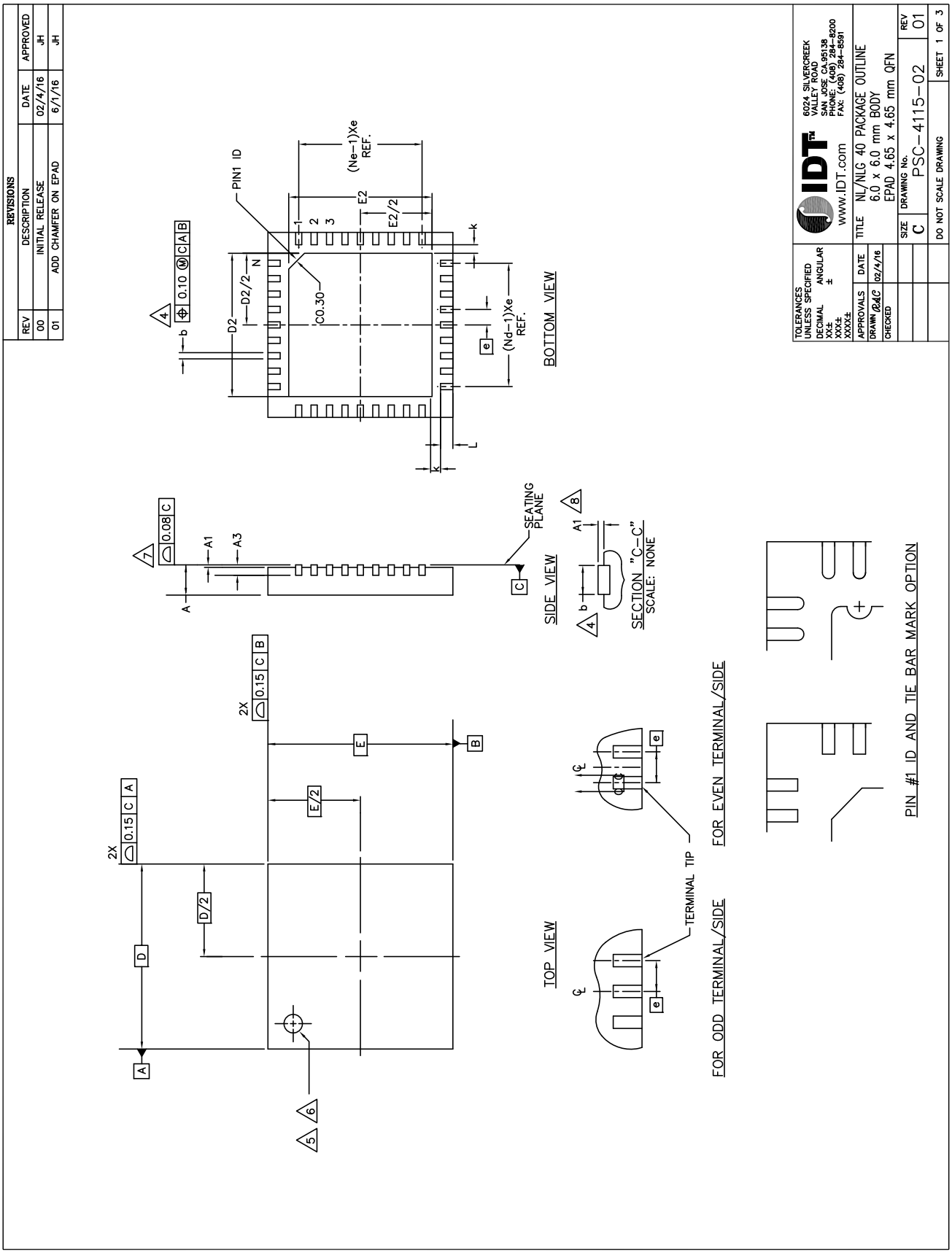
Table 48: θ_{JA} vs. Air Flow Table for a 40 Lead VFQFN[a]

θ_{JA} by Velocity			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	26.3°C/W	23.2°C/W	21.7°C/W

a. Assumes 5x5 grid of thermal vias under ePAD area for thermal conduction.

Package Drawings

Figure 32: Package Drawings



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH
01	ADD CHAMFER ON EPAD	6/1/16	JH

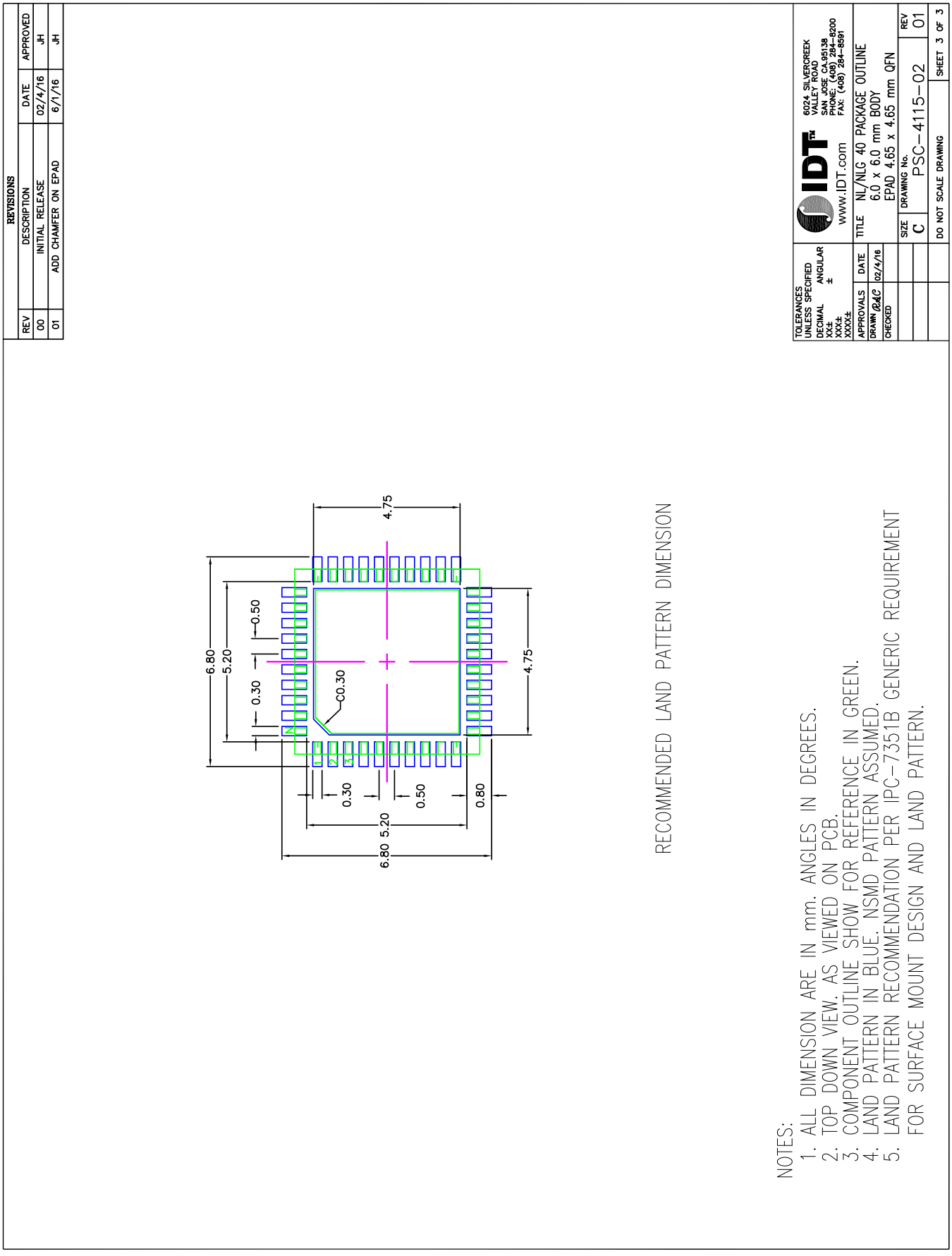
NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–220, VARIATION VJJC–3 & VJJD–5 WITH THE EXCEPTION OF D2 & E2.

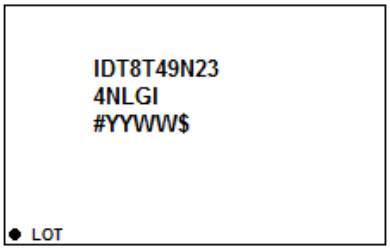
SYMBOL	DIMENSION			NOTE
	MIN	NOM	MAX	
b	0.18	0.25	0.30	4
D		6.00 BSC		
E		6.00 BSC		
D2	4.50	4.65	4.75	
E2	4.50	4.65	4.75	
L	0.30	0.40	0.50	
e		0.50 BSC		
k		0.275 REF.		
N		40		2
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.2 REF		
Nd		10		2
Ne		10		2

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com 6024 SILVERCREEK VALLEY ROAD SAN JOSE CA.95138 PHONE: (408) 284–8200 FAX: (408) 284–8591
APPROVALS DATE DRAWN RAC 02/4/16 CHECKED	TITLE NL/NLG 40 PACKAGE OUTLINE 6.0 x 6.0 mm BODY EPAD 4.65 x 4.65 mm QFN
	SIZE C · DRAWING No. PSC–4115–02 · REV 01
	DO NOT SCALE DRAWING · SHEET 2 OF 3

Figure 34: Package Drawings, continued



Marking Diagram



1. Line 1 and 2: part number
2. Line 3:
   - "#": stepping
   - "YYWW": the last two digits of the year and week that the part was assembled
   - "$": mark code

Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N234NLGI	IDT8T49N234NLGI	40 Lead VFQFN, Lead-Free	Tray	-40°C to +85°C
8T49N234NLGI8	IDT8T49N234NLGI	40 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to +85°C

Revision History

Revision Date	Description of Change
December 13, 2016	Initial release.

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