

Silicon PNP Power Transistors

2SB449

DESCRIPTION

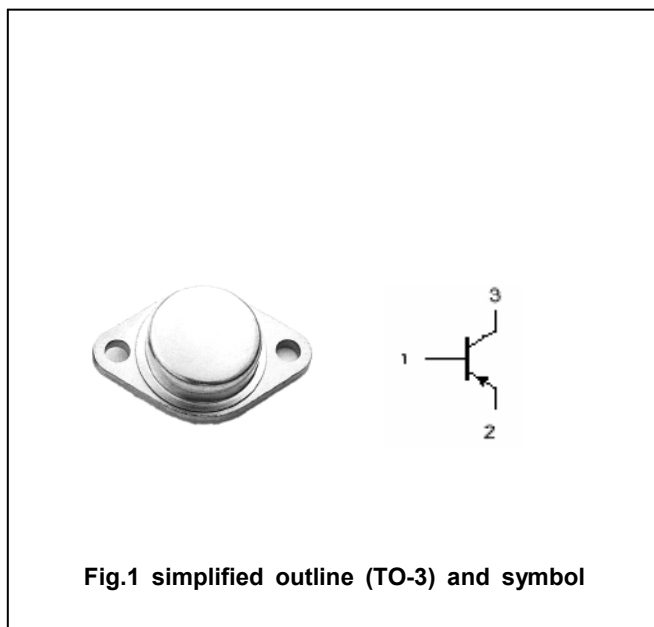
- With TO-3 package
- Low collector saturation voltage
- Wide area of safe operation

APPLICATIONS

- Power amplifier applications
- Power switching applications
- DC-DC converters

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-50	V
V_{CEO}	Collector-emitter voltage	Open base	-50	V
V_{EBO}	Emitter-base voltage	Open collector	-7	V
I_C	Collector current		-3.5	A
P_C	Collector power dissipation	$T_C = 50 \square$	22.5	W
T_j	Junction temperature		150	$\square$
T_{stg}	Storage temperature		-55~150	$\square$

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CHARACTERISTICS

Tj=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	$I_C=-10mA ; I_B=0$	-50			V
$V_{(BR)CBO}$	Collector-base breakdown voltage	$I_C=-1mA ; I_E=0$	-50			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	$I_E=-1mA ; I_C=0$	-7			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=-3A ; I_B=-0.3A$			-0.7	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=-3A ; I_B=-0.3A$			-1.2	V
I_{CBO}	Collector cut-off current	$V_{CB}=-50V ; I_E=0$			-10	μA
I_{EBO}	Emitter cut-off current	$V_{EB}=-7V ; I_C=0$			-10	μA
h_{FE}	DC current gain	$I_C=-3A ; V_{CE}=-2V$	20		85	

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PACKAGE OUTLINE

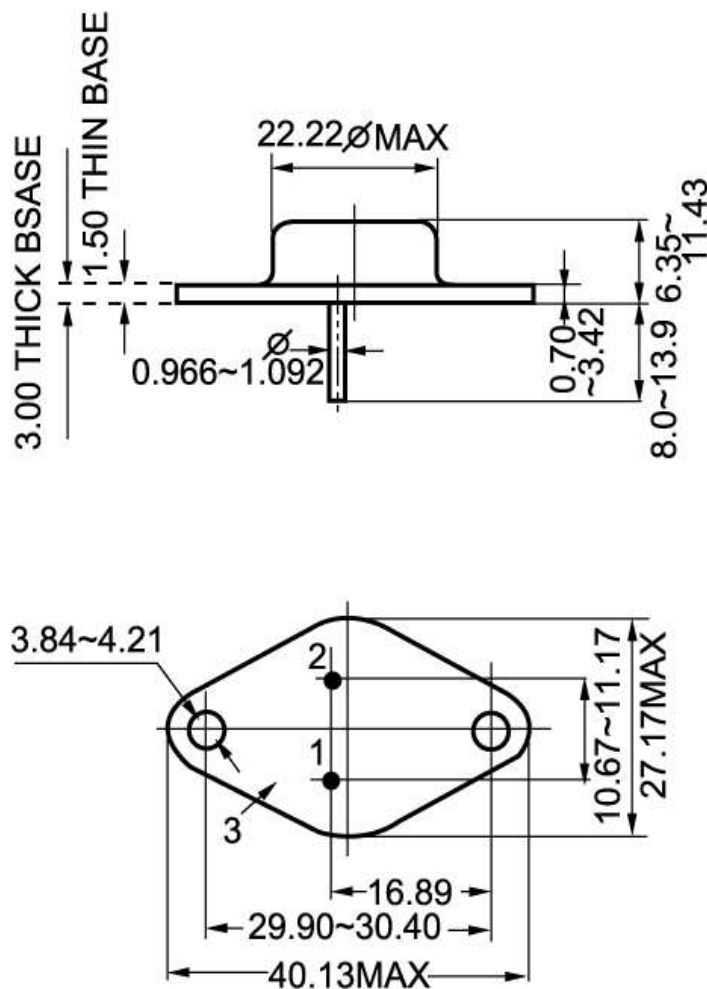


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)