ABRIDGED DATA SHEET

EVALUATION KIT AVAILABLE

DS28C36 DeepCover Secure Authenticator

General Description

The DS28C36 is a secure authenticator that provides a core set of cryptographic tools derived from integrated asymmetric (ECC-P256) and symmetric (SHA-256) security functions. In addition to the security services provided by the hardware implemented crypto engines, the device integrates a FIPS/NIST true random number generator (RNG), 8Kb of secured EEPROM, a decrement-only counter, two pins of configurable GPIO, and a unique 64-bit ROM identification number (ROM ID).

The ECC public/private key capabilities operate from the NIST defined P-256 curve and include FIPS 186 compliant ECDSA signature generation and verification to support a bidirectional asymmetric key authentication model. The SHA-256 secret-key capabilities are compliant with FIPS 180 and are flexibly used either in conjunction with ECDSA operations or independently for multiple HMAC functions.

Two GPIO pins can be independently operated under command control and include configurability supporting authenticated and nonauthenticated operation including an ECDSA-based crypto-robust mode to support secure-boot of a host processor.

DeepCover embedded security solutions cloak sensitive data under multiple layers of advanced security to provide the most secure key storage possible. To protect against device-level security attacks, invasive and noninvasive countermeasures are implemented including active die shield, encrypted storage of keys, and algorithmic methods.

Applications

- IoT Node Crypto-Protection
- Accessory and Peripheral Secure Authentication
- Secure Storage of Cryptographic Keys for a Host Controller
- Secure Boot or Download of Firmware and/or System Parameters

Benefits and Features

- ECC-256 Compute Engine
  - FIPS 186 ECDSA P256 Signature and Verification
  - ECDH Key Exchange with Authentication Prevents Man-in-the-Middle Attacks
  - ECDSA Authenticated R/W of Configurable Memory
- FIPS 180 SHA-256 Compute Engine
  - HMAC
- SHA-256 OTP (One-Time Pad) Encrypted R/W of Configurable Memory Through ECDH Established Key
- Two GPIO Pins with Optional Authentication Control
  - Open-Drain, 4mA/0.4V
  - Optional SHA-256 or ECDSA Authenticated On/Off and State Read
  - Optional ECDSA Certificate to Set On/Off after Multiblock Hash for Secure Boot
- RNG with NIST SP 800-90B Compliant Entropy Source with Function to Read Out
- Optional Chip Generated Pr/Pu Key Pairs for ECC Operations
- 17-Bit One-Time Settable, Nonvolatile Decrement-Only Counter with Authenticated Read
- 8Kbits of EEPROM for User Data, Keys, and Certificates
- Unique and Unalterable Factory Programmed 64-Bit Identification Number (ROM ID)
  - Optional Input Data Component to Crypto and Key Operations
- I^2C Communication, 100kHz and 400kHz
- Operating Range: 3.3V ±10%, -40°C to +85°C
- 6-Pin TDFN Package

Ordering Information ***appears at end of data sheet.***

Typical Application Circuit ***appears at end of data sheet.***

19-8546; Rev 0; 6/16

maxim integrated™

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to GND .....-0.5V to 4.0V
Maximum Current into Any Pin.....20mA
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow)..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.97	3.3	3.63	V
Active Supply Current	I_{CC}	(Note 2)			300	µA
Standby Supply Current	I_{CCS}				250	µA
Computation Current	I_{CMP}	Refer to the full data sheet				mA
GPIO						
Output Low	$PIOV_{OL}$				0.4	V
Input Low	$PIOV_{IL}$		-0.3		V_{CC} x 0.3V	V
Input High	$PIOV_{IH}$		V_{CC} + 0.7V		V_{CC} + 0.3V	V
Leakage current	I_L		-10		10	µA
ECC ENGINE						
Generate ECDSA Signature Time	t_{GES}	Refer to the full data sheet				ms
Generate ECC Key Pair	t_{GKP}					ms
Verify ECDSA Signature or Compute ECDH Time	t_{VES}					ms
SHA-256 ENGINE						
Computation Time (HMAC or RNG)	t_{CMP}	Refer to the full data sheet				ms
EEPROM						
W/E Endurance	NCY	T_A = +25°C (Notes 4, 5)	100K			—
Read Memory Time	t_{RM}				1	ms
Write Memory Time	t_{WM}	Refer to the full data sheet				ms
Data Retention	t_{DR}	T_A = +85°C (Notes 6, 7)	10			years
I^2C SCL AND SDA PINS (Note 8)						
Low-Level Input Voltage	V_{IL}		-0.3		0.15 × V_{CC}	V
High-Level Input Voltage	V_{IH}		0.7 × V_{CC}		V_{CC} + 0.3V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	(Note 9)		0.05 × V_{CC}		V
Low-Level Output Voltage at 4mA Sink Current	V_{OL}				0.4	V

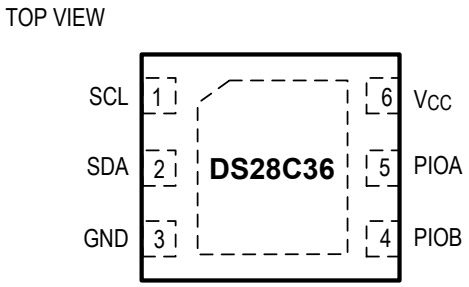
Electrical Characteristics (continued)

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF	t_{OF}	(Note 9)		30		ns
Pulse Width of Spikes that are Suppressed by the Input Filter	t_{SP}	(Note 9)			50	ns
Input Current with an Input Voltage Between 0.1VCCmax and 0.9VCCmax	II		-10		+10	µA
Input Capacitance	CI	(Note 9)		10		pF
SCL Clock Frequency	f_{SCL}	(Note 10)	0		400	kHz
Hold Time (Repeated) START Condition	$t_{HD:STA}$	After this period, the first clock pulse is generated	0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 9, 11, 12)			0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 13)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Capacitive Load for Each Bus Line	C_B	(Notes 10, 14)			400	pF
Warm-Up Time	t_{OSCWUP}	(Note 15)			250	µs

Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values at +25°C.
Note 2: Operating current continuously reading memory at 400kHz with < 25ns rise and fall times on SDA and SCL.
Note 3: Refer to the full data sheet.
Note 4: Write-cycle endurance is tested in compliance with JESD47H.
Note 5: Not 100% production tested; guaranteed by reliability qualification.
Note 6: Data retention is rested in compliance with JESD47H.
Note 7: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.
Note 8: All I^2C timing values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels, except for t_{OF}, which is measured from $V_{IH(MIN)}$ to 0.3 x V_{CC}.
Note 9: Guaranteed by design and/or characterization only. Not production tested.
Note 10: System requirement.
Note 11: The DS28C36 provides a hold time of at least 100ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to brigde the undefined regin of the falling edge of SCL. The master can provide a hold time of 0ns when writing to the device.
Note 12: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock (I^2C-bus specification Rev. 03, 19 June 2007).
Note 13: A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU:DAT} \geq$ 250ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I^2C-bus specification) before the SCL line is released. Also, the acknowledge timing must meet this set-up time. (I^2C-bus specification Rev. 03, 19 June 2007)
Note 14: C_B = total capacitance of one bus line in pF. The maximum bus capacitance allowable can vary from this value depending on the actual operating voltage and frequency of the application (I^2C-bus specification Rev. 03, 19 June 2007).
Note 15: I^2C communication should not take place for max t_{OSCWUP} time following a power-on reset.

Pin Configuration

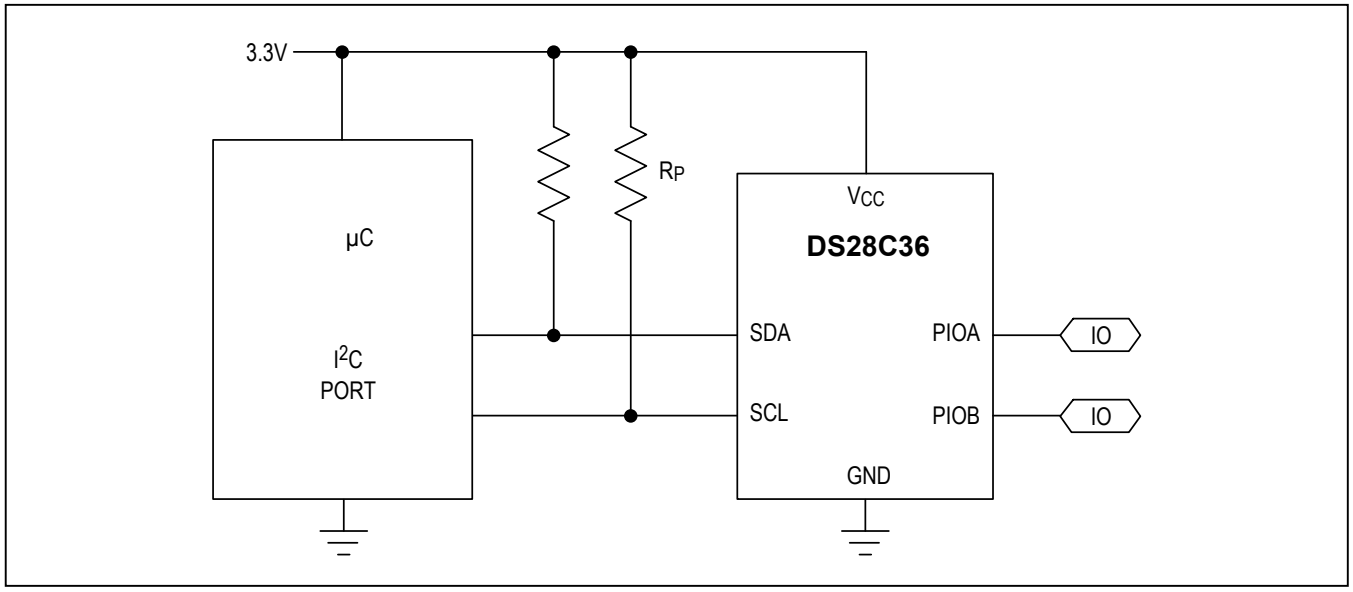


TDFN-EP
(3mm x 3mm)

Pin Description

PIN	NAME	FUNCTION
1	SCL	I^2C CLK
2	SDA	I^2C Data
3	GND	Ground
4	PIOB	General-Purpose IO
5	PIOA	General-Purpose IO
6	VCC	Supply Voltage

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28C36Q+T	-40°C to +85°C	6 TDFN-EP* (2.5k pcs)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T= Tape and reel.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 TDFN-EP*	T633+2	21-0137	90-0058

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

