Rev: 102108

DS33M30 Demo Kit

General Description

The DS33M30 demo kit (DK) is an easy-to-use evaluation board for the DS33M30 Ethernet-over-SONET/SDH devices. Maxim's ChipView software is provided with the demo kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

Windows is a registered trademark of Microsoft Corp.

Demo Kit Contents

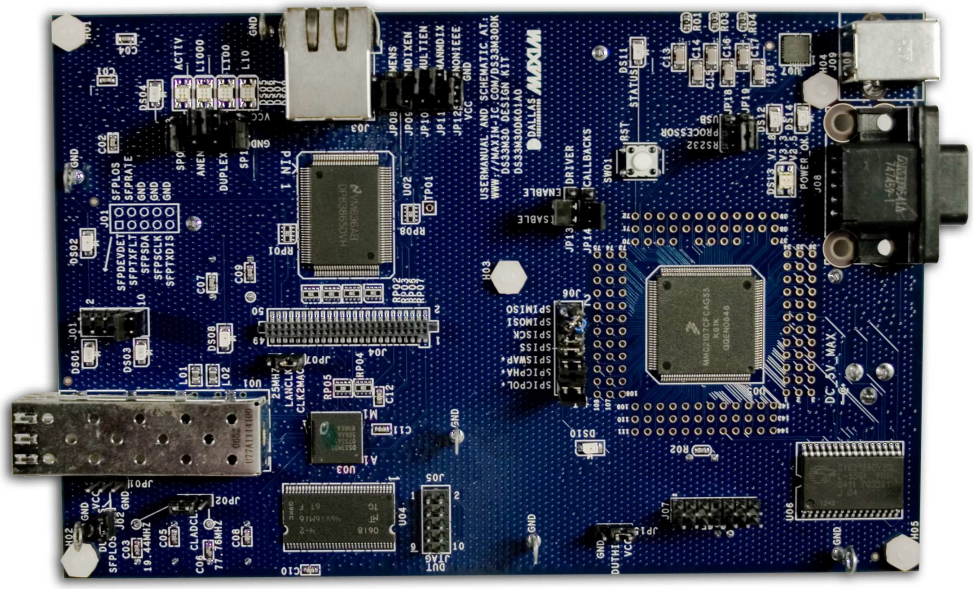
DS33M30DK Board
CD Including:
- ChipView Software
- DS33M30 Definition Files
- DS33M30DK Data Sheet
- DS33M30 Data Sheet

Features

- **Demonstrates Key Functions of DS33M30 Ethernet Transport Chipset**
- **Includes Ethernet PHY Supporting Gigabit Mode**
- **Includes Optical SFP Module for SONET/SDH Interface**
- **Network Connectors, Transformers, and Termination Ease Connectivity**
- **Careful Layout Provides Signal Integrity**
- **On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS33M30 Register Set**
- **All System Side and Overhead Pins are Easily Accessible for External Data Source/Sink**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

Ordering Information

PART	TYPE
DS33M30DK	Demo Kit for DS33M30



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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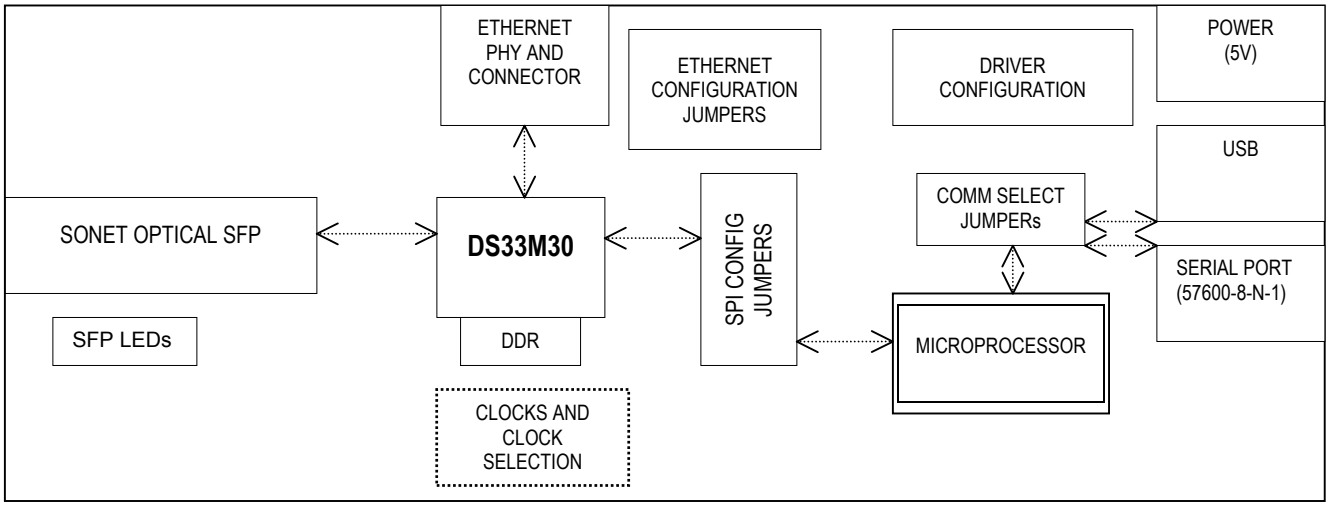
1. Board Floorplan

Figure 1-1. DS33M30DK Board Floorplan



2. PCB Errata

DS33M30DK02A0 errata:

- Silkscreen for JP08 should designate the jumper function as Mac clock enable. Instead it designates the function as MDIX enable
- Silkscreen for JP09 should designate the jumper function as MDIX enable. Instead it designates the function as Mac clock enable.
- SRAM devices U06 and UB09 have been reworked to connect pin 1 and pin 2. On the PCB this appears as a solder bridge between pin 1 and pin 2. This has been done to allow either a 128K*8 or a 512k*8 SDRAM to be installed and used as a 128K*8 device.

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3. File Locations

This demo kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website www.maxim-ic.com/DS33M30DK. All locations are given relative to the directory in the CD/zip file called "_def_ini_DS33M30".

Table 3-1. Definition and Configuration Files

FILE NAME	FILE USAGE
. \ _DS33M_GlobalSonet.def	Top level definition file to select in ChipView's register mode. This file will autoload the remaining definition files for the DS33M30 when parallel mode is used.
.\ds33M_BufferMan.def .\ds33M_EncapDecap.def .\ds33M_GlobalEth.def .\ds33M_group.def .\ds33M_LanSubscriber.def .\DS33M_serial_1234.def	DS33M30 dependent files. These are called by _DS33M_GlobalSonet.def file, which is listed above.
.\m30_rx_tx_simulation 19mhz.mfg .\m30_STS3c_bert_LoopTime.mfg .\m30_STS3c_SONET_Loopback.mfg ._m30_STS3c_Ethernet_Loopback.mfg ._m30_STS3c_GFPNull_NoScramble.mfg	Files for manually configuring the DS33M30.

4. Basic Operation

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

4.1 Powering Up the Demo Kit

- Connect PCB power jack to the wall adapter.
- Connect RS-232 serial cable, or USB cable between the host PC and demo kit.
- Verify that the jumpers are configured as described in Table 5-1.

4.1.1 General

- Upon power-up the power LEDs (DS13, DS12, DS14 green) will be lit.
- PHY LINK LED should be lit if an Ethernet cable is connected. Note that there are three link LEDs, as the DS33M30 is a Gigabit mode device. The L1000 LED should be litl the L100 and L10 LEDs should not be lit.

Following are several basic system initializations.

4.2 Basic DS33M30 Initialization

This section covers two basic methods for configuring the DS33M30.

1. Device Driver-Based Configuration: (Note: The DS33M3001A0 board revision does not come loaded with device drivers.) If the pins J20.1+J20.2 are jumpered, the device driver autoconfigures the DS33M30 upon power-up. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. To load the GUI interface for the device drivers, go to the ChipView register mode **Tools** menu and select **Tools→Plugins→DS33M30/M33 Device Driver Demo**.
2. Register-Based Configuration: EoS VC3 with two ports assigned to VCG1.
    a. Remove jumper J20.1+J20.2 to disable device drivers and reset the board.
    b. Launch ChipView.exe and select **Register View**.

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c. When prompted for a definition file, pick the file named **_DS33M30_GlobalMicroport.def**. Several additional definition files will load.
d. Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **_m30_STS3c_GFPNull_NoScramble.mfg**.

4.2.1 Additional Configuration for DS33M30

- Using either a patch or crossover cable, connect the Ethernet connector to an ordinary PC or network test equipment. This should cause the link LED to turn on.
- Place a loopback connector at the SONET network side; the optical LOS LEDs should go out.
- At this point any packets sent to the DS33M30 are echoed back. Incoming packets (i.e., ping) should cause the Activity LED to blink.
- Note that ChipView.exe display settings can be changed using the **Options→Settings** menu.

4.3 Monitor and Capture Ethernet Traffic

- Although ping is mentioned, it is **not** the recommended frame source for testing. The ping command goes through the computer's TCPIP stack and sometimes is not sent out the PC's network connector (i.e., if the PC's ARP cache is out of date). Additionally, ping requires two PCs, as a Windows PC with only one adapter cannot ping itself (i.e., a local ping gets sent to 'local host' instead of out the connector). With that said, ping is still a valuable test once the prototyping stage is complete.
- Generation and capture of arbitrary (raw) packets can be accomplished using **CommView**. A full-featured demo is available at www.tamos.com/products/commview.
- Wireshark (formerly Ethereal) is a free packet capture utility. Download is available at www.wireshark.org.
- Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters, the PC has a different IP address for each adapter. Test equipment allows selection of either adapter. Operating system-based network traffic is sent out the default adapter, which usually is the adapter that has recently had connection to a live network.

5. Jumpers and Connectors

Jumpers and connectors are listed in Table 5-1. They are listed in order of appearance on the PCB from left to right, top to bottom (as viewed with SONET connector on the left side of the board).

Table 5-1. Jumpers and Connectors

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J03	Ethernet Connection	Connected	14	Connect to Gigabit Ethernet source.
JP06 + JP03	Bias PHY Speed1 + Speed0	Jumper P2+3(high) P2+1 (low)	14	If auto negotiation is enabled this setting advertises capability for 1000 speeds. If auto negotiation is disabled then this setting forces 1000Mb mode.
JP04	Bias PHY ANEN	Jumper P2+3 (high)	14	Jumper P2+3 to enable auto negotiation.
JP05	Bias PHY Duplex	Jumper P2+3 (high)	14	Jumper P2+3 to enable full duplex, Jumper P1.2 to force half duplex.
JP09	Bias PHY MdixEn	Jumper P2+1 (high)	14	P2+3 disables pair swap mode, P2+1 enables pair swap mode.
JP08	Bias PHY MacClkEn	Jumper P2+3 (low)	14	P2+3 PHY clock to mac output is disabled, P1+2 PHY clock to mac output is enabled. Mac clock only needs to be enabled in Gigabit mode.

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SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
DS05	LED activity	--	14	Flashes for PHY Tx-Rx activity.
DS06 DS07 DS09	LED link speed	DS06 shold be lit (when linked)	14	LED to indicate link speed: 1000, 100, or 10Mbps. Only DS06 should be lit since the DS33M30 is GMII only.
J04	PHY test points	--	12	PHY test points. The connector pinout is compatible with existing PHY cards, but cannot be used with U04 on the board.
JP13 JP14	Runtime options	NA	11	Currently the device drivers do not fit in flash, and are not loaded to the DK.
DS11	Status	—	11	LED kit status, not lit.
J03	USB	—	11	USB interface. See folder marked USBdrivers_CP210x for drivers.
J04	RS232 DB9 connector	—	11	RS-232 DB-9 connector, operates in ASCII mode at 57.6K,8,N,1.
JP18 JP19	Comm Port	Jumper P1+2 P1+2	11	Jumper pins 1+2 to select the RS232 transceiver. Jumper pins 2+3 to select the USB to serial converter.
SW01	Reset	—	7	System Reset button.
J06	SPI	All jumpered	6	SPI™ bias and data pins. Control by external processor is possible after removing CS, MISO, MOSI, and SCK
JP15	HIZ	Jumper P2+3	6	Dut three-state control.
J07	Software Debug	—	11	ONcE EBDI.
JP07	Clock select	Jumper P2+1	4	Clock selection for PHY and Ethernet side of DS33M30.
JP02	Clock select	Jumper P1+2	4	Clad clock selection, Jumper P1+2 to drive with 19.44MHz. Jumper P2+3 to drive with 77.76MHz clock.
DS08	DS33M30 Int	—	9	LED, lit when DS33M30 Interrupt is asserted.
J01	SFP test points	Jumper P9+10		Test points for SFP module.
DS01	SFP MOD0	—	2	Lit when a SFP module is installed.
DS03	SFP TXDISABLE	—	2	Lit when Tx is enabled.
DS02	SFP LOS	—	2	Lit when fiber optic cable is removed.
J02 JP01	SFP LOS/M33 LOS	Jumper	2	Jumper J02 to connect SFP LOS to DS33M30 LOS. If J02 is removed, then JP01 can be used to pull DS33M30 LOS high or low.
U01	SFP	Installed	2	SFP module.
J05	JTAG	—	6	DS33M30 JTAG.

SPI is a trademark of Motorola, Inc.

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6. Line-Side Connections

The DS33M30DK has one optical port and one Ethernet port.

7. Microcontroller

The microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS33M30 and the FPGAs.

8. Power-Supply Connectors

Connect a 5.0V wall adapter to the PCB power jack. LED DS1 provides indications that a 5.0V supply is connected properly. The board power supplies (3.3V, 2.5V, and 1.8V) are regulated to supply proper voltages to various circuits on the board.

9. Connecting to a Computer

Both USB and serial modes are supported.

To connect through a RS-232 serial port, set jumpers JP25 and JP26 jumpers to pins 1+2, identified in the silkscreen as RS232,PROCESSOR. Connect a standard DB-9 serial cable between the serial port on the DS33M30DK and an available serial port on the host computer. The host computer must be a Windows-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

To connect through USB, set jumpers JP25 and JP26 jumpers to pins 3+2, identified in the silkscreen as USB, PROCESSOR. Connect a USB cable between the DS33M30DK USB connector and the PC. The host computer must be a Windows-based PC, which should automatically recognize the device as a virtual com port and assign the device drivers. If drivers are not automatically assigned, direct the **New Hardware** wizard to the driver files on the CD in the folder marked **USBdrivers_CP210x**.

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10. Installing and Running the Software

ChipView is a general-purpose program that supports a number of Maxim demo kits. To install the ChipView software, run Chipview.msi from the disk included in the DS33M30DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS33M30DK.

After installation, run the ChipView program with the DS33M30DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Maxim evaluation platforms. In the active subwindow, select the _DS33M_GlobalSonet.def definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS33M30's register map. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

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11. Address Map

SPI mode address space begins at 0x0.

Table 11-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000	DS33M30	DS33M30 registers

12. Additional Information/Resources

12.1 DS33M30 Information

For more information about the DS33M30, refer to the DS33M30 data sheet at www.maxim-ic.com/DS33M30.

12.2 DS33M30DK Information

For more information about the DS33M30DK, refer to the DS33M30DK Quick View page at www.maxim-ic.com/DS33M30DK.

12.3 Technical Support

For additional technical support, submit your questions at www.maxim-ic.com/support.

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13. Component List

DESIGNATION	DESCRIPTION	SUPPLIER	PART
C01, C03, C05, C06, C09, C11, CB11, CB12, CB15, CB16, CB17, CB19, CB20, CB24, CB39, CB44, CB45, CB48, CB56, CB57, CB60, CB66, CB71, CB74, CB75, CB88, CB97, CB101, CB112	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
Component listing on next line, begins with C02	0603 CERAM 4.7uF 6.3V MULTILAYER	Digi-Key	ECJ-1VB0J475M
C02, C04, C07, CB05, CB07, CB18, CB21, CB22, CB25, CB31, CB32, CB33, CB35, CB38, CB42, CB43, CB46, CB47, CB49, CB50, CB51, CB53, CB55, CB61, CB62, CB63, CB64, CB67, CB68, CB70, CB72, CB73, CB76, CB77, CB78, CB79, CB80, CB81, CB83, CB84, CB86, CB89, CB90, CB94, CB95, CB103, CB105, CB109, CB110, CB116, CB121			
C08, C10, C12, CB04, CB08, CB09, CB10, CB14, CB30, CB40, CB65, CB85, CB107	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
C1, C13, C14, C15, C16, C17, C18, CB120 , CB23, CB27, CB28, CB29, CB41, CB87, CB98, CB106	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB01, CB02, CB03, CB13, CB111	D CASE TANT 470uF 6.3V 20%	KEM	T491D477M006AS
CB06, CB26, CB34, CB36, CB37, CB52, CB54, CB58, CB59, CB69, CB82, CB91, CB92, CB93, CB96, CB102, CB108, CB114, CB115	0603 CERAM .1uF 16V 10%	Panasonic	ECJ-1VB1C104K
CB104, CB117	L_1206 CERAM 1uF 16V 10%	Panasonic	ECJ-3YB1C105K
CB113	1206 CERAM 4.7uF 25V 10% X5R	Panasonic	ECJ-3YB1E475K
CB99, CB100, CB118, CB119	L_D CASE TANT 68uF 16V 20%	Panasonic	ECS-T1CD686R
DB01	SCHOTTKY DIODE, 1 AMP 40 VOLT	Internatioanl Rectifier	10BQ040
DS01, DS03, DS11 , DS04, DS12, DS14	L_LED, GREEN, SMD	Panasonic	LN1351C
DS02, DS08, DS10	L_LED, RED, SMD	Panasonic	LN1251C
DS05, DS06, DS07, DS09	LED, GREEN/GREEN, SMD	LUMEX	67-1362-1-ND
DS13	LED, RED/GREEN, SMD	LITEON	160-1172-1-ND
GND_TP01, GND_TP02, GND_TP03, GND_TP04, GND_TP05, GND_TP06, GND_TPB01, GND_TPB02, GND_TPB03	STANDARD GROUND CLIP	KEYSTONE	4954
H01, H02, H03, H04, H05, H08	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	Labstock	4-40KIT4
J01	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Digi-Key	S2012-05-ND
J02, JB01	100 MIL 2 POS JUMPER	Labstock	NA
J03	CONNECTOR, SINGLE LEVEL, GIGABIT RJ-45, 10 PIN	Halo Electronics	HFJ11-1G02E

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J04	PLUG, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	SFM-125-L2-S-D-LC
J05	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Samtec	TSW-105-07-T-D
J06	HEADER, 14 PIN, DUAL ROW, VERT	Samtec	HDR-TSW-107-14-T-D
J07	100 MIL 2*7 POS JUMPER	Labstock	NA
J08	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J09	TYPE B SINGLE RT ANGLE, BLACK	Digi-Key	WM17108-ND
JB02	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A also requires 5V ACDC adapter INPUT 100-240VAC 50-60HZ 0.6A OUTPUT DC 5V 2.6A. PN DMS050260-P5P-SZ. MODEL 3Z-161WP05	CUI, INC	PJ-002AH
JP01, JP02, JP03, JP04, JP05, JP06, JP07, JP08, JP09, JP13, JP14, JP15, JP18, JP19	100 MIL 3 POS JUMPER	Labstock	NA
L01, L02	1uH ±10% 0805 Multilayer Ceramic 400 mA	TDK	GLF2012T1R0M
L1	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-10
R01, R03, R04, RB19	RES 0603 0.0 Ohm 1/16W 5%	Panasonic	ERJ-3GEY0R00V
R02	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
RB01, RB18 , RB03, RB20, RB22	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
RB02, RB04, RB12, RB13, RB14	RES 0603 30 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ300V
RB05	RES 0603 2.2K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ222V
RB06, RB07, RB16	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
RB08	RES 0603 100 Ohm 1/16W 1%	Panasonic	ERJ-3EKF1000V
RB09, RB11	RES 0603 1.00K Ohm 1/16W 1%	Panasonic	ERJ-3EKF1001V
RB15	RES 0603 9.76K Ohm 1/16W 1%	Panasonic	ERJ-3EKF9761V
RB17, RB21	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RP01, RP02, RP03, RP04, RP05, RP06, RP07, RP08, RPB12	RESISTOR, 4 PACK, 30 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V300JX
RPB01, RPB07, RPB20, RPB24	RESISTOR, 4 PACK, 330 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V331JX

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RPB02, RPB08, RPB11, RPB17, RPB19	RESISTOR, 4 PACK, 1K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V102JX
RPB03, RPB04, RPB13, RPB15, RPB18, RPB21, RPB22, RPB23, RPB25, RPB26, RPB27, RPB28, RPB29	RESISTOR, 4 PACK, 10K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V103JX
RPB05, RPB06, RPB14	RESISTOR, 4 PACK, 2.2K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V222JX
RPB09, RPB10	RESISTOR, 4 PACK, 50 OHM 2PCT QUAD 0603	KOA	CN1J4TTD500G
SW01	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
TP01	TEST POINT, 1 PLATED HOLE, DO NOT STUFF	Labstock	NA
U01	SFP host / receptacle	PARTS_KIT	SFP_HOST-TYCO
U02	GIG PHYTER V, 10/100/1000 ETHERNET PHYSICAL LAYER, 128 PIN QFP	National Semiconductor	DP83865DVH
U03	ETHERNET EXTENSION DEVICE	Dallas Semiconductor	DS33M30
U04	DOUBLE DATA RATE (DDR) SDRAM 2-2-2 TIMING 256MBITX16 TSSOP	MICRON	MT46V16M16TG-75E
U05	MMC2107 PROCESSOR	Motorola	MMC2107
U06, UB09	CYPRESS SRAM, LAB STOCK	Labstock	NA
U07	IC, SINGLE-CHIP USB TO UART BRIDGE, 28 PIN QFN	SIL	CP2101
U1	SPI SERIAL EEPROM 8M 8 PIN SOIC 3.3V	Atmel	AT26DF081A
UB01	IC, LINEAR REG 1.5W, 2.5V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-25
UB02	IC, LINEAR REG 1.5W, 1.8V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-18
UB03	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	Maxim	MAX811TEUS-T
UB04, UB05, UB07	IC, LINEAR REG 1.5W, 3.3V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-33
UB06	HIGH SPEED BUFFER	FAIRCHILD	NC7SZ86
UB08	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	MAX3233E
XB01	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
YB01	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 19.44 MHZ	SaRonix	SOCKET+NTH089A3-19.44

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YB02	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ	SaRonix	NTH089AA3-25.000+SOCKET
YB03	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 77.76 MHZ	SaRonix	SOCKET+NTH089A3-77.7600

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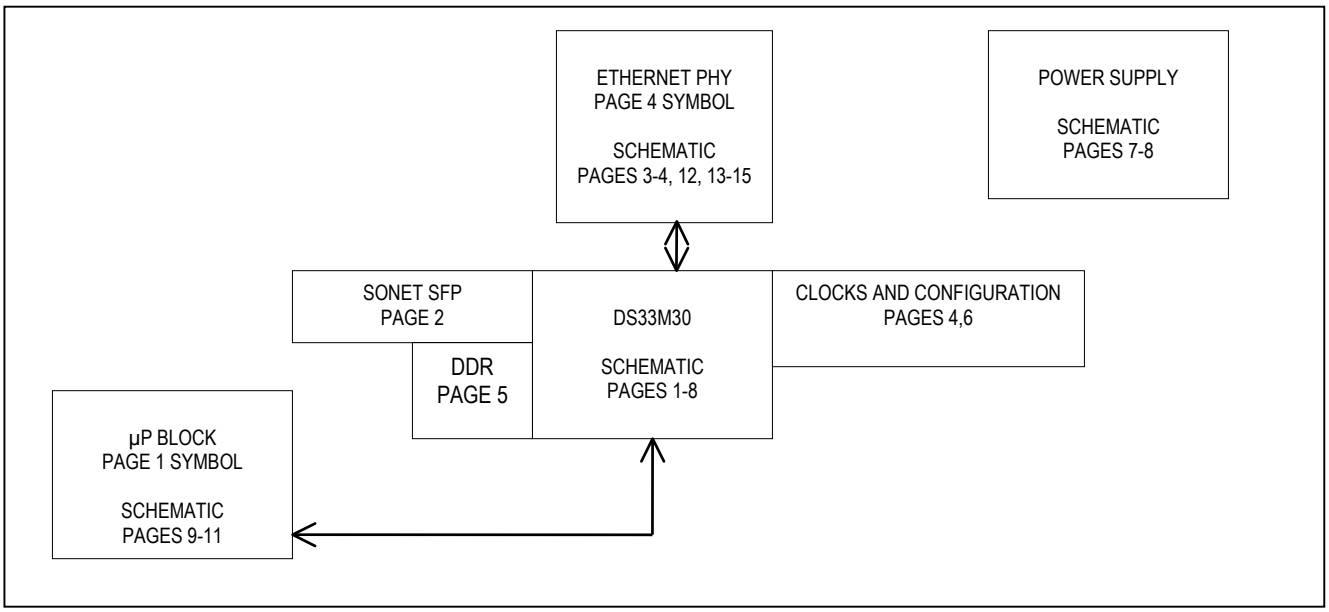
14. Schematics

The DS33M30DK schematics are featured in the following pages. The schematic contains three hierarchal blocks: Microcontroller, Ethernet PHY, and Ethernet Test Points.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. Figure 14-1 shows the system diagram in terms of hierarchal blocks with schematic page numbers given for each functional block.

Figure 14-1. DS33M30 PCB Layout and Schematic Hierarchy Block Page Listing



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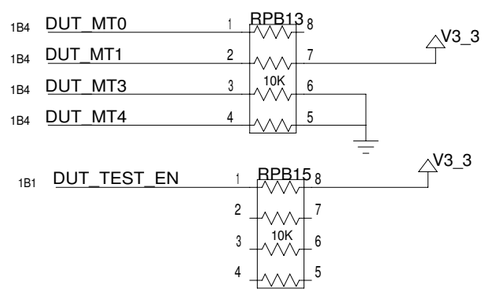
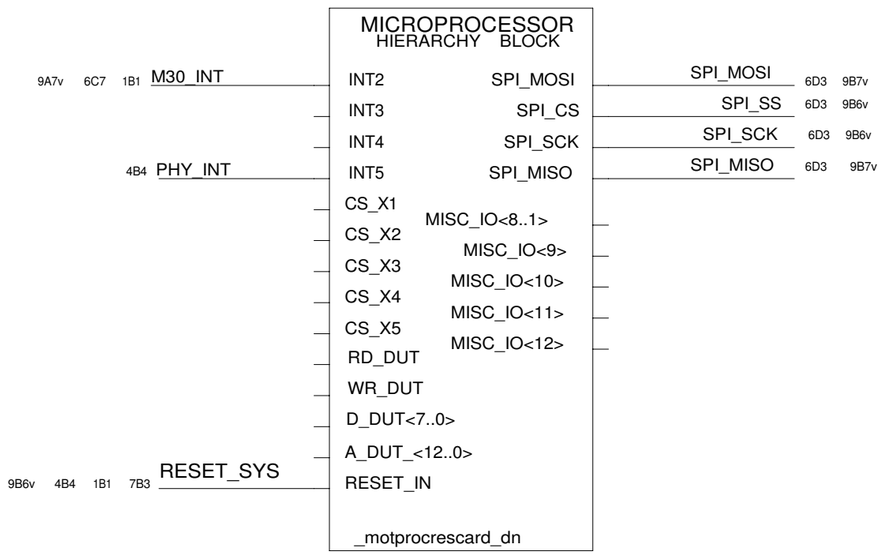
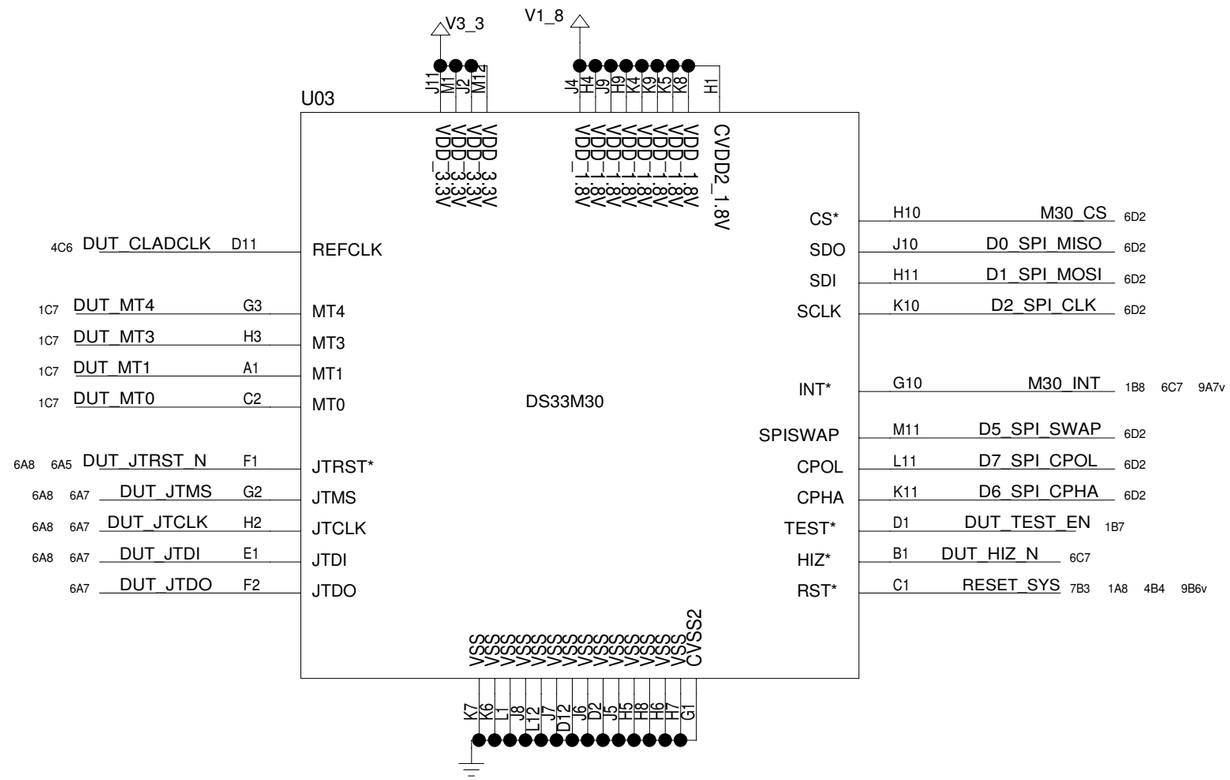




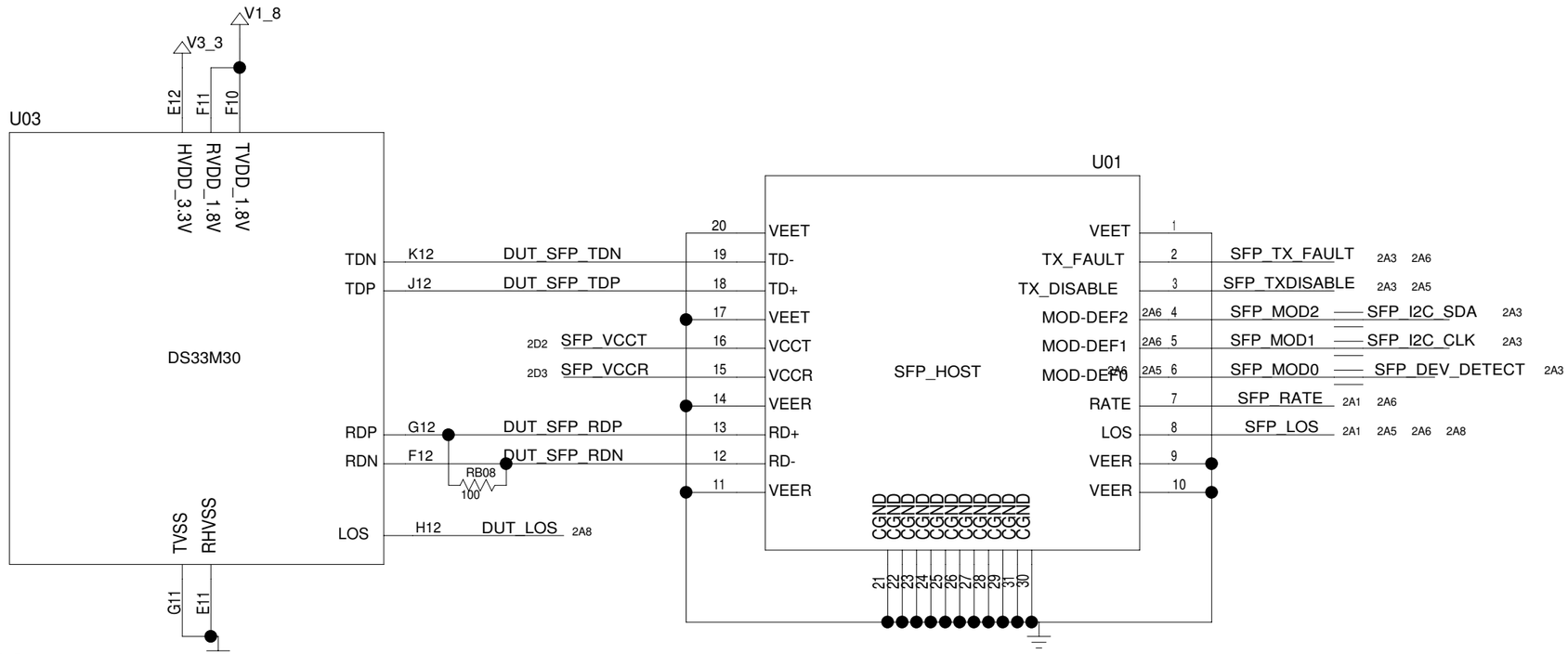


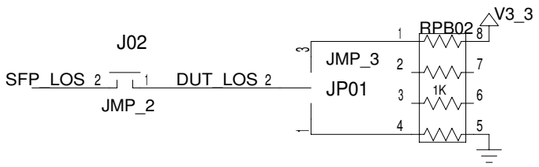
BEGINNING OF DS33M30DK

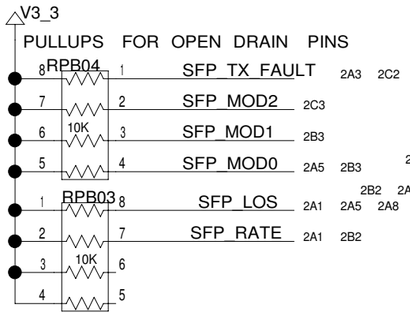
TITLE: DS33M30DK02A0 MICROPORT. P.1,9-11	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 1/8(BLOCK) 1/14(TOTAL)

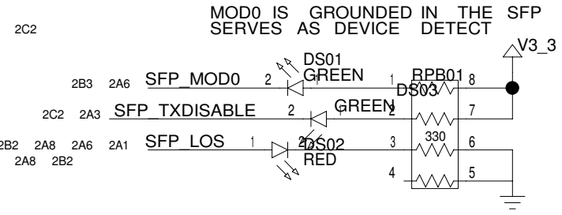
BLOCK NAME: _rc_top_dn_.

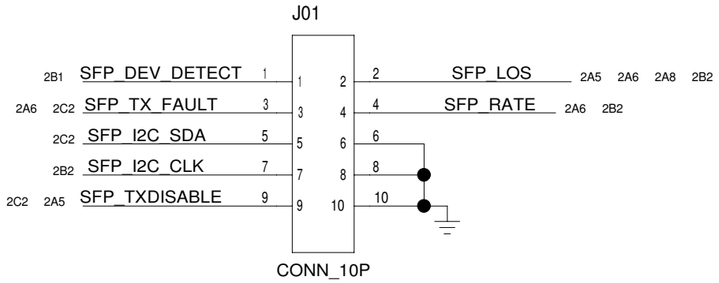
Downloaded from: http://www.datasheetcatalog.com/











TITLE: DS33M30DK02A0 SERDES. P.2	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 2/8(BLOCK) 2/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

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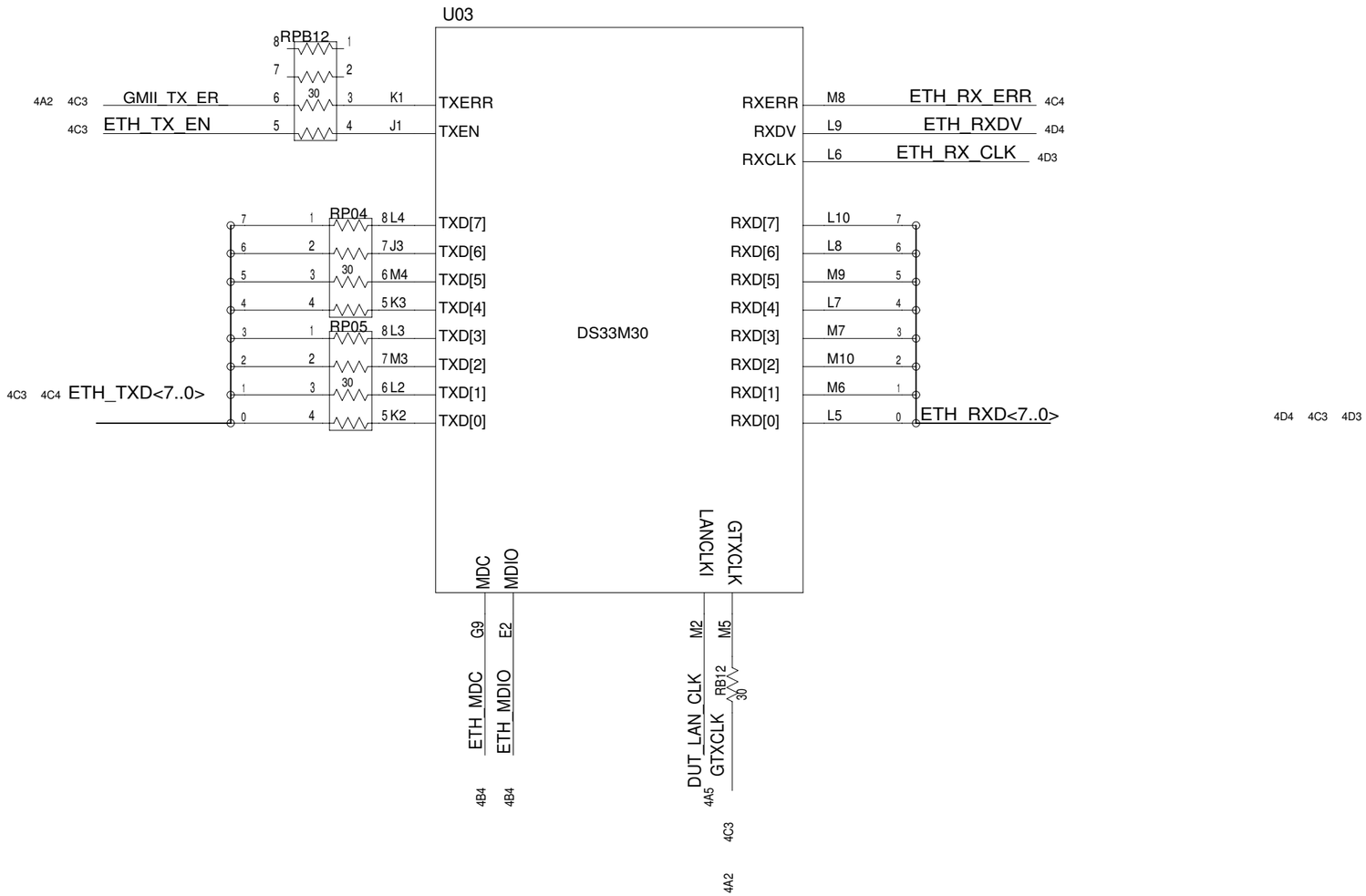

TITLE: DS33M30DK02A0 ETHERNET. P.3-4,12,13-15 ENGINEER: STEVE SCULLY	DATE: 03/10/2008 PAGE: 3/8(BLOCK) 3/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

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YB03
OSC
V3_3
VCC
GND
OUT
77.76MHZ_3.3V_SOCKET

YB01
OSC
V3_3
VCC
GND
OUT
19.44MHZ_3.3V_SOCKET

JMP_3
JP02
RB02
30
DUT_CLADCLK 1C4

YB02
25.000MHZ_3.3V_SOCKET
OSC
V3_3
VCC
GND
OUT
REFC_25M
JMP_3
RB04
30
PY25MHZOSC 4B4 12B5v 13B4v

JP07
RB14
30
DUT_LAN_CLK 3A4
RB13
30
AV_LAN_CLK 4B4 12B5v
ETH_REF_CLK IS ONLY
USED IN RMII MODE (50 MHZ)
CLK_TO_MAC
13B1v 12B5v 4B1 4C3

_phy_dp83865bvh_dn

COL_DET
RXD<7..0>
RXDV
RX_CLK
RX_CRS
RX_ERR
TXD<7..0>
TX_CLK
TX_EN
TX_ER_
CLKTOMAC
CLKTOMAC_TESTPNT
GMII_CLKFROM_MAC
GMII ONLY
LAN_CLK
PHYOSC25M
MDC
MDIO
RESET_B
PHY_INT
SPARE<4..1>

V3_3
RB05
2.2K

13A1v 12C5v ETH_COL_DET
ETH_RXD<7..0> 3B2 4C3 4D3 12B5v 12C5v 13A7v 13B7v
13B7v
13A1v 12C5v 4D4 3B2 ETH_RXD<3..0>
3C3 12C5v
ETH_RXDV
ETH_RX_CLK
12C5v 13A1v
ETH_RX_CRS
13A1v 12B5v
3C3
ETH_RX_ERR
ETH_TXD<7..0> 3B6 4C3 12B5v 12C5v 13B7v
13B7v 12C5v 3B6 4C4 ETH_TXD<3..0>
ETH_TX_CLK
ETH_TX_EN
GMII_TX_ER 3C6 4A2 12B5v 13A7v
CLK_TO_MAC 4A7 4B1 12B5v 13B1v
13A7v 12B5v 4D4 3B2 ETH_RXD<7..4>
GTXCLK 3A4 4A2 12B5v 13B7v
13B7v 12B5v 3B6 4C4 ETH_TXD<7..4>
AV_LAN_CLK
PY25MHZOSC
ETH_MDC
ETH_MDIO
RESET_SYS
PHY_INT

SINGLE 50 PIN
I.M. CARD PLUG-CONNECTORS
USED ON BOTTOM OF MOTHERBOARD
FOR CONNECTION TO ETHERNET CARD

_phy_imbus_mb_dn

PT1_COL_DET
PT1_RXD<3..0>
PT1_RXDV
PT1_RX_CLK
PT1_RX_CRS
PT1_RX_ERR
PT1_TXD<3..0>
PT1_TX_CLK
PT1_TX_EN
PT2_COL_DET
PT2_RXD<3..0>
PT2_RXDV
PT2_RX_CLK
PT2_RX_CRS
PT2_RX_ERR
PT2_TXD<3..0>
PT2_TX_CLK
PT2_TX_EN
LAN_CLK
OSC25M
MDC
MDIO
RESET_B
PHY_INT

ETHERNET (LAN)
CONNECTORS

SPARE
GMII_CLKFROM_MAC
GMII_TX_ER
GMII_CLKTOMAC_BUF

13B1v 12B5v 4C3 4A7 CLK_TO_MAC
13A7v 12B5v 4C3 3C6 GMII_TX_ER
13B7v 12B5v 3A4 4C3 GTXCLK

ETHERNET CONNECTOR (I.M. BUS)
IS INTENDED FOR USE AS TESTPOINTS
NOT CONNECTION TO A RESOURCE CARD

TITLE: DS33M30DK02A0 ETHERNET. P.3-4,12,13-15	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 4/8(BLOCK) 4/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

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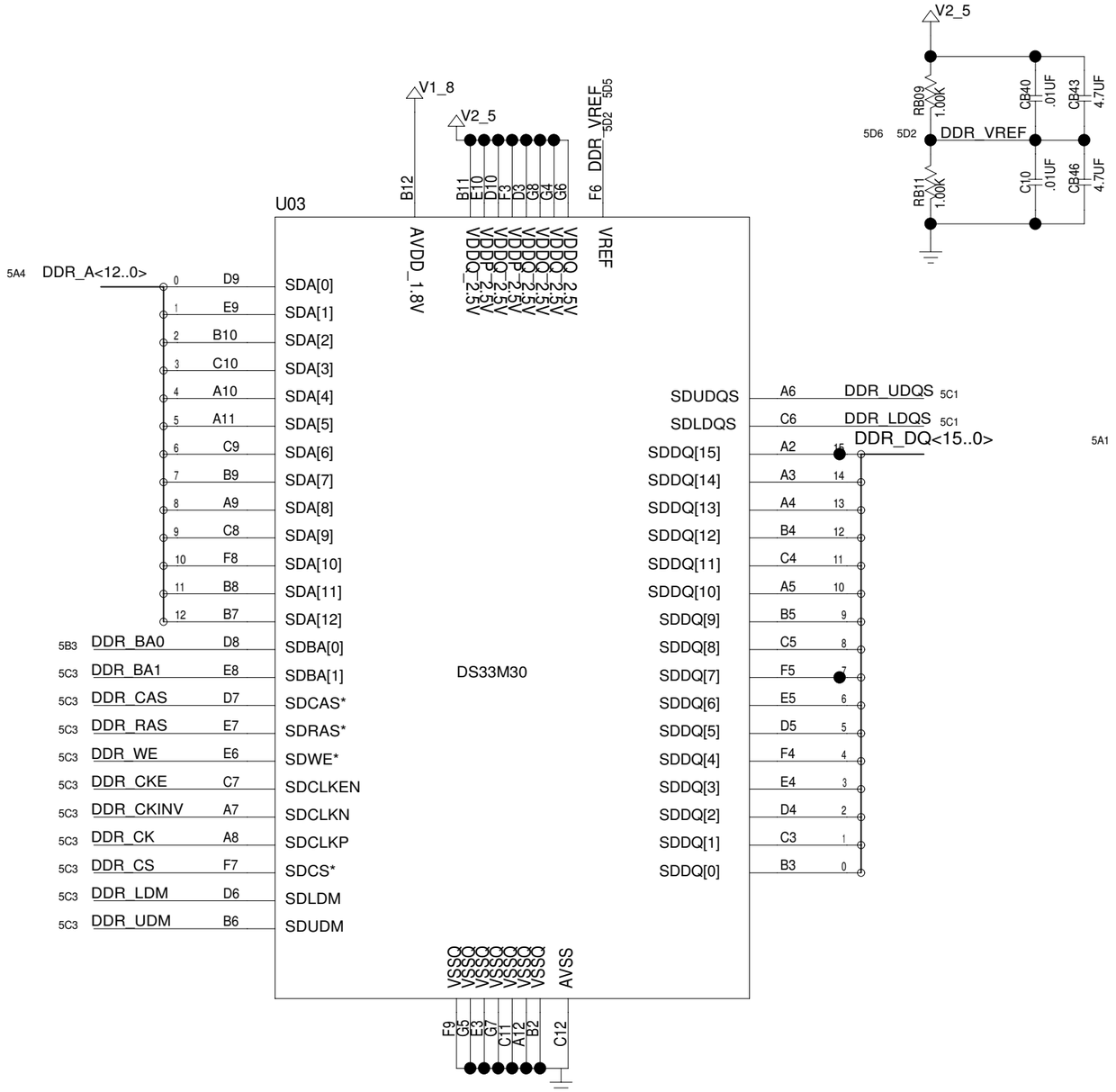

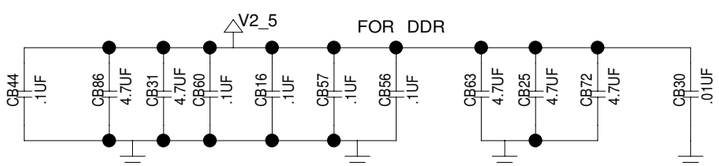

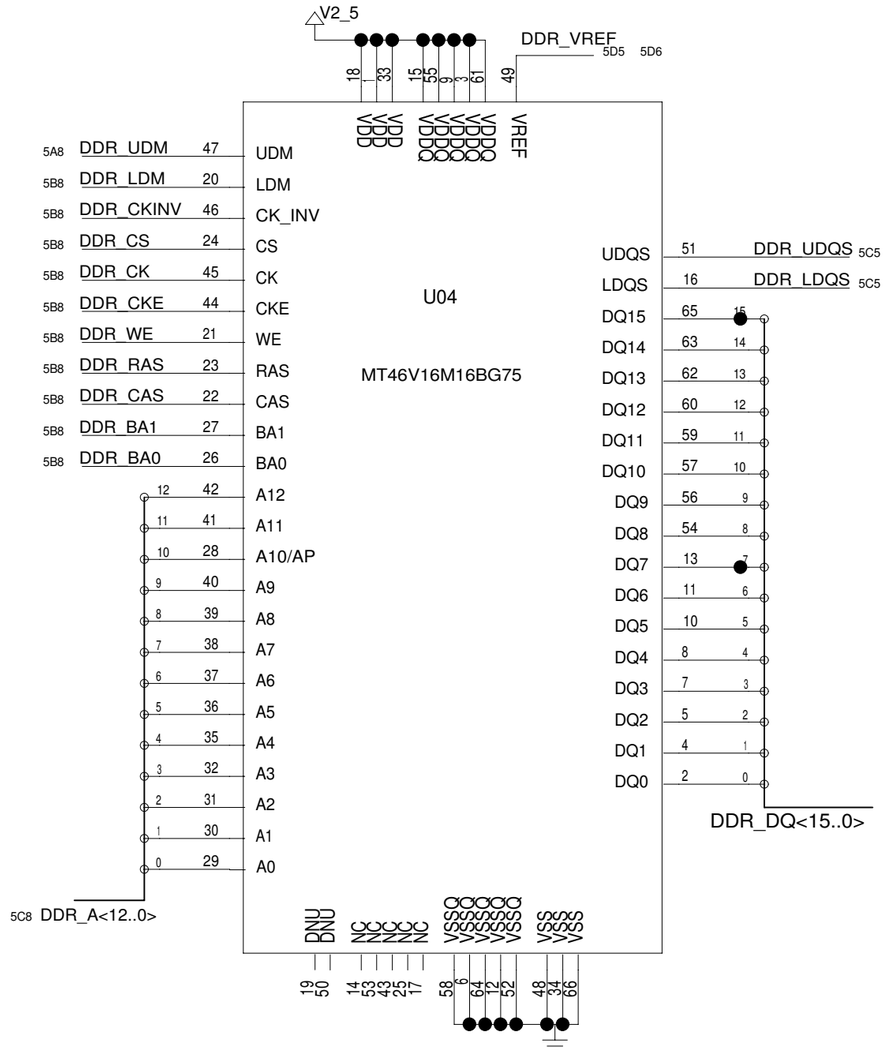

TITLE: DS33M30DK02A0 DDR MEMORY. P.5	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 5/8(BLOCK) 5/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

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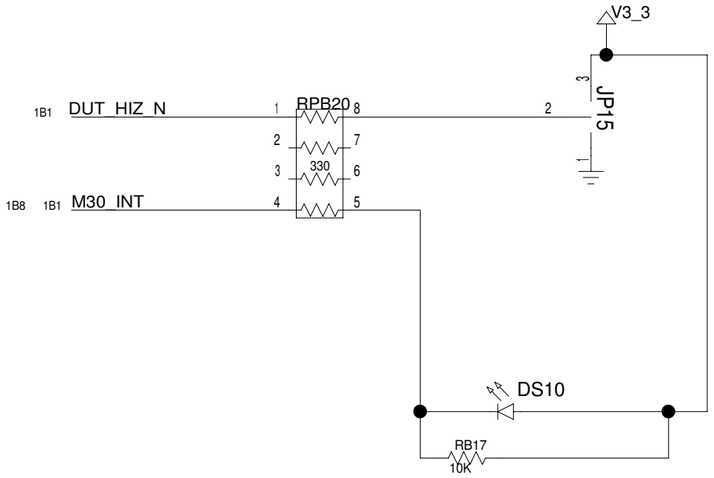

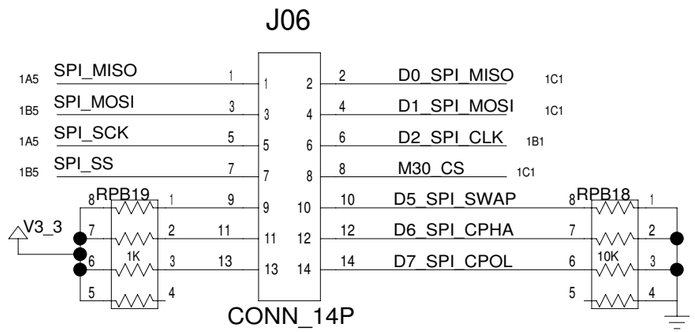

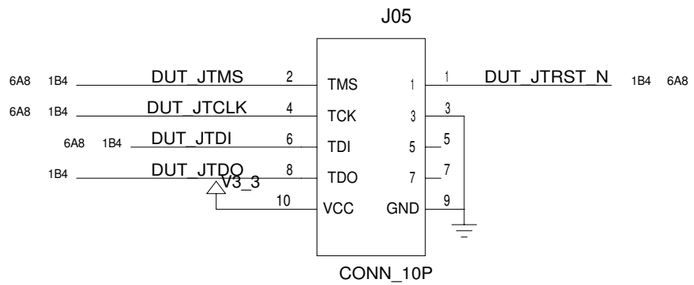

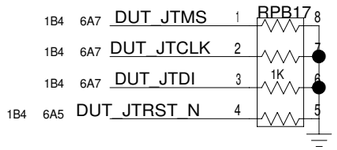

TITLE: DS33M30DK02A0 BIAS+CONFIG. P.6	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 6/8(BLOCK) 6/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

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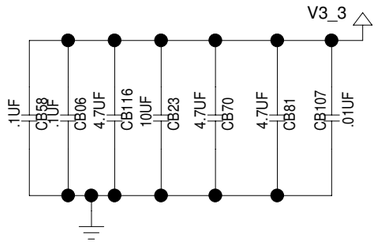

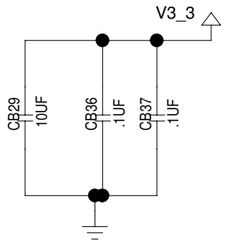

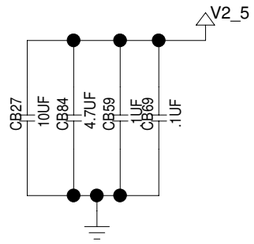

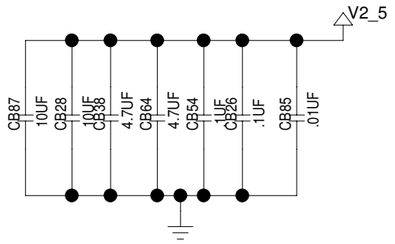

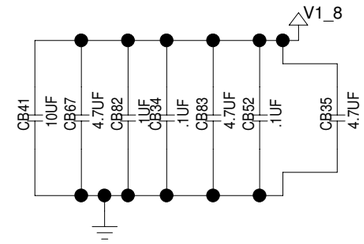

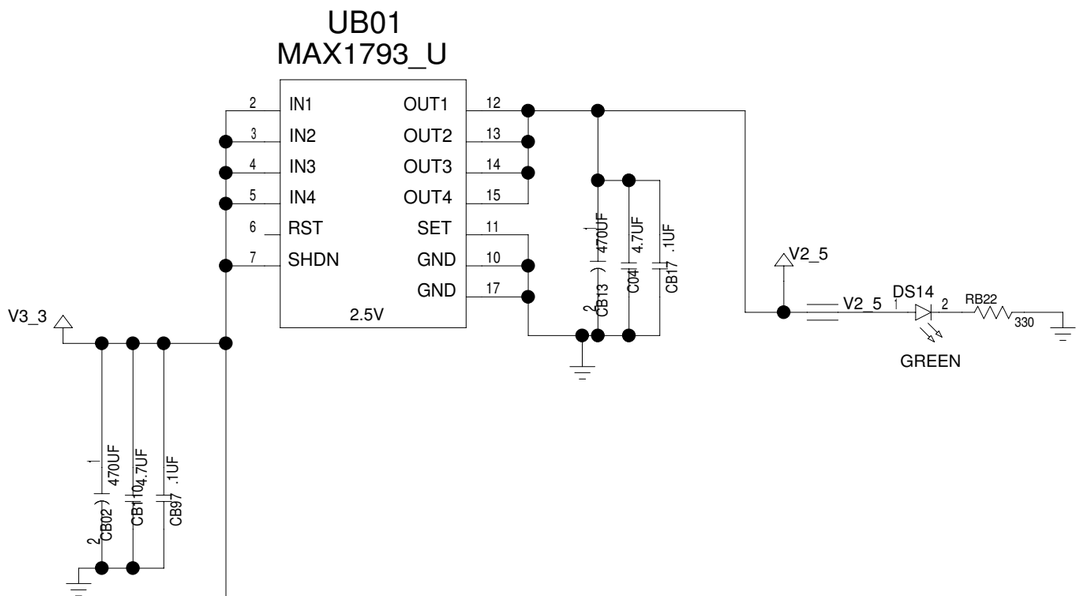

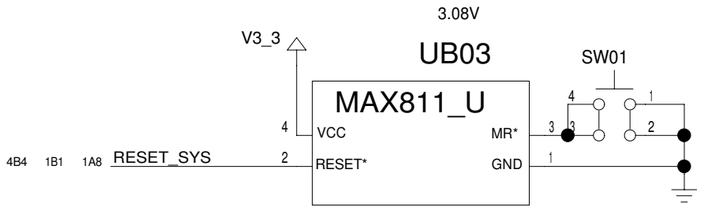

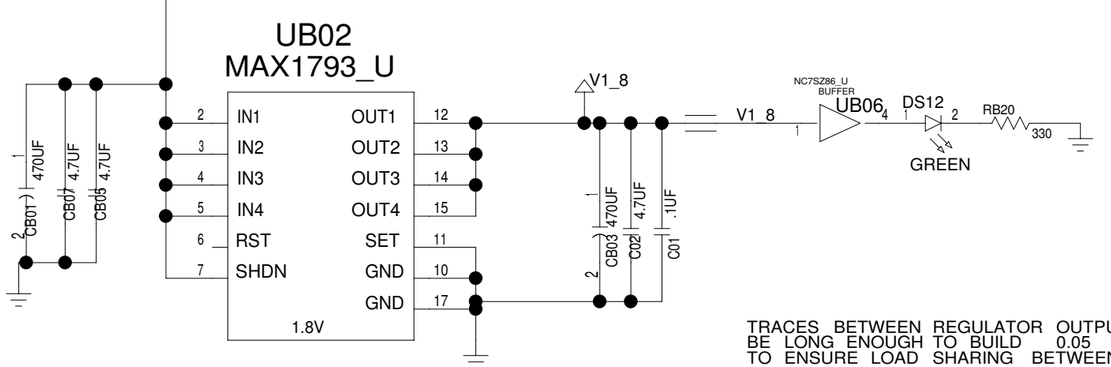

TRACES BETWEEN REGULATOR OUTPUT AND V2.5 SHOULD BE LONG ENOUGH TO BUILD 0.05 OHM OF RESISTANCE TO ENSURE LOAD SHARING BETWEEN THE 2.5V 1% REGULATORS TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

TITLE: DS33M30DK02A0 POWER. P.7-8	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 7/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

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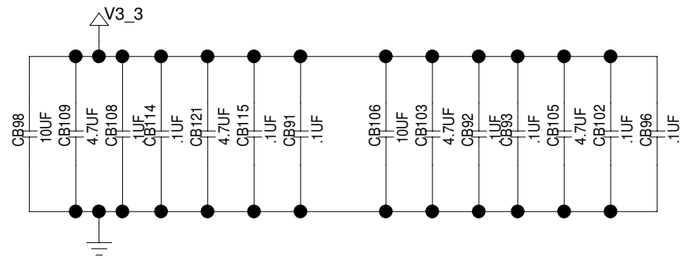

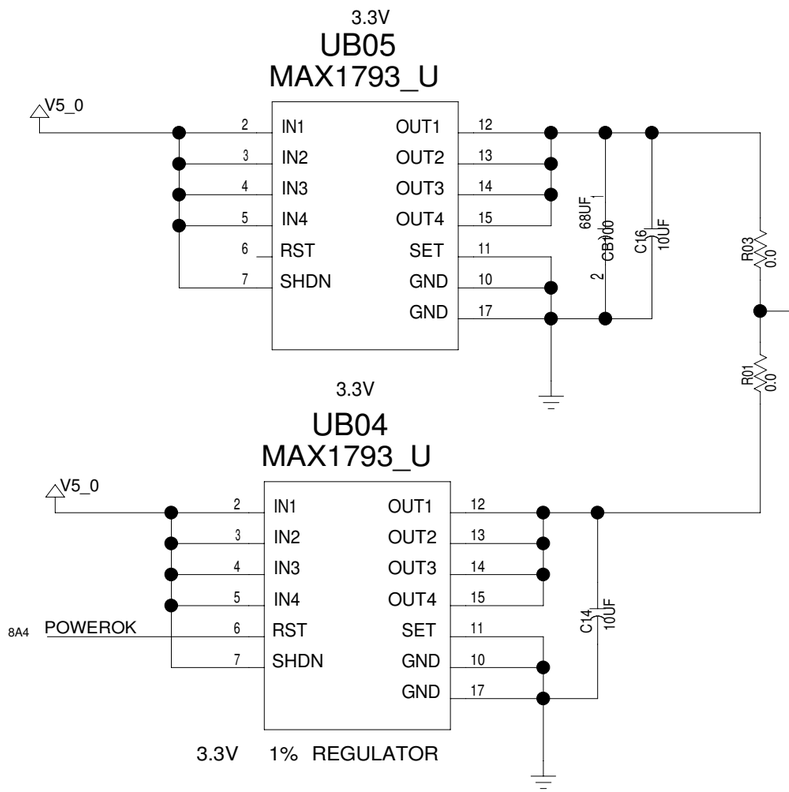

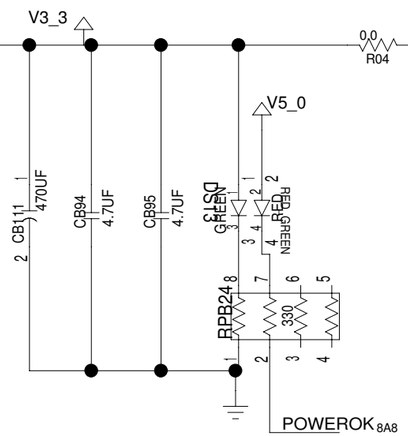

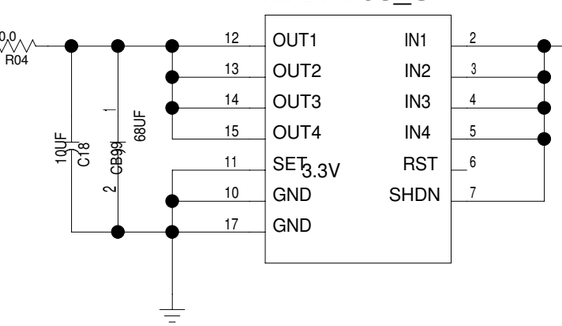

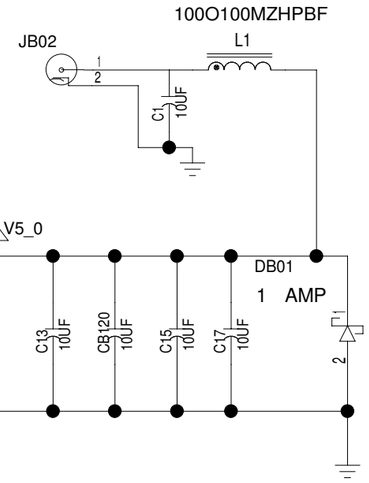

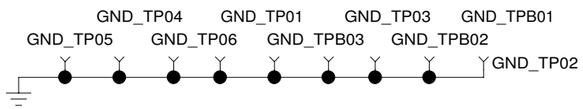

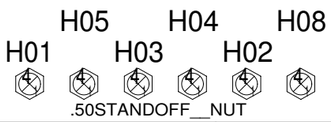

TITLE: DS33M30DK02A0 POWER. P.7-8	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 8/8(BLOCK) 8/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

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U05 TIM_16H_8L

MMC2107 CONTROL

U05

MMC2107 PORT

DS08

BEGINNING OF PROCESSOR HIERARCHY BLOCK

TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 1/3(BLOCK) 9/14(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _rc_top_dn_\

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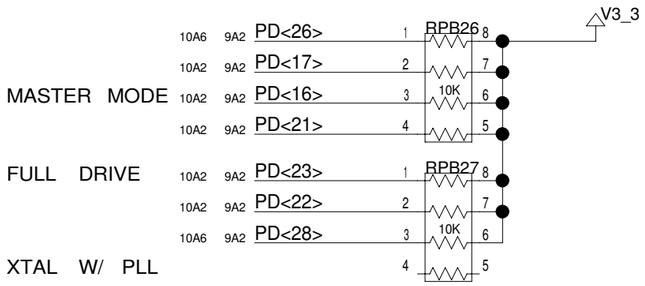
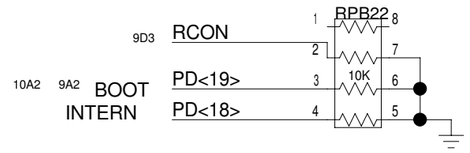
RESET CONFIGURATION

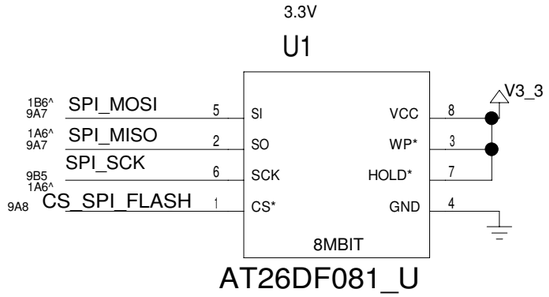
MASTER MODE

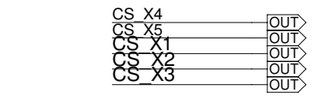
FULL DRIVE

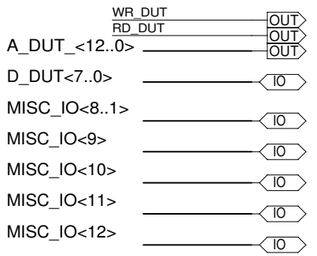
XTAL W/ PLL

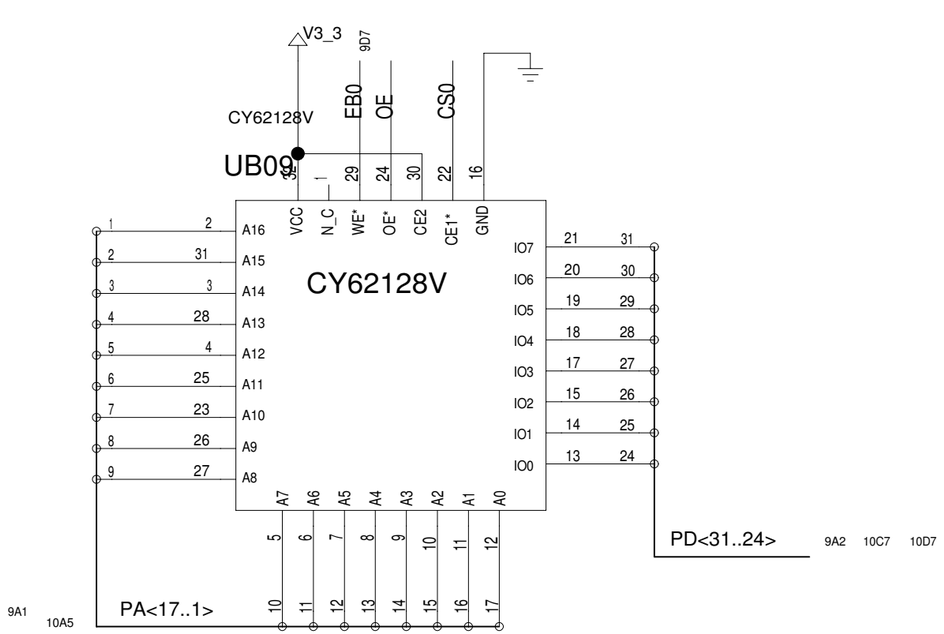


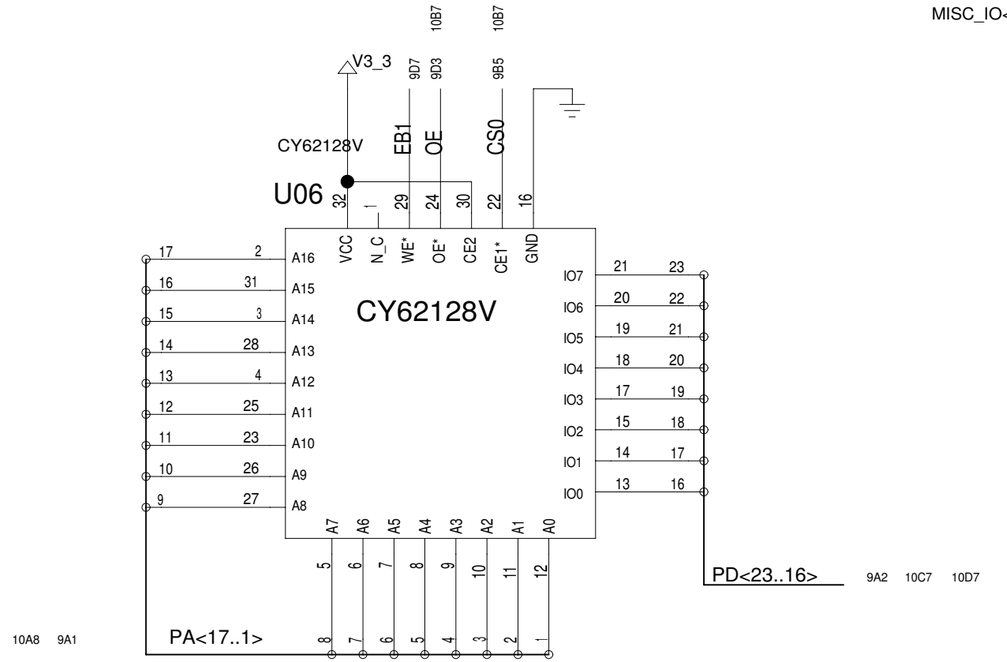












TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 2/3(BLOCK) 10/14(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _rc_top_dn_\

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XB01
8.0MHZ
OSC_MCU 9A6
R02
1.0M
PLACE PADS FOR CAP
BUT DO NOT POPULATE
XTAL 9A7

DS11
GREEN
KIT_STATUS 9A7
RB18
330

J07
CON14P
9D6 ONCE_TDI
9D6 2107_TDO
9A6 ONCE_TCLK
RESET_IN
1A7^ 10D1 9B5 V3_3
ALIGN KEY
ONCE_TMS 9A6
ONCE_DE_B 9B5
ONCE_TRST_B 9A6
V5_0
FLASH_VPP 9D3
JB01
RPB29
10K
V3_3

USB
J09
VDD
DAT-
DAT+
GND
RB21
CB113
CB112
.1UF
VDD IS A (UNUSED) OUTPUT ON CP2101 CHIP
U07
CP2101
USBDM
USBDP
VBUS
RST*
REGIN
SUSPEND_LOW*
SUSPEND_HIGH
11B2 SSPL
CB117 1UF
GND NC1 NC2 NC3 NC4 NC5 NC6
NC7 NC8 NC9 NC10 NC11
TXD 26 USB_DOUT 11A5
RXD 25 USB_DIN 11B5
RTS* CTS* DTR* DSR* DCD* RI*
RPB23
RPB25
10K
SSPL
DTR AND RTS USE RPACK CONNECTION AS TESTPOINTS

UB08
MAX3233E
R2OUT R2IN
INVALID* T2OUT
T2IN GND
T1IN V-
FORCEON C2-
R1OUT C2+
T1OUT C1-
R1IN C1+
VCC V+2
FORCEOFF* V+1
11A5 UART_DIGIN
11A5 UART_DIGOUT
11A8 PRT1_OUT
11A8 PRT1_IN
V3_3

9B8 PROCSER_OUT
JMP_3
JP18
UART_DIGIN 11B8
USB_DIN 11B2
9B8 PROCSER_IN
JMP_3
JP19
UART_DIGOUT 11B8
USB_DOUT 11B2

J08
CONN_DB9P
PRT1_OUT 11B8
PRT1_IN 11B8
RPB28
10K
V3_3

TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 3/3(BLOCK) 11/14(TOTAL)

BLOCK_NAME: motprocrescard_dn. PARENT_BLOCK: \ rc_top_dn \

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V3_3 I67 V3_3

I68 GND

J04
SMT
SFM-125-L2-S-D-LC
NA
I78

4B3^ 12A8 RESET_B 1
4C3^ 12D1 PT1_TXD<3..0>
4C3^ 12D1 PT1_TX_EN 15
4C3^ 12D1 PT1_TX_CLK 17
4B1^ 12A4 GMII_CLKFROM_MAC 21
4B1^ 12A4 GMII_TX_ER_ 23
4B1^ 12A4 GMII_CLKTOMAC_BUF 25
4B3^ IO OSC25M 27
4B3^ 12A8 LAN_CLK 29
4C3^ 12C1 PT2_TXD<3..0>
12C1 PT2_TX_EN 43
12C1 PT2_TX_CLK 45
4B3^ 12A8 MDIO 47
4B3^ 12A8 MDC 49

2 PT1_RXD<3..0> 12C1 4D3^
V1_8
12 PT1_RX_CRS 12D1 4D3^
14 PT1_RXDV 12C1 4D3^
16 V3_3
18 PT1_RX_CLK 12D1 4D3^
20 PT1_COL_DET 12D1 4D3^
22 PT1_RX_ERR 12D1 4C3^
24
26 PHY_INT 12A8 4B3^
28 SPARE 12A7
30 PT2_RXD<3..0> 12B1 4C3^
32
34
36
38
40 PT2_RX_CRS 12C1
42 PT2_RXDV 12C1
44 V2_5
46 PT2_RX_CLK 12C1
48 PT2_COL_DET 12C1
50 PT2_RX_ERR 12C1

PT1_TXD<3..0> IO
PT1_TX_EN IO
PT1_TX_CLK IO
PT1_RX_CLK IO
PT1_COL_DET IO
PT1_RX_ERR IO
PT1_RX_CRS IO
PT1_RXDV IO
PT1_RXD<3..0> IO

PT2_TXD<3..0> IO
PT2_TX_EN IO
PT2_TX_CLK IO
PT2_RX_CLK IO
PT2_COL_DET IO
PT2_RX_ERR IO
PT2_RX_CRS IO
PT2_RXDV IO
PT2_RXD<3..0> IO

CONNECTORS FOR LAN MOTHERBOARD TO RESOURCE CARD

LAN_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO

12B4 SPARE IO

GMII_CLKFROM_MAC IO 12B6 4B1^
GMII_TX_ER_ IO 12B6 4B1^
GMII_CLKTOMAC_BUF IO 12B6 4B1^

TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 12/14(TOTAL)

BLOCK NAME: _phy_imbus_mb_dn. PARENT BLOCK: _rc_top_dn_\

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<TXT_GIGABITPHYMOTHERBRDCONNECTOR>. SCHEMATIC ON <PGNM_GIGABITPHYMOTHERBRDCONNECTOR>

PLACE 9.76K RES CLOSE TO BG_REF

RESET_B — RB15 9.76K — BG_REF

V3_3 V1_8 V2_5 V1_8

U02

DP83865_U

OUTPUT
COL PIN39
CRS PIN40
RXER PIN41
RXDV PIN44
RXD[0:7] [PIN56:PIN45]
RXCLK PIN57
TXCLK PIN60
CLKTOMAC PIN85
CLKOUT PIN87

INPUT
TXERR PIN61
TXEN PIN62
TXD[0:7] [PIN76:PIN65]
GTXCLK PIN79
MDC PIN81
CLKIN PIN86

RB06 2.0K — BP01 30

RX_CRS_BUF, COL_DET_BUF, TX_CLK_BUF

TXD<7..0> — RP06, RP03 30

RXD<7..0>

TX_EN, GMII_CLKFROM_MAC, TX_ER_, RX_CLK_BUF, RX_ER_BUF, RXDV_BUF

MDC, MDIO, INTERRUPT*, MDIA_P/N, MDIB_P/N, MDIC_P/N, MDID_P/N

RPB10, RPB09 — 0603_2PCT_50 — PLACE MDI RESISTORS CLOSE TO PHY — MAINTAIN 50OHM STIPLINE TO V2_5PHY

PHYOSC25M, LAN_CLK, MDC, MDIO, RESET_B, PHY_INT, SPARE<4..1>

GMII_CLKFROM_MAC, TX_ER_, CLKTOMAC_TESTPNT, CLKTOMAC, TXD<7..0>, TX_EN, TX_CLK, RX_CLK, COL_DET, RX_ERR, RX_CRS, RXDV, RXD<7..0>

RP07 — RX_CLK_BUF, TX_CLK_BUF

RP08 — CLKTOMAC_BUF, CLKOUT_BUF — TP01

RP02 — COL_DET_BUF, RX_CRS_BUF, RX_ERR_BUF, RXDV_BUF

CLK_IN, CLK_OUT, CLK_TO_MAC, NON_IEEE_STRAP, MAN_MDIX_STRAP/TX_TCLK, ACTIVITY_LED/SPEED0_STRAP, LINK10_LED/SPEED1_STRAP, LINK100_LED/DUPLEX_STRAP, LINK1000_LED/AN_EN_STRAP, DUPLEX_LED/PHYADDR<0>_STRAP, PHYADDR<1>_STRAP, PHYADDR<2>_STRAP, PHYADDR<3>_STRAP, PHYADDR<4>_STRAP, MULTI_EN_STRAP/TX_TRIGGER, MDIX_EN_STRAP, MAC_CLK_EN_STRAP/TX_SYN_CLK

RPB08 — 1K

VSS<1..35> — 128

V3_3 — V3_3, GND

RPB11 — 1K — TX_ER_

RB01 330 — DS04 GREEN — RB07 2.0K — A0_DUPLEX

TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 13/14(TOTAL)

BLOCK NAME: _phy_dp83865bvh_dn. PARENT BLOCK: _rc_top_dn_\

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V3_3
JMP_3
JP04
RPB05 8
2.2K
L1000OB
GREEN_GREEN
DS06

V3_3
JMP_3
JP05
RPB05 7
2.2K
L100OB
GREEN_GREEN
DS07

V3_3
JMP_3
JP06
RPB05
2.2K
L10OB
GREEN_GREEN
DS09

V3_3
JMP_3
JP03
RPB05 5
2.2K
LACTOB
GREEN_GREEN
DS05

RPB07
1 LINK1000LED_ANEN 13B3
2 LINK100LED_DUPLEX 13B3
3 330 LINK10LED_SPEED1 13B3
4 ACTIVITYLED_SPEED0 13B3

CHECK THAT 2.2K RES USE THE SAME RPACK
STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET

V3_3
RB16
2.0K
NON_IEEE_STRAP 13B3

V3_3
JP09
JP08
RPB14
1 MAN_MDIX_STRAP__TX_TCLK 13B3
2 MULTI_EN_STRAP__TX_TRIGGER 13A3
3 2.2K MDIX_EN_STRAP 13A3
4 MAC_CLK_EN_STRAP__TX_SYN_CLK 13A3

V3_3
4B4^ 13D6 13D2 RESET_B RPB06
4B4^ 13D2 13C3 MDIO
4B4^ 13D2 13C3 PHY_INT
2.2K

CAPS FOR DECOUPLE OF MX.+-
V2_5
CB65 .01UF
CB09 .01UF
CB10 .01UF
CB08 .01UF
CB42 4.7UF
CB78 4.7UF

J03
CMR CHOKES
13C3 MDIA_P 1 TD0+
13C3 MDIA_N 2 TD0-
13C3 MDIB_P 3 TD1+
13C3 MDIB_N 6 TD1-
13C3 MDIC_P 4 TD2+
13B3 MDIC_N 5 TD2-
13B3 MDID_P 7 TD3+
13B3 MDID_N 8 TD3-
0.01 UF X4
750 X4
J1 MX0+
J2 MX0-
J3 MX1+
J6 MX1-
J4 MX2+
J5 MX2-
J7 MX3+
J8 MX3-
V2_5
9 VCC
10 GND
1000PF, 2KV
11 SH1
12 SH2
CONN_HFJ11_1G02E_U

V3_3
CB62 4.7UF
C07 4.7UF
CB53 4.7UF
CB73 4.7UF
CB49 4.7UF
CB77 4.7UF
CB55 4.7UF
CB12 .1UF
CB74 .1UF
C06 .1UF
C09 .1UF
C03 .1UF
C05 .1UF
C08 .01UF
C12 .01UF

V1_8
CB30 4.7UF
CB61 4.7UF
CB89 4.7UF
CB51 4.7UF
CB68 4.7UF
CB76 4.7UF
CB50 4.7UF
CB47 4.7UF
CB11 .1UF
CB45 .1UF
CB20 .1UF
CB24 .1UF
CB66 .1UF
C11 .1UF
CB75 .1UF
CB71 .1UF
CB48 .1UF
CB14 .01UF

V2_5
CB33 4.7UF
CB32 4.7UF
CB80 4.7UF
CB79 4.7UF
CB88 .1UF
CB39 .1UF
CB04 .01UF

TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 14/14(TOTAL)

BLOCK NAME: _phy_dp83865bvh_dn. PARENT BLOCK: _rc_top_dn_\