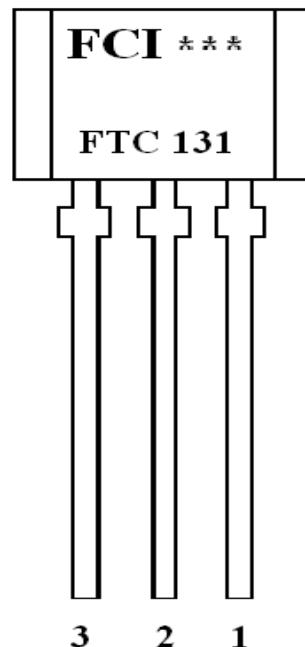
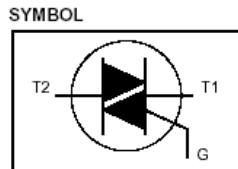


**Description:**

Glasspassivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to micro controllers, logic integrated circuits and other low power gate trigger circuits.

**FTC131**
**V<sub>DRM</sub> 500V/600 V**
**I<sub>T(RMS)</sub> 1A**
**I<sub>TSM</sub> 16A**

**Pinging :TO-92: DESCRIPTION**
**Pin1: Main Terminal 2**
**Pin 2: G**
**Pin 3: Main Terminal 3**
**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V <sub>DRM</sub>	Repetitive peak off-state voltages		-	-500 500	-600 600	V
I <sub>T(RMS)</sub> I <sub>TSM</sub>	RMS on-state current Non-repetitive peak on-state current	full sine wave; T <sub>lead</sub> ≤ 51 °C full sine wave; T <sub>j</sub> = 25 °C prior to surge	-	1		A
I <sup>2</sup> t dI <sub>T</sub> /dt	I <sup>2</sup> t for fusing Repetitive rate of rise of on-state current after triggering	t = 20 ms t = 16.7 ms t = 10 ms I <sub>TM</sub> = 1.5 A; I <sub>G</sub> = 0.2 A; dI <sub>G</sub> /dt = 0.2 A/μs	- - - T2+ G+ T2+ G- T2- G- T2- G+	16 17.6 1.28 50 50 50 10		A A A <sup>2</sup> s A/μs A/μs A/μs A/μs
I <sub>GM</sub> V <sub>GM</sub> P <sub>GM</sub> P <sub>G(AV)</sub> T <sub>stg</sub> T <sub>j</sub>	Peak gate current Peak gate voltage Peak gate power Average gate power Storage temperature Operating junction temperature	over any 20 ms period	- - - - -40 -	2 5 5 0.5 150 125		A V W W °C °C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/μs.



# 1A 500V/600V BIDIRECTIONAL TRIACS

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-lead}}$	Thermal resistance junction to lead	full cycle	-	-	60	K/W
$R_{th\ j\text{-a}}$	Thermal resistance junction to ambient	half cycle pcb mounted; lead length = 4mm	-	150	80	K/W

## STATIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{GT}$	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.4	3	mA
		$T_2+ G+$	-	1.3	3	mA
		$T_2+ G-$	-	1.4	3	mA
		$T_2- G-$	-	3.8	7	mA
$I_L$	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	1.2	5	mA
		$T_2+ G+$	-	4.0	8	mA
		$T_2+ G-$	-	1.0	5	mA
		$T_2- G-$	-	2.5	8	mA
$I_H$ $V_T$ $V_{GT}$	Holding current On-state voltage Gate trigger voltage	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	1.3	5	mA
		$I_T = 2.0\text{ A}$	-	1.2	1.5	V
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.7	1.5	V
$I_D$	Off-state leakage current	$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125^\circ\text{C}$	0.2	0.3	-	V
		$V_D = V_{DRM(max)}; T_j = 125^\circ\text{C}$	-	0.1	0.5	mA

## DYNAMIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$dV_D/dt$	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125^\circ\text{C};$ exponential waveform; $R_{GK} = 1\text{ k}\Omega$	5	15	-	V/ $\mu\text{s}$
$t_{gt}$	Gate controlled turn-on time	$I_{TM} = 1.5\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$



# 1A 500V/600V BIDIRECTIONAL TRIACS

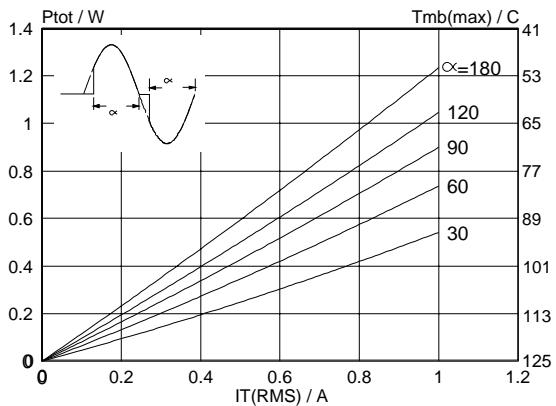


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus rms on-state current,  $IT_{(RMS)}$ , where  $\alpha$  = conduction angle.

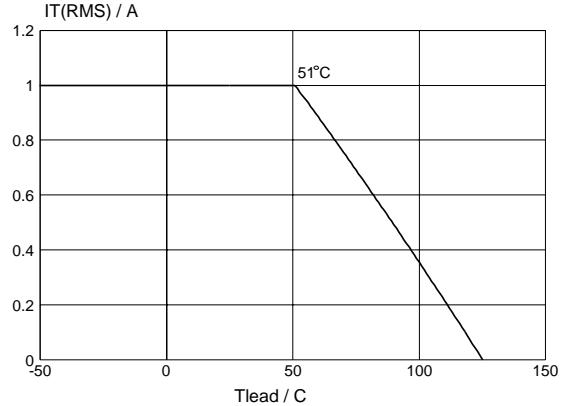


Fig.4. Maximum permissible rms current  $IT_{(RMS)}$ , versus lead temperature  $T_{lead}$ .

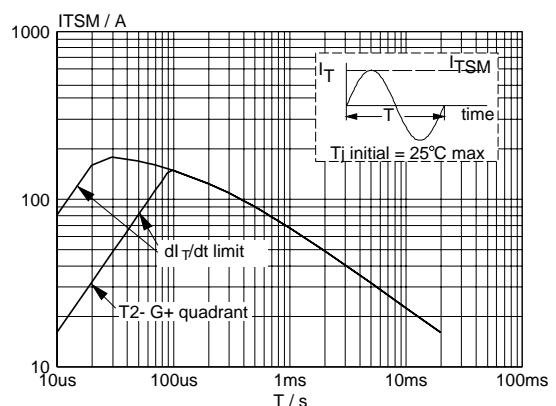


Fig.2. Maximum permissible non-repetitive peak on-state current  $IT_{SM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 20ms$ .

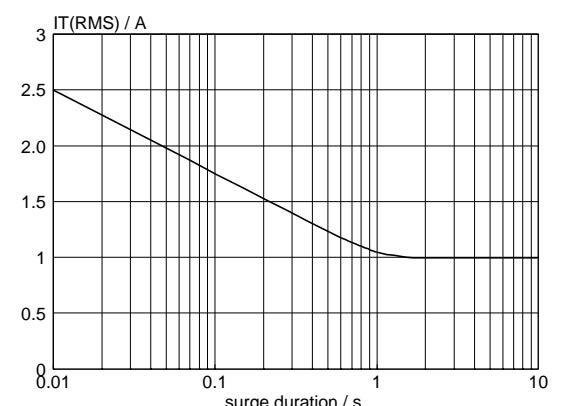


Fig.5. Maximum permissible repetitive rms on-state current  $IT_{(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50$  Hz;  $T_{lead} \leq 51^\circ C$ .

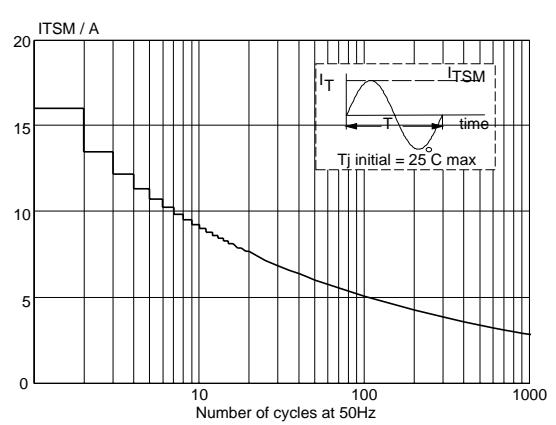


Fig.3. Maximum permissible non-repetitive peak on-state current  $IT_{SM}$ , versus number of cycles, for sinusoidal currents,  $f = 50$  Hz.

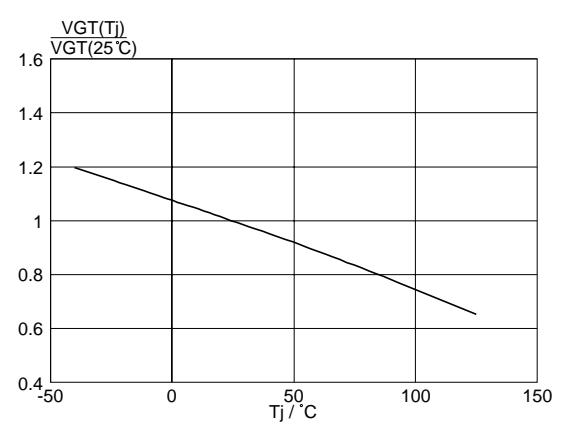


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j)/V_{GT}(25^\circ C)$ , versus junction temperature  $T_j$ .



# 1A 500V/600V BIDIRECTIONAL TRIACS

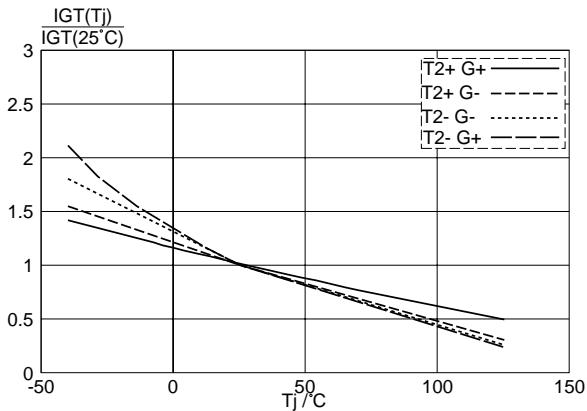


Fig.7. Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ C)$ , versus junction temperature  $T_j$ .

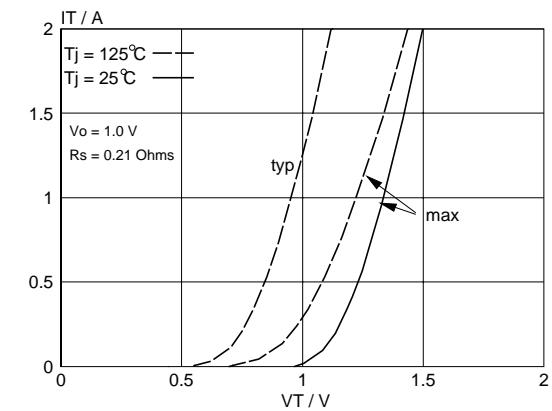


Fig.10. Typical and maximum on-state characteristic.

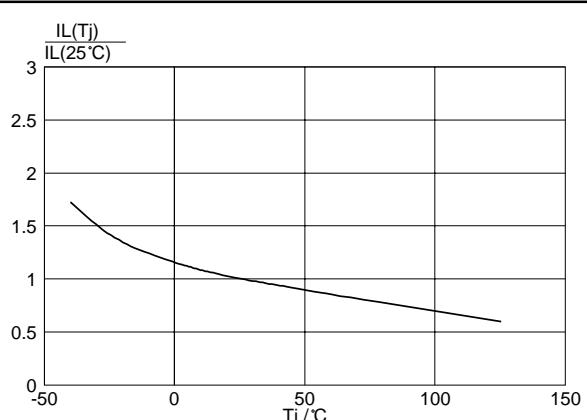


Fig.8. Normalised latching current  $I_L(T_j)/I_L(25^\circ C)$ , versus junction temperature  $T_j$ .

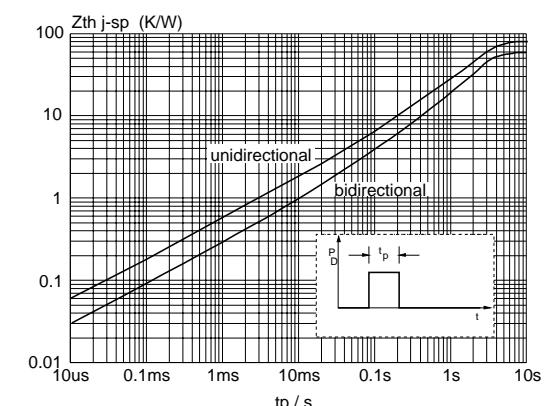


Fig.11. Transient thermal impedance  $Z_{th,j-sp}$ , versus pulse width  $t_p$ .

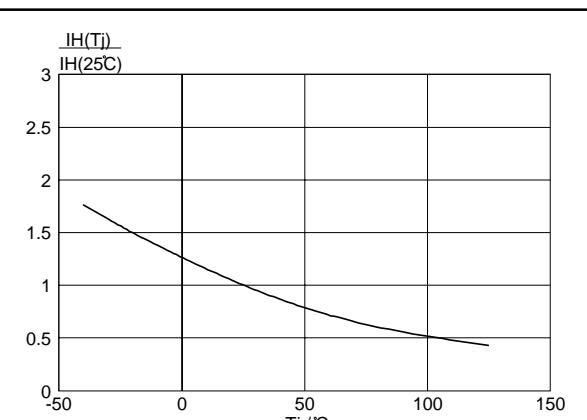


Fig.9. Normalised holding current  $I_H(T_j)/I_H(25^\circ C)$ , versus junction temperature  $T_j$ .

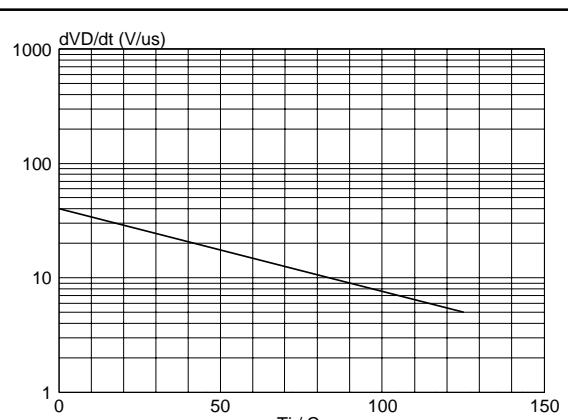


Fig.12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  versus junction temperature  $T_j$ .