GaN Hybrid Power Amplifier HT1919-30A

RFHIC

RoHS Comply

Product Features

- GaN on SiC HEMT
- In/Out Impedance Matching
- Surface Mount Hybrid Type
- Small Size & Mass
- High Efficiency
- Low Cost
- Custom design available

Applications

- RF Sub-Systems
- Base Station
- Repeater
- LTE system

Package Type : NP-1EL

Description

The HT1919-30A is designed for LTE Repeater & RF Sub-systems application frequencies from 1930 ~ 1995MHz
This amplifier uses GaN HEMT technology which performs high breakdown voltage, high efficiency. High In/Output impedance, High power density.

Electrical Specifications @ Vds =28V, Ta=25℃

PARAMETER	UNIT	MIN	TYP	MAX	CONDITION
Frequency Range	MHz	1930	-	1995	ZS = ZL = 50 ohm
Power Gain	dB	36	38	40	Amp : Idq1 = 110mA Idq2 = 130mA
Gain Flatness		-	0.7	2	
Input Return Loss		-	-10	-8	
Pout @ Average	dBm	-	37	-	
Pout @ Psat	dBm	44	45	-	Pulse Width=50us, 10%Duty
ACLR @ BW 10MHz LTE (PAPR 7.5dB)	dBc	-	-32	-28	Non DPD
		-	-53	-	With DPD
Drain Efficiency	%	25	26	-	Pout @ Average
Ids	mA	-	670	710	
Supply Voltage	V	-	-3.0	-2.0	Gate Bias (Vgs1 and Vgs2)
	V	27.5	28	-	Main Bias(Vds)

Caution

The drain voltage must be supplied to the device after the gate voltage is supplied
Turn on : Turn on the Gate Voltage supply and last turn On the Drain voltage supplies
Turn off : Turn off the Drain Voltage and last turn off the Gate voltage

Note

1. ACLR Measured Pout=37dBm @ fc± 10MHz / 9.015MHz
   LTE 10MHz 1FA PAPR=7.5dB @ 0.01% probability on CCDF, (DPD Engine: Optichron OP6180)
2. HT Series have internal DC blocking capacitors at the RF input and output ports

Mechanical Specifications

PARAMETER	UNIT	TYP	REMARK
Mass	g	2	-
Dimension	㎜	20.5 x 15 x 3.5	-

Absolute Maximum Ratings

PARAMETER	UNIT	RATING	SYMBOL
Gate-Source Voltage	V	-10 ~0	Vgs1 Vgs2
Drain-Source Voltage	V	50	Vds
Gate Current	mA	9.3	Ig
Operating Junction Temperature	°C	225	T_J
Operating Case Temperature	°C	-30 ~ 85	T_C
Storage Temperature	°C	-40 ~ 100	T_{STG}
***Maximum Input Level**	dBm	25	Pin

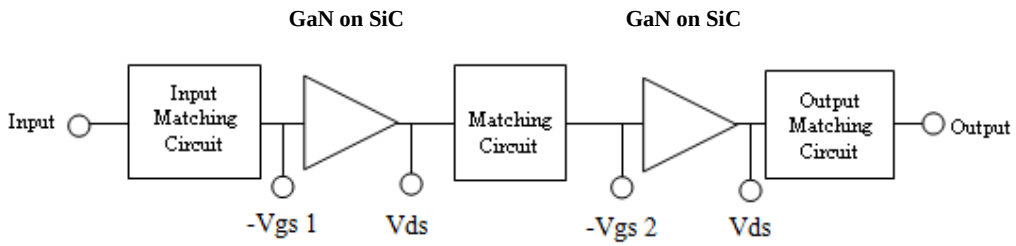
*** Test Condition :** Pulse Width=50us, 10%Duty

Operating Voltages & Input Level

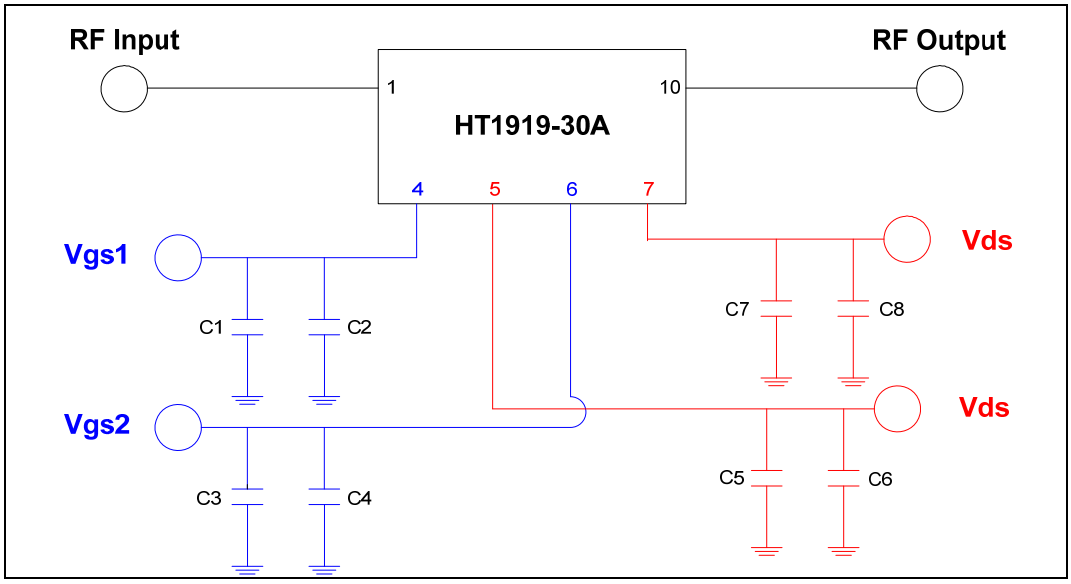
PARAMETER	UNIT	MIN	TYP	MAX	SYMBOL
Drain Voltage	V	-	28	-	Vds
Gate Voltage (on-stage)	V	-	-3	-2	Vgs 1
Gate Voltage (on-stage)	V	-	-3	-2	Vgs 2
Gate Voltage (off-stage)	V	-	-8	-	Vgs 1
Gate Voltage (off-stage)	V	-	-8	-	Vgs 2
Idq1	mA	105	110	115	Idq1
Idq2	mA	120	130	140	Idq2
***RF Input Level**	dBm	-	-	20	Pin

*** Test Condition :** Pulse Width=50us, 10%Duty

Block Diagram



Application Circuit



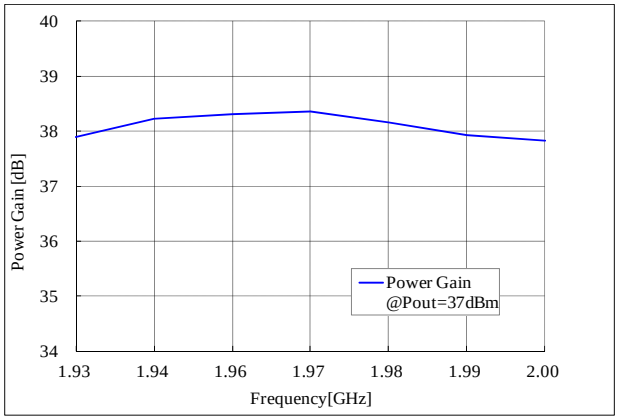
Part List

Location	Model No.	Spec.	Maker
C6, C8	TAJD106M050R	10uF / 50V	AVX
C1, C3	TAJA475M016R	4.7uF / 16V	AVX
C5, C7	GRM32ER72A225KA35L	2.2uF/100V	MURATA
C2, C4,	GRM1885C1H104BA01D	100nF	MURATA
Evaluation Board	RO4350B	2Layer, 30mil	ROGERS

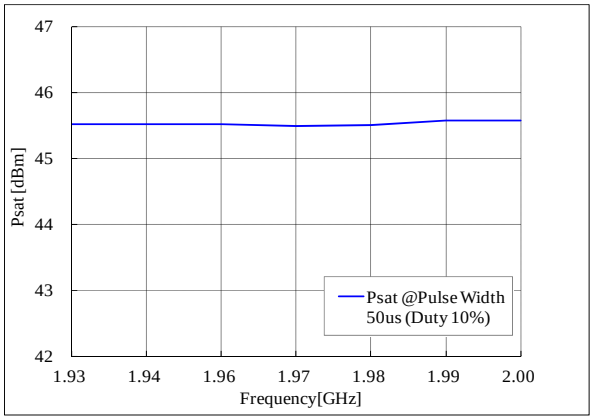
Performance Charts

*** Bias condition** @ Idq1= 110mA, Idq2= 130mA, Vds= 28V, Ta=25℃

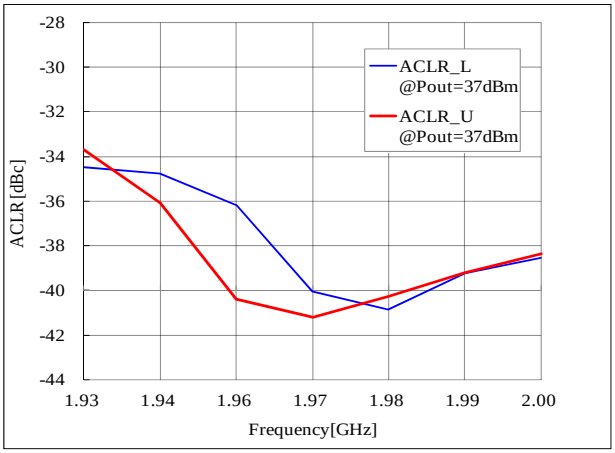
Power Gain vs. Frequency



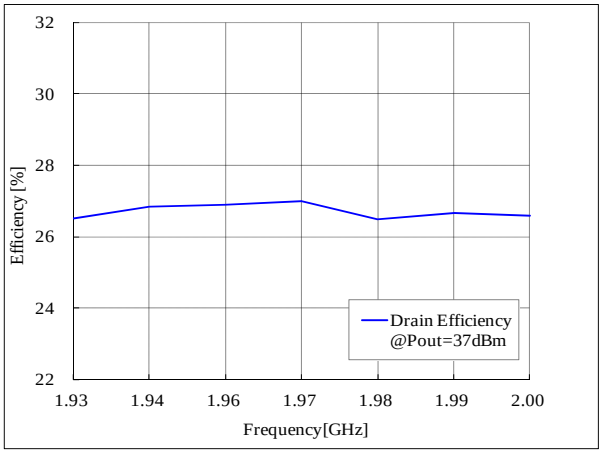
Psat vs. Frequency



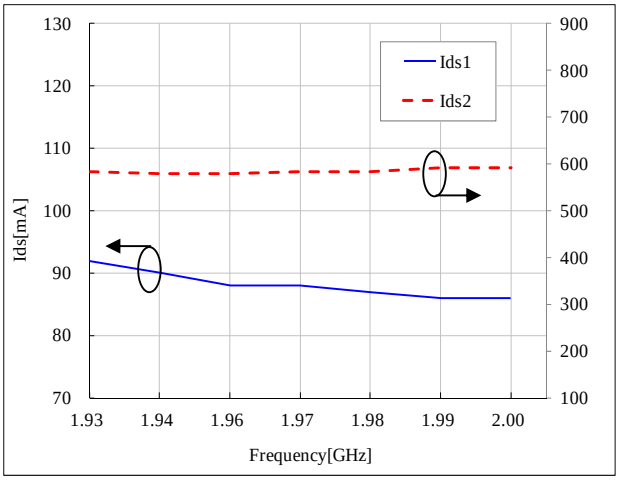
ACLR vs. Frequency



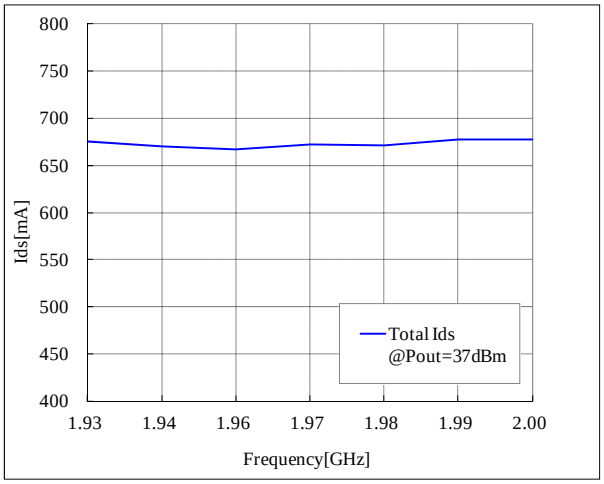
Drain Efficiency vs. Frequency



Ids1 vs Ids2 vs. Frequency



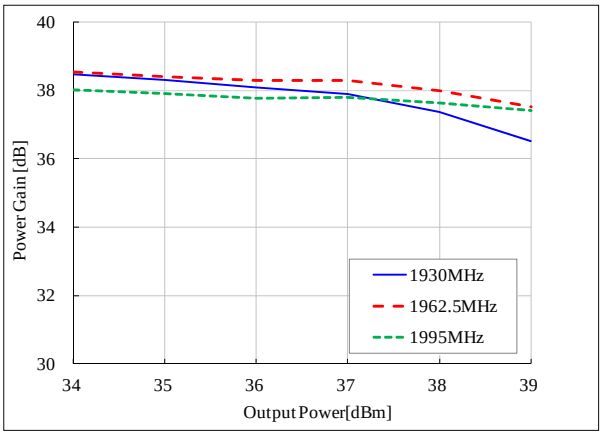
Total Ids vs. Frequency



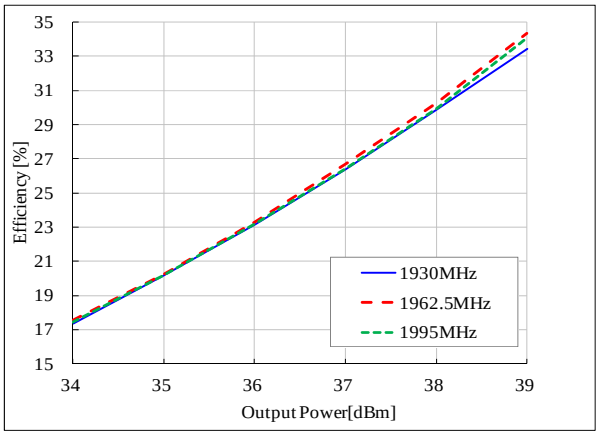
Performance Charts

*** Bias condition** @ Idq1= 110mA, Idq2= 130mA, Vds= 28V, Ta=25℃

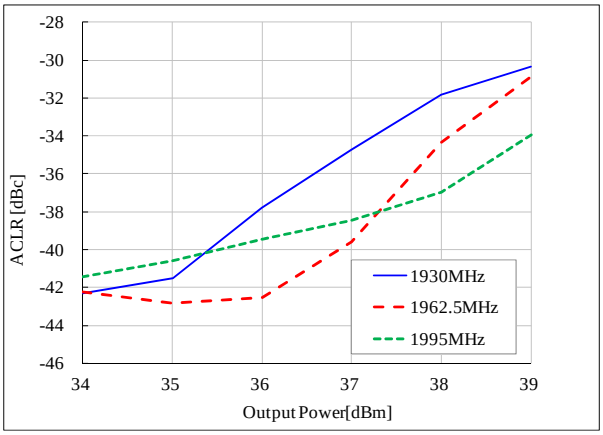
Power Gain vs. Output Power



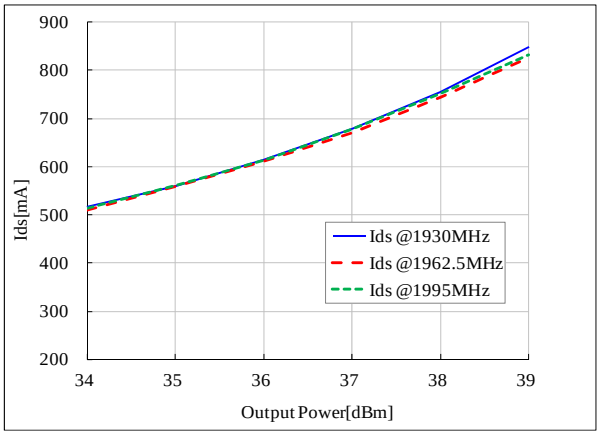
Drain Efficiency vs. Output Power



ACLR vs. Output Power



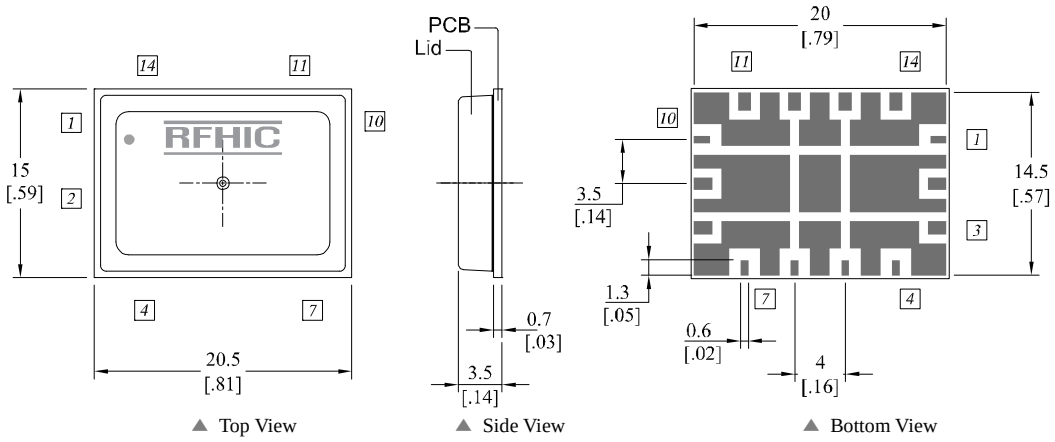
Ids vs. Output Power



*LTE 10MHz (PAPR=7.5dB) w/o DPD

Package Dimensions (Type: NP-1EL)

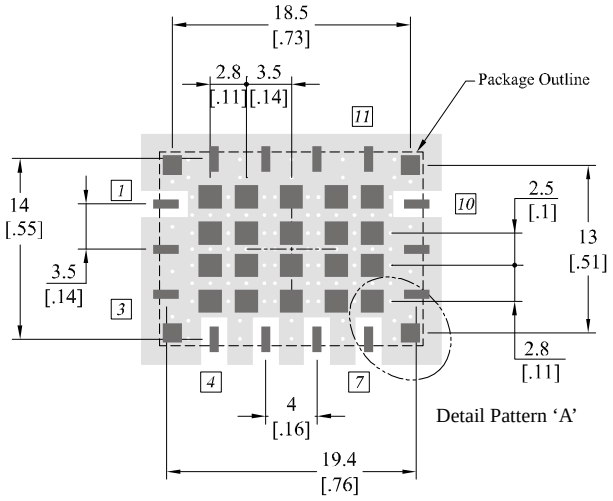
* Unit: mm[inch] | Tolerance: ±0.15[.006]



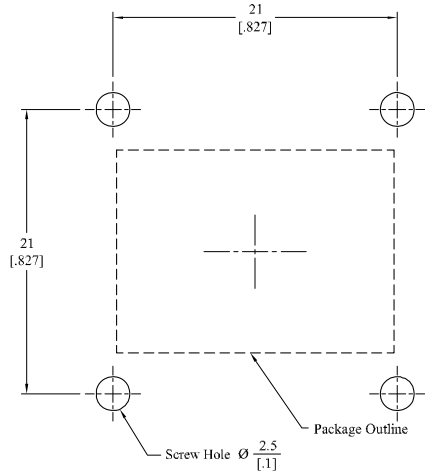
▲ Top View ▲ Side View ▲ Bottom View

Pin Description							
Pin No	**Function**	**Pin No**	**Function**	**Pin No**	**Function**	**Pin No**	**Function**
1	RF Input	4	Vgs1	8	GND	11	GND
2	GND	5	Vds	9	GND	12	GND
3	GND	6	Vgs2	10	RF Output	13	GND
-	-	7	Vds	-	-	14	GND

Recommended Pattern



Recommended Mounting Configuration



*** Mounting Configuration Notes**

1. For the proper performance of the device, Ground / Thermal via holes must be designed to remove heat.
2. To properly use heatsink, ensure the ground/thermal via hole region to contact the heatsink. We recommend the mounting screws be added near the heatsink to mount the board
3. In designing the necessary RF trace, width will depend upon the PCB material and construction.
4. Use 1 oz. Copper minimum thickness for the heatsink.
5. Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink
6. We recommend adding as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Precautions

This product is a Gallium Nitride Transistor.
The Gallium Nitride Transistor requires a Negative Voltage Bias which operates alongside a Positive Voltage Bias. These Biases are applied in accordance to the Sequence during Turn-On and Turn-Off.
The Pallet Amplifier does not have a built-in Bias Sequence Circuit. Therefore, users need to either apply positive voltages and negative voltages in the required sequence, or add an external Bias Circuit to this Amplifier.
The required sequence for power supply is as follows.

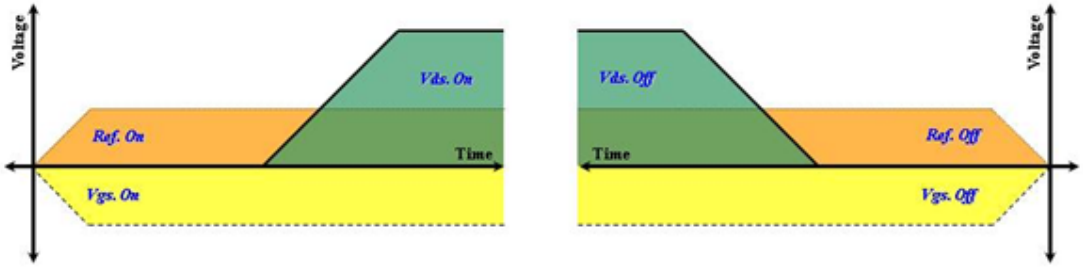
During Turn-On

1. Connect GND.
2. Apply Vgs1 and Vgs2.
3. Apply Vds.
4. Apply the RF Power.

During Turn-Off

1. Turn off RF power.
2. Turn off Vds, and then, turn off the Vgs1 and Vgs2.
3. Remove all connections.

Turn On **Turn Off**



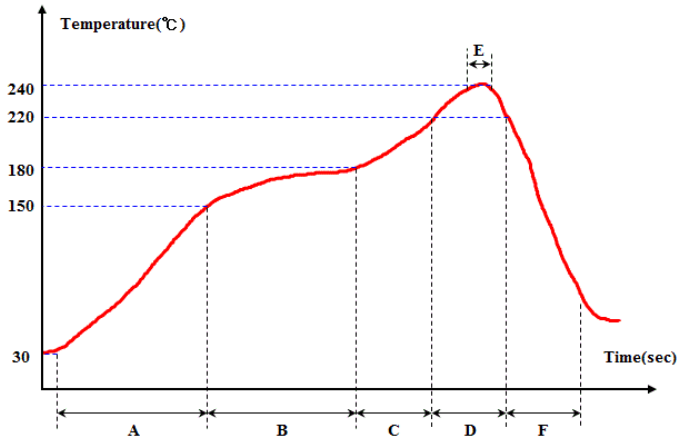
- Sequence Timing Diagram -

Reflow Profile

*** Reflow oven settings**

Zone	A	B	C	D	E	F
Temperature(°C)	30 ~ 150 ℃	150 ~ 180 ℃	180 ~ 220 ℃	220 ~ 220 ℃	235 ~ 240 ℃	2 ~ 6 ℃/ Sec Drop
Belt speed	55 ~ 115 sec	55 ~ 75 sec	30 ~ 50 sec	30 ~ 50 sec	5 ~ 10 sec	60 ~ 90 sec

*** Measured reflow profile**



Ordering Information

Part Number	Package Design
HT1919-30A	-R (Reel)
	-B (Bulk)
	-EVB (Evaluation Board)

Revision History

Part Number	Release Date	Version	Modification	Data Sheet Status
HT1919-30A	2013.12.20	1.0	Electrical Specification, Changed Package	-
HT1919-30A	2013.09.20	0.6	Changed Specification	Preliminary
HT1919-30A	2013.04.20	0.5	Changed Case Temperature	Preliminary