

# International **IR** Rectifier

PD - 95361A

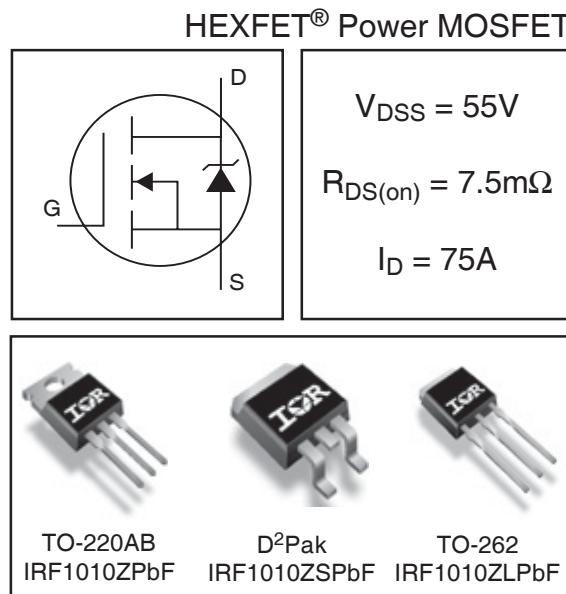
**IRF1010ZPbF**  
**IRF1010ZSPbF**  
**IRF1010ZLPbF**

## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

## Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	94	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	66	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	75	
I <sub>DM</sub>	Pulsed Drain Current ①	360	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.90	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub> (Thermally limited)	Single Pulse Avalanche Energy ②	130	mJ
E <sub>AS</sub> (Tested )	Single Pulse Avalanche Energy Tested Value ③	180	
I <sub>AR</sub>	Avalanche Current ④	See Fig.12a, 12b, 15, 16	A
E <sub>AR</sub>	Repetitive Avalanche Energy ⑤		mJ
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw ⑦	300 (1.6mm from case )	
		10 lbf•in (1.1N•m)	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	1.11	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat Greased Surface ⑧	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient ⑨	—	62	
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) ⑩	—	40	

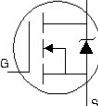
# IRF1010Z/S/LPbF

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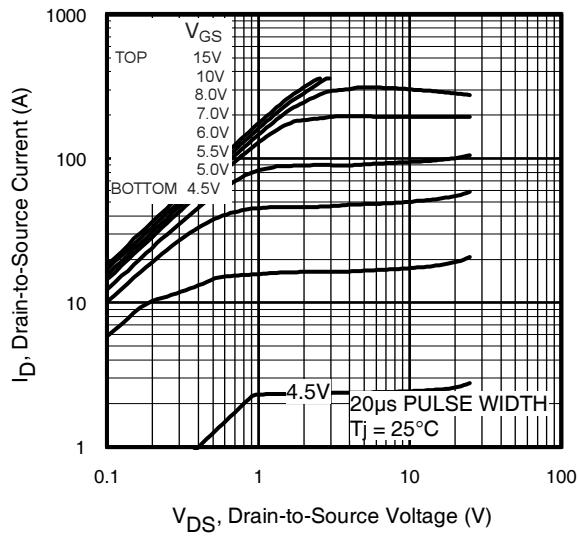
## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.049	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	5.8	7.5	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$ , $I_D = 75\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\mu\text{A}$
$g_{\text{fs}}$	Forward Transconductance	33	—	—	S	$V_{\text{DS}} = 25\text{V}$ , $I_D = 75\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{\text{DS}} = 55\text{V}$ , $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 55\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -20\text{V}$
$Q_g$	Total Gate Charge	—	63	95	nC	$I_D = 75\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	—	19	—		$V_{\text{DS}} = 44\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller") Charge	—	24	—		$V_{\text{GS}} = 10\text{V}$ ③
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	18	—	ns	$V_{\text{DD}} = 28\text{V}$
$t_r$	Rise Time	—	150	—		$I_D = 75\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	36	—		$R_G = 6.8 \Omega$
$t_f$	Fall Time	—	92	—		$V_{\text{GS}} = 10\text{V}$ ③
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{\text{iss}}$	Input Capacitance	—	2840	—		
$C_{\text{oss}}$	Output Capacitance	—	420	—	pF	$V_{\text{GS}} = 0\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	250	—		$V_{\text{DS}} = 25\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	1630	—		$f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	360	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 1.0\text{V}$ , $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	560	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 44\text{V}$ , $f = 1.0\text{MHz}$
						$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 0\text{V}$ to $44\text{V}$ ④

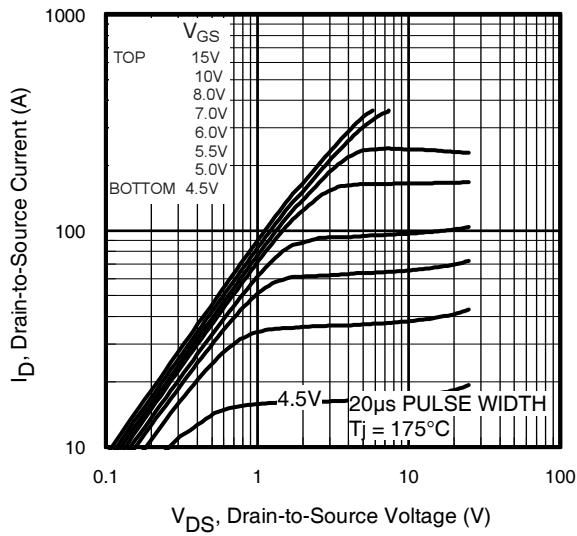
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
	Pulsed Source Current (Body Diode) ①	—	—	360		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$ , $I_S = 75\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ③
$t_{\text{rr}}$	Reverse Recovery Time	—	22	33	ns	$T_J = 25^\circ\text{C}$ , $I_F = 75\text{A}$ , $V_{\text{DD}} = 25\text{V}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	15	23	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ③
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $LS+LD$ )				

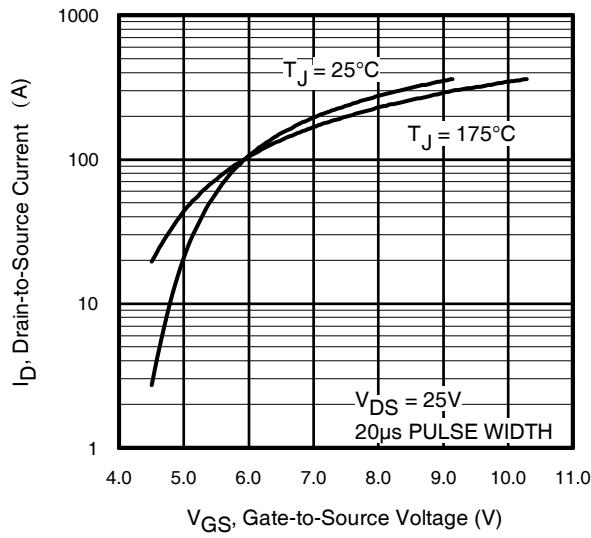
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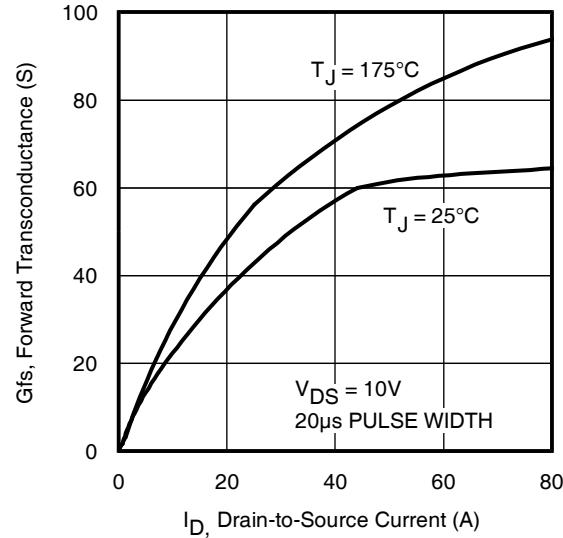
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



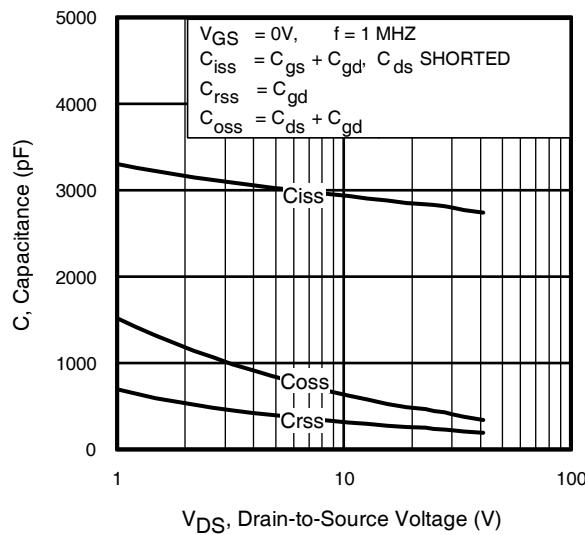
**Fig 3.** Typical Transfer Characteristics



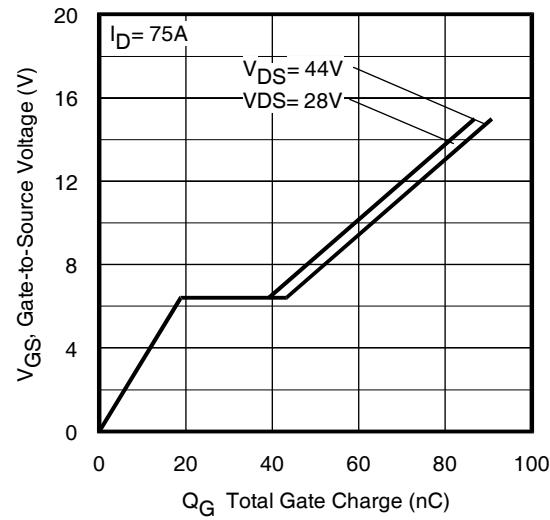
**Fig 4.** Typical Forward Transconductance Vs. Drain Current

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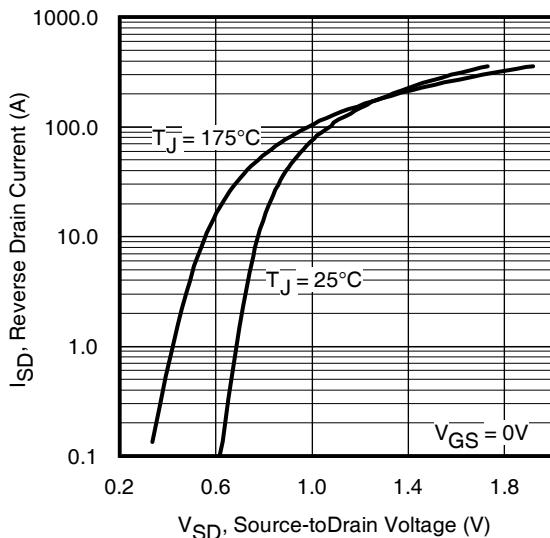
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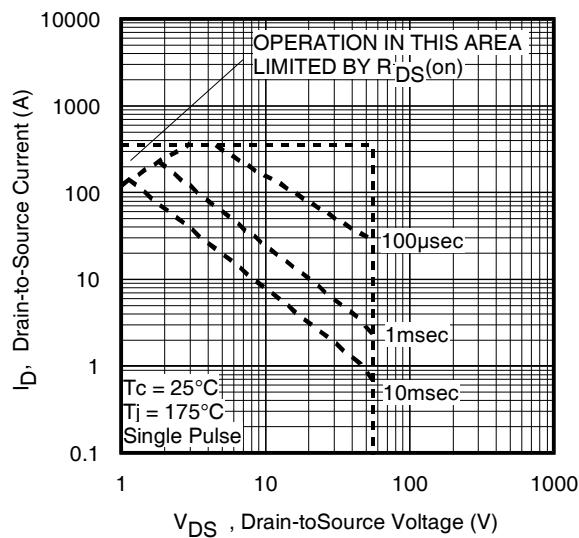
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



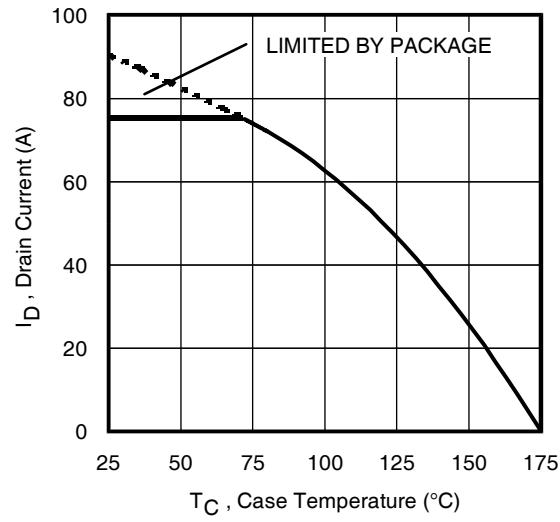
**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage



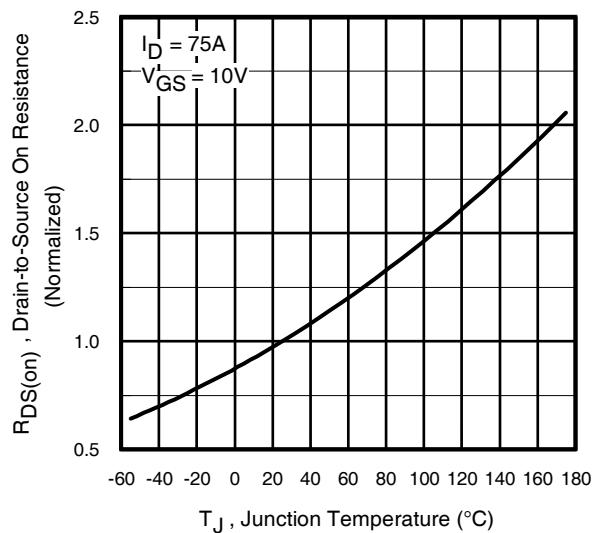
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



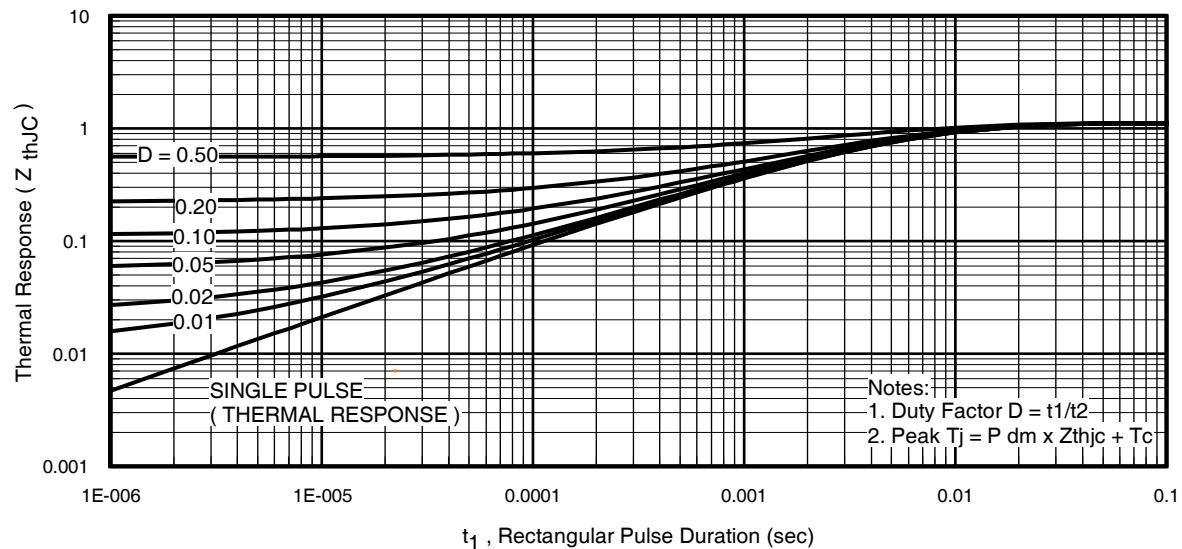
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs.  
Case Temperature



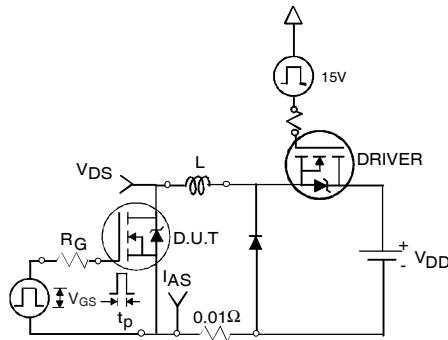
**Fig 10.** Normalized On-Resistance  
Vs. Temperature



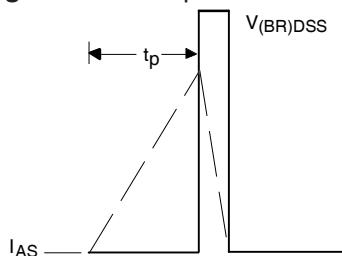
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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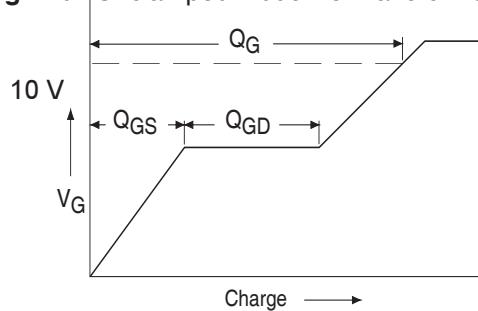
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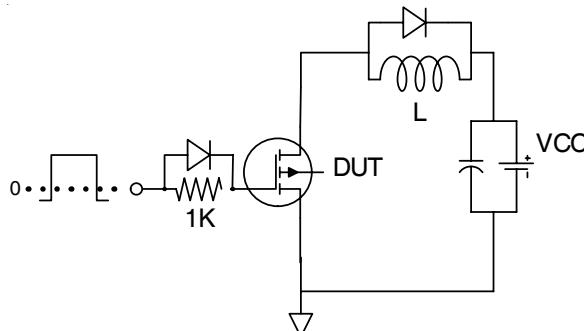
**Fig 12a.** Unclamped Inductive Test Circuit



**Fig 12b.** Unclamped Inductive Waveforms

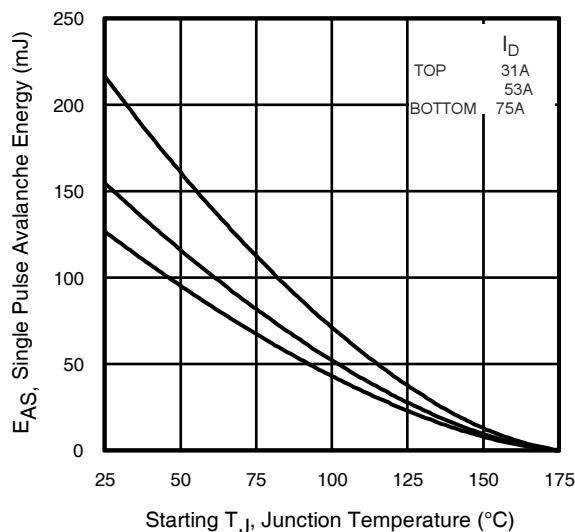


**Fig 13a.** Basic Gate Charge Waveform

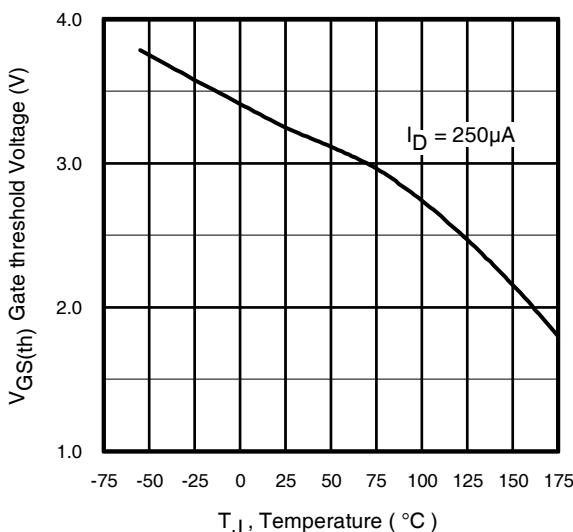


**Fig 13b.** Gate Charge Test Circuit

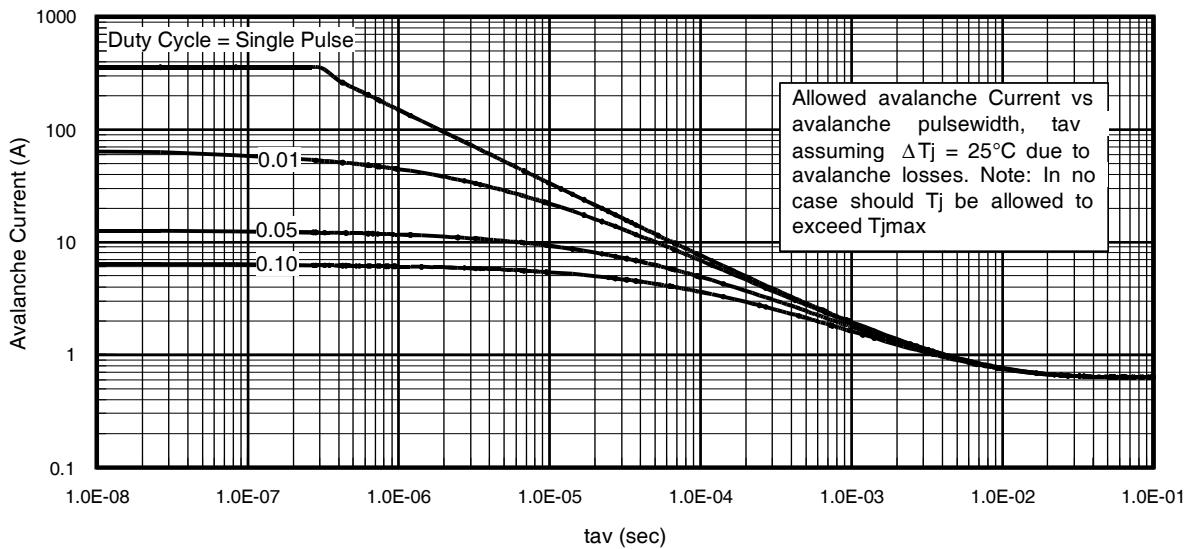
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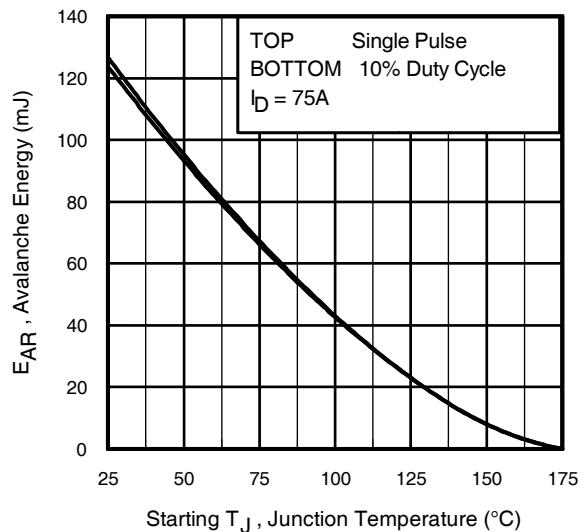
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature  
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**Fig 15.** Typical Avalanche Current Vs.Pulsewidth



**Fig 16.** Maximum Avalanche Energy Vs. Temperature

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**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
 (For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_D(\text{ave})$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

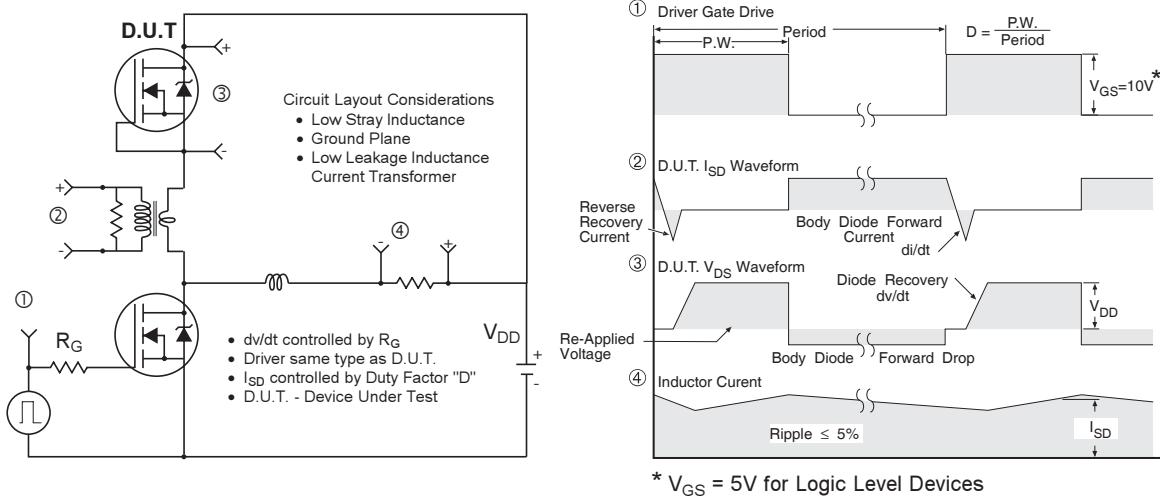
$$P_D(\text{ave}) = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

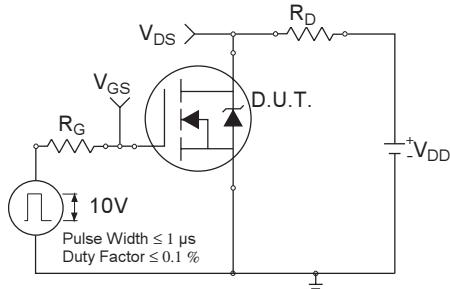
$$E_{AS(AR)} = P_D(\text{ave}) \cdot t_{av}$$

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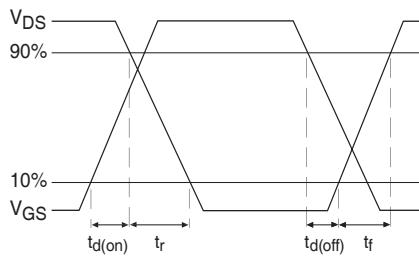
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**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 18a.** Switching Time Test Circuit



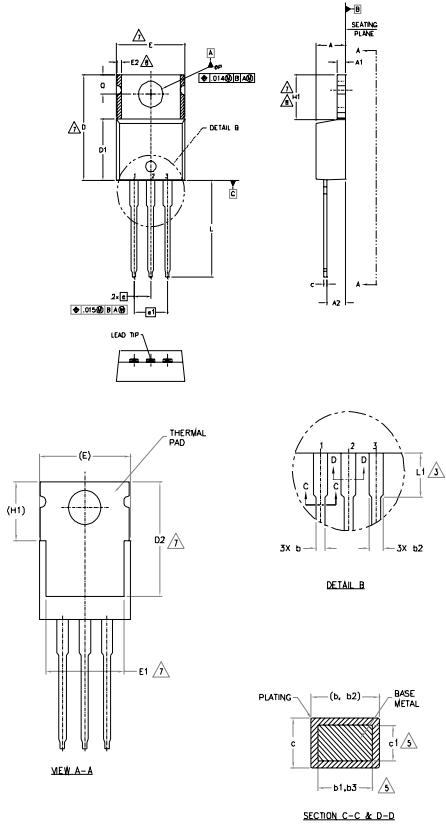
**Fig 18b.** Switching Time Waveforms

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# IRF1010Z/S/LPbF

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DIMENSION b1, b2 & c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION : INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1.
- DIMENSION E2 X H1 DEFINES A ZONE WHERE STAMPING AND SINGULATION IRRREGULARITIES ARE ALLOWED.
- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS		NOTES
	MILLIMETERS	INCHES	
	MIN.	MAX.	
A	.356	.483	.140 .190
A1	.051	.140	.020 .055
A2	2.03	2.92	.080 .115
b	.38	1.01	.015 .040
b1	.38	0.97	.015 .038
b2	1.14	1.78	.045 .070
b3	1.14	1.73	.045 .068
c	.36	.61	.014 .024
c1	.36	.56	.014 .022
D	14.22	16.51	.560 .650
D1	8.38	9.02	.330 .355
D2	11.68	12.88	.460 .507
E	9.65	10.67	.380 .420
E1	6.86	8.89	.270 .350
E2	-	0.76	- .030
e	2.54 BSC	.100 BSC	
e1	6.08 BSC	.200 BSC	
H1	5.84	6.86	.230 .270
L	12.70	14.73	.500 .580
L1	3.56	4.06	.140 .160
oP	3.54	4.08	.139 .161
O	2.54	3.42	.100 .135

**LEAD ASSESSMENTS**

1 - GATE
2 - DRAIN
3 - SOURCE

**ROUTING**

1 - GATE
2 - DRAIN
3 - SOURCE

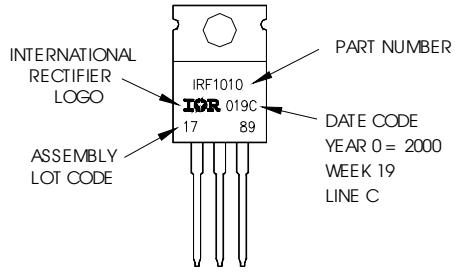
**INDEXES**

1 - ANODE
2 - CATHODE
3 - MIDDLE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
indicates "Lead-Free"



### Notes:

- For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/datasheets/data/auirf1010z.pdf>
- For the most current drawing please refer to IR website at <http://www.irf.com/package/>

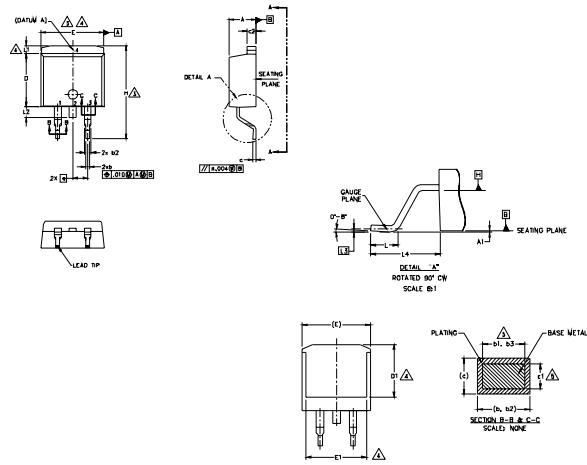
[www.irf.com](http://www.irf.com)

# IRF1010Z/S/LPbF

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## D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	0.00	0.254	.000	.010		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035	5	
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068	5	
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	—	.270	—	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	—	.245	—	4	
e	2.54	BSC	.100	BSC		
H	14.61	15.88	.575	.625		
L	1.78	2.79	.070	.110		
L1	—	1.65	—	.066		
L2	—	1.78	—	.070		
L3	0.25	BSC	.010	BSC		
L4	4.78	5.28	.188	.208		

### LEAD ASSIGNMENTS

#### DIODES

- 1 - ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 3 - CATHODE
- 3 - ANODE

#### HEXFET

- 1, - GATE
- 2, 4 - GATE
- 3 - SOURCE
- 2, 4 - Emitter

#### IGBT<sub>Si</sub> CoPACK

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

△ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.

△ THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

△ DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

6. DATUM A & B TO BE DETERMINED AT DATUM H.

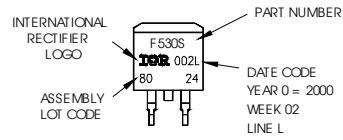
7. CONTROLLING DIMENSION: INCH.

8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

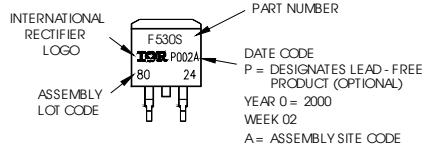
## D<sup>2</sup>Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position  
indicates "Lead - Free"



OR



### Notes:

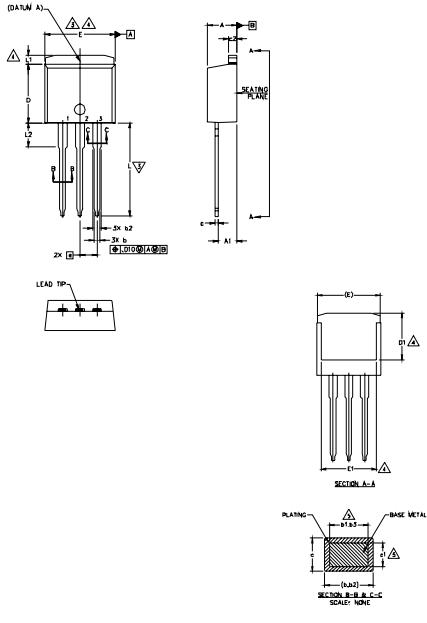
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/datasheets/data/auirf1010z.pdf>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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**IR** Rectifier

# IRF1010Z/S/LPbF

## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. CONTROLLING DIMENSION: INCH.
  7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

### LEAD ASSIGNMENTS

#### HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

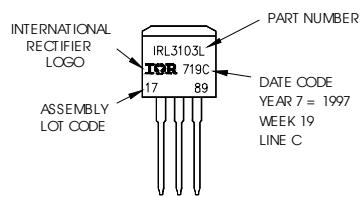
#### IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

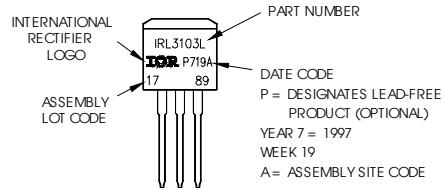
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
indicates "Lead - Free"



OR



### Notes:

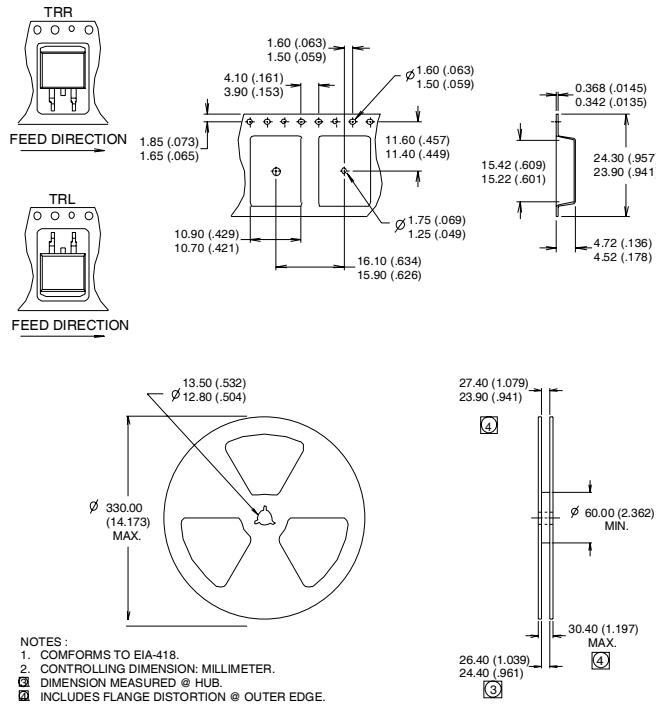
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/datasheets/data/auirf1010z.pdf>
  2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>
- [www.irf.com](http://www.irf.com)

# IRF1010Z/S/LPbF

International  
**IR** Rectifier

## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :  
1. CONFORMS TO EIA-418.  
2. CONTROLLING DIMENSION: MILLIMETER.  
3. DIMENSION MEASURED @ HUB.  
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

**TO-220AB package is not recommended for Surface Mount Application.**

### Notes:

- ① Repetitive rating: pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.05\text{mH}$   $R_G = 25\Omega$ ,  $I_{AS} = 75\text{A}$ ,  $V_{GS} = 10\text{V}$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is only applied to TO-220AB package.
- ⑧ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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