Analog Power AM2317P

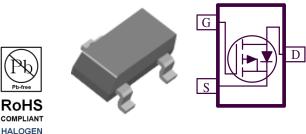
#### P - Channel Logic Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low $r_{DS(on)}$ provides higher efficiency and
	extends battery life

- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$\mathbf{r}_{\mathbf{DS(on)}}(\Omega)$ $\mathbf{I}_{\mathbf{D}}(\mathbf{A})$			
-30	$0.30 @ V_{GS} = -10 V$	-1.0		
-30	$0.50 @ V_{GS} = -4.5V$	-0.9		



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		$V_{DS}$	-30	V	
Gate-Source Voltage			±20	V	
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =25°C	Ι_	±0.9	A	
Continuous Drain Current	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	П	±0.75		
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	±10			
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	0.4	A	
Danie Diagram di ma	T <sub>A</sub> =25°C	D.	0.5	W	
Power Dissipation <sup>a</sup>	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	$P_{D}$	0.42		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	

FREE

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Maximum	Units		
a a	t <= 5 sec	D	250	°C/W	
Maximum Junction-to-Ambient"	Steady-State	$R_{THJA}$	285	C/W	

1

#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
D 4			Limits			
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Switch Off Characteristics						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = -250 \text{ uA}$	-30			
Zana Cata Valtaga Dunin Cumant		$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μА
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-10	
Gate-Body Leakage	Igss	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
Switch On Characteristics						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$	-0.80	-1.7	-2.6	V
On-State Drain Current <sup>A</sup>	ID(on)	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-2			A
		$V_{GS} = -10 \text{ V}, I_D = -1.0 \text{ A}$		0.25	0.30	
Drain-Source On-Resistance <sup>A</sup>	fDS(on)	$V_{GS} = -4.5 \text{ V}, I_{D} = -0.9 \text{ A T}_{J} = 55^{\circ} \text{C}$		0.53	0.66	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -0.9 \text{ A}$		0.45	0.50	
Forward Tranconductance <sup>A</sup>	gfs	$V_{DS} = -5 \text{ V}, I_{D} = -1.1 \text{ A}$		2		S
Diode Forward Voltage	$V_{\mathrm{SD}}$	$I_S = -0.4 \text{ A}, V_{GS} = 0 \text{ V}$		-0.70	-1.2	V
Dynamic <sup>b</sup>						
Total Gate Charge	Qg	101111 511		2.0	3.0	
Gate-Source Charge	Qgs	$V_{DS} = -10 \text{ V}, V_{GS} = -5 \text{ V},$		0.5		nC
Gate-Drain Charge	$Q_{gd}$	$I_D = -0.9 \text{ A}$		1.1		
Switching						
Turn-On Delay Time	$t_{d(on)}$			8	16	
Rise Time	$t_{\rm r}$	$V_{DS} = -10 \text{ V}, I_D = -0.9 \text{ A},$		16	32	ns
Turn-Off Delay Time	td(off)	$R_G = 50 \Omega$ , $V_{GEN} = -10 V$		36	93	1115
Fall-Time	$t_{\mathrm{f}}$			33	94	

#### Notes

- a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typical" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

## Typical Electrical Characteristics

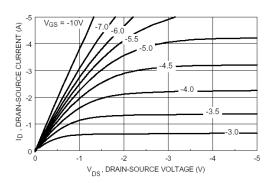


Figure 1. On-Region Characteristics

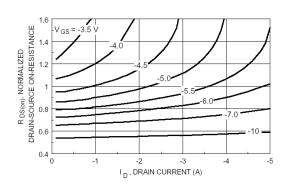


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

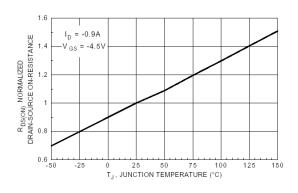


Figure 3. On-Resistance Variation with Temperature

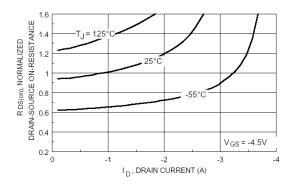


Figure 4. On-Resistance Variation with Gate to Source Voltage

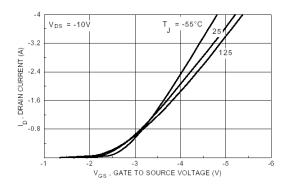


Figure 5. Transfer Characteristics

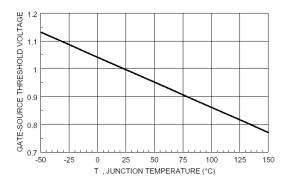
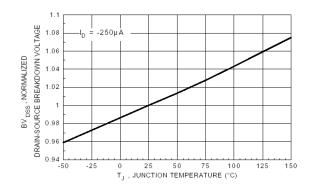


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

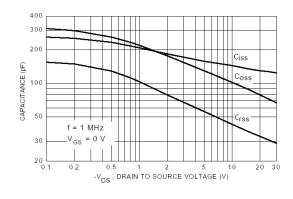
### Typical Electrical Characteristics



0.0001 0 0.2 0.4 0.6 0.8 1 1.2 1.4 -V<sub>SD</sub>, BODY DIODE FORWARD VOLTAGE (V)

Figure 7. Breakdown Voltage With Temperature

Figure 8. Body Diode Forward Voltage With Source Current & Temperature



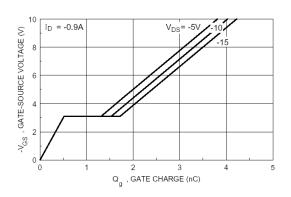


Figure 9. Capacitance Characteristic

Figure 10. Gate Charge Characteristic

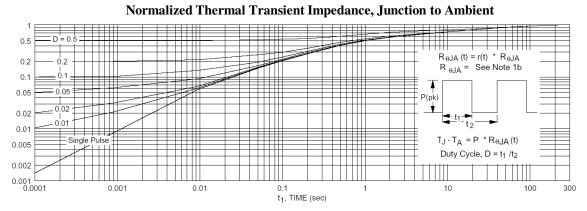


Figure 11. Transient Thermal Response Curve

## Typical Electrical Characteristics

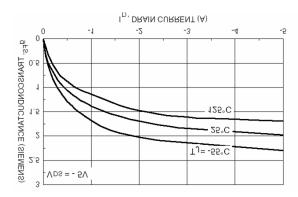


Figure 13. Transconductance Variation With Current & Temperature

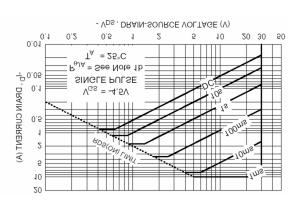


Figure 14. Maximum Safe Operation Area

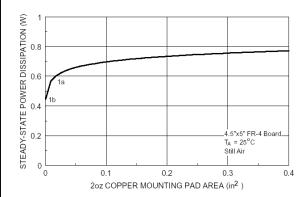


Figure 15. SOT-3 Maximum Steady-State Variation Power Dissipation versus Copper Pad Area

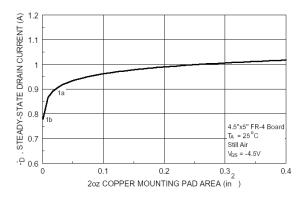
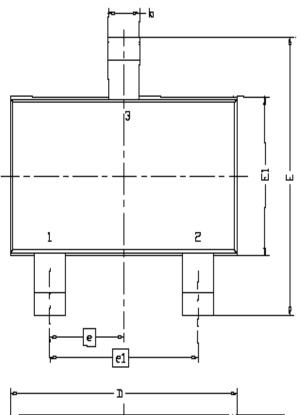


Figure 16. Maximum State-State Drain Current Versus Copper Pad Area

# Package Information



пты	MIL	LIMETE	RS	
DIM,	MIN	NDM	MAX	
Α	0.935	0.95	1.10	
A1	0.01	-	0.10	
A2	0.85	0.90	0.925	
Ь	0.30	0.40	0.50	
С	0.10	0.15	0.25	
D	2.70	2.90	3.10	
Ε	2.60	2.80	3.00	
E1	1.40	1.60	1.80	
6	0.95 BSC			
el	1.90 BSC			
L	0.30	0.40	0.60	
L1	0.60REF			
LZ	0,25BSC			
R	0.10			
θ	Ű.	4*	8,	
81	7*N□M			

